

LM2512A

Mobile Pixel Link (MPL-1), 24-Bit RGB Display Interface Serializer with Optional Dithering and Look Up Table

General Description

The LM2512A is a MPL Serializer (SER) that performs a 24-bit to 18-bit Dither operation and serialization of the video signals to Mobile Pixel link (MPL) levels on only 3 or 4 active signals. An optional Look Up Table (Three X 256 X 8 bit RAM) is also provided for independent color correction. 18-bit Bufferless or partial buffer displays from QVGA (320 x 240) up to VGA (640 x 480) pixels can utilize a 24-bit video source.

The interconnect is reduced from 28 signals to only 3 or 4 active signals with the LM2512A and companion deserializer easing flex interconnect design, size constraints and cost.

The LM2512A SER resides by the application, graphics or baseband processor and translates the wide parallel video bus from LVCMOS levels to serial Mobile Pixel Link levels for transmission over a flex cable (or coax) and PCB traces to the DES located near or in the display module.

When in Power_Down, the SER is put to sleep and draws less than 10µA. The link can also be powered down by stopping the PCLK (DES dependant) or by the PD* input pins.

The LM2512A provides enhanced AC performance over the LM2512. It implements the physical layer of the MPL-1 and uses a single-ended current-mode transmission.

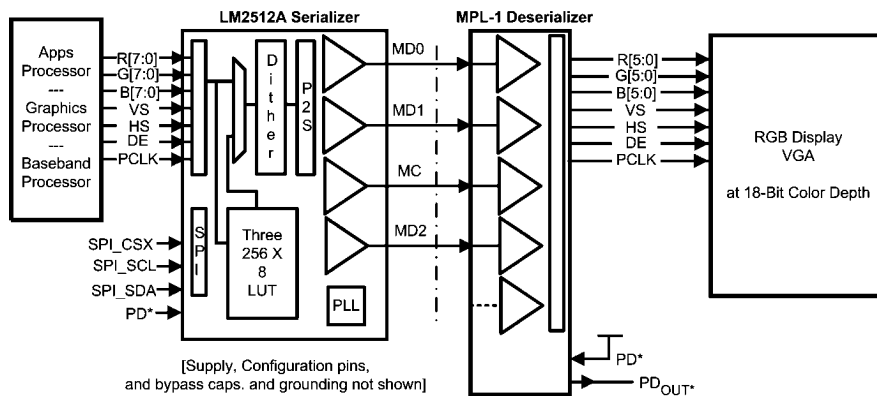
Features

- 24-bit RGB Interface support up to 640 x 480 VGA format
- Optional 24 to 18-bit Dithering
- Optional Look Up Table for independent color correction
- MPL-1 Physical Layer
- SPI Interface for Look Up Table control and loading
- Low Power Consumption & Powerdown state
- Level translation between host and display
- Optional Auto Power Down on STOP PCLK
- Frame Sequence bits auto resync upon data or clock error
- 1.6V to 2.0V core / analog supply voltage
- 1.6V to 3.0V I/O supply voltage range

System Benefits

- Dithered Data Reduction
- Independent RGB Color Correction
- 24-bit Color Input
- Small Interface, Low Power and Low EMI
- Intrinsic Level Translation

Typical 3 MD Lane Application Diagram - Bridge Chip



30015301

Ordering Information

NSID	Package Type, Qty Size	Package ID
LM2512ASM	49L UFBGA, 4.0 X 4.0 X 1 mm, 0.5 mm pitch, Reel of 1000	SLH49A
LM2512ASMXX	49L UFBGA, 4.0 X 4.0 X 1 mm, 0.5 mm pitch, Reel of 4500	SLH49A
LM2512ASN	40L LLP, 6.0 X 6.0 X 0.4 mm, 0.5 mm pitch, Reel of 1000	SNA40A
LM2512ASNXX	40L LLP, 6.0 X 6.0 X 0.4 mm, 0.5 mm pitch, Reel of 4500	SNA40A

Pin Descriptions

Pin Name	No. of Pins	I/O, Type	Description RGB Serializer
MPL SERIAL BUS PINS			
MD[2:0]	3	O, MPL	MPL Data Line Driver
MC	1	O, MPL	MPL Clock Line Driver
SPI INTERFACE and CONFIGURATION PINS			
SPI_CSX	1	I, LVCMOS	SPI_Chip Select Input SPI port is enabled when: SPI_CSX is Low, PD* is High, and PCLK is static.
SPI_SCL	1	I, LVCMOS	SPI_Clock Input
SPI_SDA/HS	1	IO, LVCMOS	Multi-function Pin: If SPI_CSX is Low, this is the SPI_SDA IO signal. Default is Input. Pin will be an output for a SPI Read transaction. See HS description below also.
PD*	1	I, LVCMOS	Power Down Mode Input SER is in sleep mode when PD* = Low, SER is enabled when PD* = High In PD*=L - Sleep mode: SPI interface is OFF, Register settings are RESET , and LUT data is retained.
RES1	1	I, LVCMOS	Reserved 1 - Tie High (V_{DDIO}) only available on SLH49A package
TM	1	I, LVCMOS	Test Mode L = Normal Mode, tie to GND H = Test Mode (Reserved)
NC	1	NA	Not Connected - Leave Open; only on SLH49A package
VIDEO INTERFACE PINS			
PCLK	1	I, LVCMOS	Pixel Clock Input Video Signals are latched on the RISING edge.
R[7:0] G[7:0] B[7:0]	24	I, LVCMOS	RGB Data Bus Inputs – Bit 7 is the MSB.
VS	1	I, LVCMOS	Vertical Sync. Input This signal is used as a frame start for the Dither block and is required. The VS signal is serialized unmodified.
SPI_SDA/HS	1	IO, LVCMOS	Multi-function Pin: Horizontal Sync. Input (when SPI_CSX = High) See SPI_SDA description above also.
DE	1	I, LVCMOS	Data Enable Input
POWER/GROUND PINS			
V_{DDA}	1	Power	Power Supply Pin for the PLL (SER) and MPL Interface. 1.6V to 2.0V
V_{DD}	1	Power	Power Supply Pin for the digital core. 1.6V to 2.0V
V_{DDIO}	3	Power	Power Supply Pin for the parallel interface I/Os. 1.6V to 3.0V
V_{SSA}	1	Ground	Ground Pin for PLL (SER) and MPL interface
V_{SS}	1	Ground	Ground Pin for digital core. For SN40A package, this is the large center pad.
V_{SSIO}	4	Ground	Ground Pin for the parallel interface I/Os. For SNA40A package, this is the large center pad.

Note:

I = Input, O = Output, IO = Input/Output. **Do not float input pins.**

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DDA})	-0.3V to +2.2V
Supply Voltage (V_{DD})	-0.3V to +2.2V
Supply Voltage (V_{DDIO})	-0.3V to +3.3V
LVC MOS Input/Output Voltage	-0.3V to (V_{DDIO} + 0.3V)
MPL Output Voltage	-0.3V to V_{DDA}
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C

ESD Ratings:

HBM - JESD22-A114C std.	$\geq \pm 2$ kV
MM - JESD22-A115-A std.	$\geq \pm 200$ V
CDM - JESD22-C101-C std.	$\geq \pm 500$ V

Maximum Package Power Dissipation Capacity at 25°C	
SLH49A Package	2.5 W
SNA40A Package	3.2 W
Derate SLH49A Package above 25°C	25 mW/°C
Derate SNA40A Package above 25°C	26 mW/°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DDA} to V_{SSA} and V_{DD} to V_{SS}	1.6	1.8	2.0	V
V_{DDIO} to V_{SSIO}	1.6		3.0	V
PClock Frequency (4X)	7.5		22.5	MHz
PClock Frequency (6X)	5		15	MHz
MC Frequency	30		90	MHz
Ambient Temperature	-30	25	85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
MPL							
I _{OLL}	Logic Low Current (5X I _B)			3.947I _B	5.0 I _B	6.842I _B	μA
I _{OMS}	Mid Scale Current				3.0 I _B		μA
I _{OLH}	Logic High Current (1X I _B)			0.711 I _B	1.0 I _B	1.368 I _B	μA
I _B	Current Bias				190		μA
I _{OFF}	MPL Leakage Current	V _{MPL} = 0V		−2		+2	μA
LVCMOS (1.6V to 3.0V Operation)							
V _{IH}	Input Voltage High Level			0.7 V _{DDIO}		V _{DDIO}	V
V _{IL}	Input Voltage Low Level			GND		0.3 V _{DDIO}	V
V _{HY}	Input Hysteresis				100		mV
I _{IN}	Input Current			−1	0	+1	μA
V _{OH}	Output Voltage High Level	SPI_SDA	I _{OH} = −1 mA	0.7 V _{DDIO}		V _{DDIO}	V
V _{OL}	Output Voltage Low Level		I _{OL} = 1 mA	V _{SSIO}		0.2 V _{DDIO}	V
SUPPLY CURRENT							
I _{DD}	Total Supply Current - Enabled (Note 4)	MC = 80 MHz, Checkerboard Pattern 3 MD Lane (Note 5)	V _{DDIO}		0.02	0.07	mA
			V _{DD} /V _{DDA}		5.4	9.0	mA
		MC = 60 MHz, Checkerboard Pattern 2 MD Lane	V _{DDIO}		0.01		mA
			V _{DD} /V _{DDA}		4.1		mA
	Supply Current -Enabled	MC = 60 MHz, Pseudo-Random Pattern 2 MD Lane	V _{DDIO}		0.02		mA
			V _{DD} /V _{DDA}		3.7		mA
I _{DDZ}	Supply Current—Disable Power Down Modes Ta = 25°C	PD* = L	V _{DDIO}		<1	2	μA
			V _{DD} /V _{DDA}		<1	5	μA
		Stop Clock	V _{DDIO}		<1	2	μA
			V _{DD} /V _{DDA}		<1	5	μA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PARALLEL BUS TIMING						
t _{SET}	Set Up Time	SER Inputs <i>Figure 1</i>	5			ns
t _{HOLD}	Hold Time		5			ns
SERIAL BUS TIMING						
t _{DVBC}	Serial Data Valid before Clock Edge	SER Data Pulse Width <i>Figure 2</i> , (Notes 10, 11)	0.38			UI
t _{DVAC}	Serial Data Valid after Clock Edge		0.38			UI
POWER UP TIMING						
t ₀	Bias Up Time	<i>Figure 9</i>		200		PCLK cycles
t ₁	MC Pulse Width LOW			200		PCLK cycles
t ₂	MC Pulse Width HIGH			20		PCLK cycles
t ₃	MC Pulse LOW			8		PCLK cycles
t ₄	MC Pulse LOW - SER PLL Lock Counter			600		PCLK cycles
t _{PZXclk}	Enable Time - Clock Start	PCLK to MC _{OUT} <i>Figure 4</i>		(Note 6)		
MPL POWER OFF TIMING						
t _{PAZ}	Disable Time to Power Down	(Note 8)			15	ms
t _{PXZclk}	Disable Time - Clock Stop	PCLK to MC _{OUT} <i>Figure 3</i>		2		PCLK cycles
SPI INTERFACE						
t _{ACC}	SPI Data Active (SDA_device)	<i>Figure 16</i>	0		50	ns
t _{OHR}	SPI Data Tri-State (SDA_device)		0		50	ns

Recommended Input Timing Requirements (PCLK and SPI)

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PIXEL CLOCK (PCLK)						
f_{PCLK}	Pixel Clock Frequency	3 MD Lane, (4X)	7.5		22.5	MHz
		2 MD Lane, (6X)	5		15	MHz
PCLK_{DC}	Pixel Clock Duty Cycle		30	50	70	%
t_{T}	Transition Time	(Notes 7, 11)	2	>2		ns
t_{STOPpclk}	Clock Stop Gap	(Notes 9, 11)	4	2		PCLK cycles

SPI INTERFACE

f_{SCLw}	SCL Frequency	WRITE			10	MHz
f_{SCLr}		READ			6.67	MHz
t_{s0}	CSX Set Time	Figure 15		60		ns
t_{s1}	SI Set Time			30		ns
t_{h1}	SI Hold Time			30		ns
t_{w1h}	SCL Pulse Width High	Figures 15, 16	WRITE	35		ns
			READ	60		ns
t_{w1l}	SCL Pulse Width Low		WRITE	35		ns
			READ	60		ns
t_{r}	SCL Rise Time	Figure 15			5	ns
t_{f}	SCL Fall Time				5	ns
t_{OH}	SI Hold Time			30		ns
t_{h0}	CSX Hold Time			65		ns
t_{w2}	CSX OFF Time			100		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for $V_{\text{DDIO}} = 1.8\text{V}$ and $V_{\text{DD}} = V_{\text{DDA}} = 1.8\text{V}$ and $T_{\text{A}} = 25^{\circ}\text{C}$.

Note 3: Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

Note 4: For IDD tests - input signal conditions are: (swing, edge, freq, DE = H, VS = L, HS = L, RGB Checkerboard Pattern: AAAAAA-555555)

Note 5: Total Supply Current Conditions: checkerboard data pattern, 20MHz PCLK (3MDs), TYP $V_{\text{DDIO}} = V_{\text{DDA}} = V_{\text{DD}} = 1.8\text{V}$, MAX VDDIO = 3.0V, MAX VDDA = VDD = 2.0V.

Note 6: Enable Time is a complete MPL start up comprised of $t_0 + t_1 + t_2 + t_3 + t_4$.

Note 7: Maximum transition time is a function of clock rate and should be less than 30% of the clock period to preserve signal quality.

Note 8: Guaranteed functionally by the I_{DDZ} parameter. See also Figure 10.

Note 9: This is the minimum time that the PCLK needs to be held off for in order for the device to be reset. Once PCLK is reapplied, a PLL Lock is required and start up sequence before video data is serialized.

Note 10: 1 UI is the serial data MD pulse width = $1 / 8 \times \text{PCLK}$ (3 MD lanes), 1 UI is the serial data MD pulse width = $1 / 12 \times \text{PCLK}$ (2 MD lanes)

Note 11: This is a functional parameter and is guaranteed by design or characterization.

Timing Diagrams

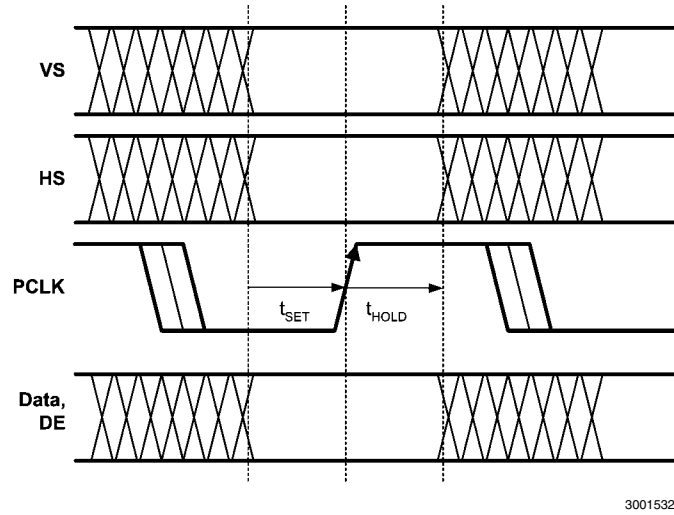


FIGURE 1. Input Timing for RGB Interface

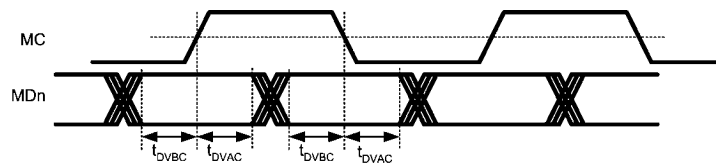


FIGURE 2. Serial Data Valid

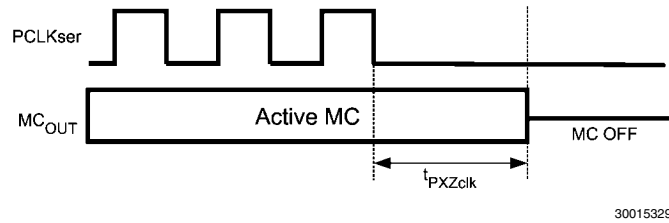


FIGURE 3. Stop PClock Power Down

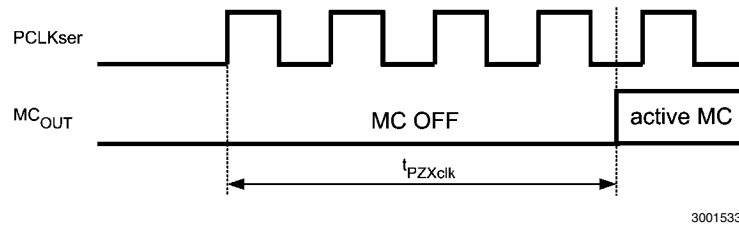
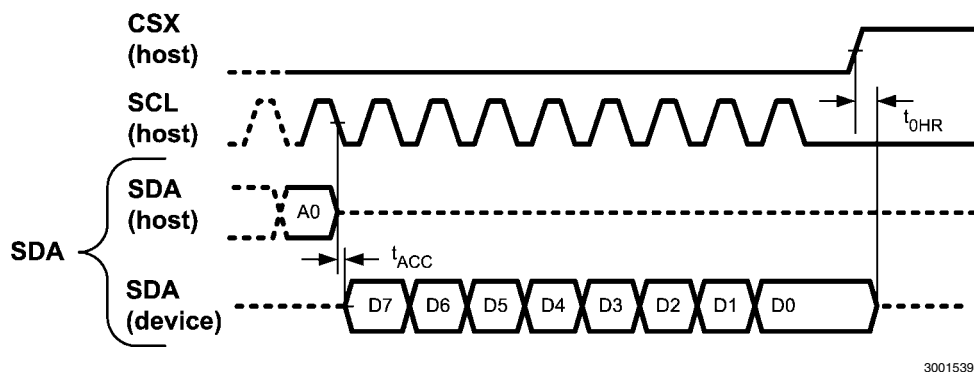


FIGURE 4. Stop PClock Power Up



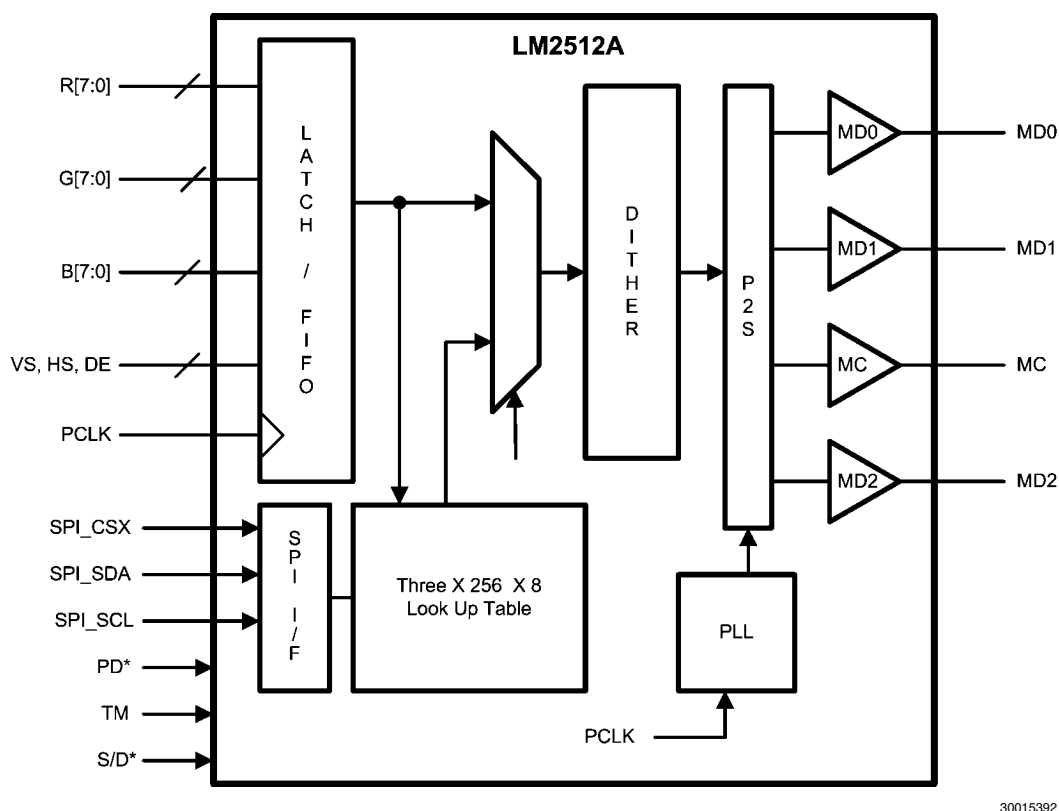
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FIGURE 5. SPI Interface

Functional Description

The LM2512A is a Mobile Pixel Link (MPL) Serializer that serializes a 24-bit RGB plus three control signals (VS, HS, and DE) to two or three MPL MD lines plus the serial clock MC. Two options are provided: 24-bit RGB data dithering to 18

bits, and an optional Look Up Table. The three 256 X 8-bit RAMs may also be used and is controlled via a 3-wire SPI interface. The LM2512A is compatible with certain discrete MPL Deserializers and also Display Drivers with integrated MPL Deserializers (i.e. FPD95320).



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FIGURE 6. General LM2512A Block Diagram

BUS OVERVIEW

The LM2512A is a multi-lane MPL Serializer that supports a 24-bit RGB source interface. The MPL physical layer is purpose-built for an extremely low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the MPL receiver. A maximum raw throughput of 480 Mbps (3-lane raw) is possible with this chipset. The MPL interface is designed for use with common 50Ω to 100Ω lines using standard materials and connectors. Lines may be microstrip or stripline construction. Total length of the interconnect is expected to be less than 20cm.

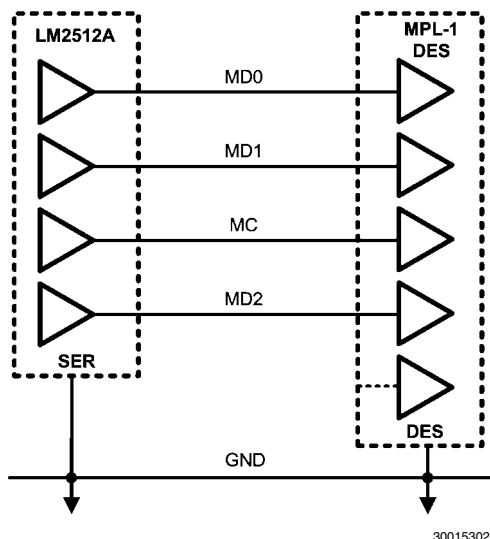


FIGURE 7. Three MD Lane MPL Interface

SERIAL BUS TIMING

Data valid is relative to both edges of a RGB transaction as shown in *Figure 8*. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, and Skew between data lines should be less than 500ps.

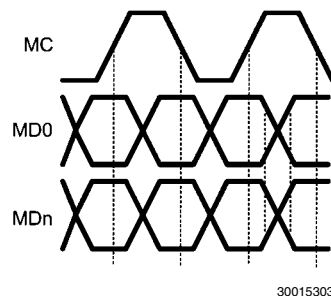


FIGURE 8. Dual Link Timing

SERIAL BUS PHASES

There are three bus phases on the MPL serial bus. These are determined by the state of the MC and MD lines. The MPL bus phases are shown in *Table 1*.

The LM2512A supports MPL Level 0 Enhanced Protocol with a Class 0 PHY.

TABLE 1. Link Phases

Name	MC State	MDn State	Phase Description	Pre-Phase	Post-Phase
OFF (O)	0	0	Link is Off	A, or LU	LU
LINK-UP (LU)	0LHL	000L	Start Up Pulse	O	A or O
Active (A)	A	X	Streaming Data	LU	O

Notes on MC/MD Line State:

0 = no current (off)

L = Logic Low—The higher level of current on the MC and MD lines

H = Logic High—The lower level of current on the MC and MD lines

X = Low or High

A = Active Clock

SERIAL BUS START UP TIMING

In the Serial Bus OFF phase, SER line drivers for MDs and MC are turned off such that zero current flows over the MPL lines. On the SER side, when the PD* input pin is de-asserted (driven High), or with PD* = High and the PCLK is turned on, the SER will power up its bias block during t0.

The SER will next drive the MC line to the logic Low (5I current) state for 200 PCLK cycles (t1). The DES devices detect the current flowing in the MC line, and powers up its analog circuit blocks (or alternately is controlled by its PD* input pin - device specific).

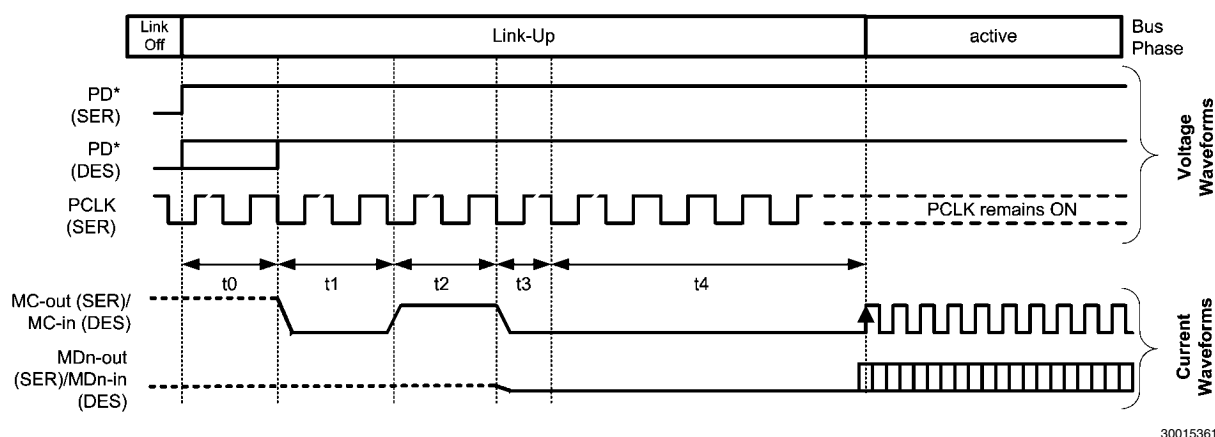
The SER then drives the MC line to a logic High (1I current) for 20 PCLK cycles (t2). On the MC low-to-high transition, the

DES samples the current and optimizes its current sources to match that of the drivers.

The MC is now driven to a logic Low (5I current) for 8 PCLK cycles (t3).

Next the SER PLL is locked to the PCLK. A hold off counter of 600 PCLK cycles is used to hold off until the PLL has locked and is stable (t4). At this point, streaming RGB information is now sent across the MPL link.

Link-Up is shown in *Figure 9*. The MC and MDn signals are current waveforms. Data at the DES output will appear a latency delay later.

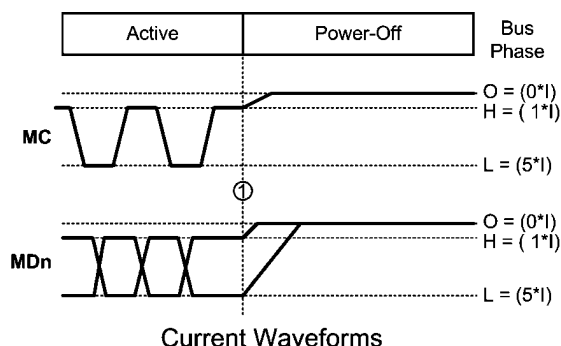


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FIGURE 9. MPL Power Up Timing

OFF PHASE

In the OFF phase, MPL transmitters are turned off with zero current flowing on the MC and MDn lines. *Figure 10* shows the transition of the MPL bus into the OFF phase. If an MPL line is driven to a logical Low (high current) when the OFF phase is entered it may temporarily pass through as a logical High (low current) before reaching the zero line current state. The link may be powered down by asserting both the SER's and DES's PD* input pins (Low) or by stopping the PCLK (DES dependant). This causes the devices to immediately put the link to the OFF Phase and internally enter a low power state.



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FIGURE 10. Bus Power Down Timing

RGB VIDEO INTERFACE

The LM2512A is transparent to data format and control signal timing. Each PCLK, RGB inputs, HS, VS and DE are sampled on the rising edge of the PCLK. A PCLK by PCLK representation of these signals is duplicated on the opposite device after being transferred across the MPL Level-0 interface.

The LM2512A can accommodate a wide range of display formats. QVGA to VGA can be supported within the 2MHz to 20 MHz PCLK input range.

The 24-bit RGB (R0-7, G0-7, B0-7) color information is dithered to 18 bits then serialized, followed by the control bits VS (VSYNC), HS (HSYNC), DE (Data Enable) and PE (Odd Parity) and Frame Sequence (F[1:0]) bits.

The default configuration is for 2 MD lanes plus the MC. Via the SPI Interface, the Serializer can be configured for a 3 MD Lane configuration.

When transporting color depth below 24-bit, the 24-bit protocol can be used by offsetting the color data. The LSBs of the RGB are not used and data is offset toward the upper (MSB) end of the bit fields. Unused inputs should be tied off.

At a maximum PCLK of 20 MHz (3MDs), a 80MHz MC clock is generated. The data lane rate uses both clock edges, thus 160Mbps (raw) are sent per MD lane.

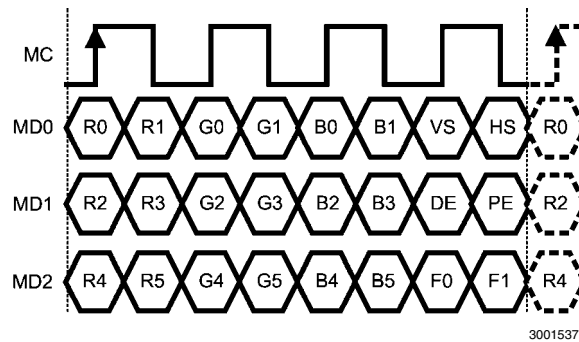


FIGURE 11. 24-bit to 18-bit Dithered, 3 MD Lane, RGB Transaction

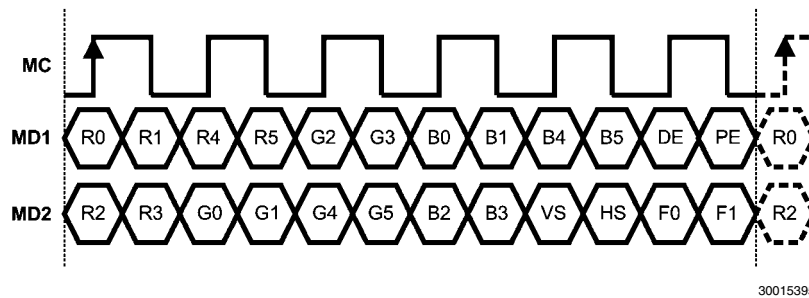


FIGURE 12. 24-bit to 18-bit Dithered, 2 MD Lane (Default), RGB Transaction (NOTE MD1 and MD2)

Serial Payload Parity Bit

Odd Parity is calculated on the RGB bits, control (VS, HS, and DE) bits and F0, F1 bits and then sent from the SER to the DES via the serial PE bit. This is included for compatibility with certain MPL Deserializers.

Synchronization Detect and Recovery

If a data error or clock slip error occurs over the MPL link, the RGB MPL Deserializer can detect this condition and recover from it. The method chosen is a data transparent method, and has very little overhead because it does not use a data expansion coding method. For the Dithered 18-bit color transaction, it uses two bits that are already required in the 4 MC cycle transaction. Total overhead for each pixel is 3/24 or 12.5%.

The LM2512A MPL RGB Serializer simply increments the two bit field F[1:0] on every pixel (MPL frame) transmitted. Therefore every four MPL frames, the pattern will repeat. It is very unlikely that this pattern would be found within the payload data, and if it were found, the probability that it would repeat for many frames becomes infinitely small. This code is used by the MPL Deserializer to detect any frame alignment problems and quickly recover.

The RGB MPL Deserializer, upon a normal power up sequence, starts in the proper synchronization. If synchroniza-

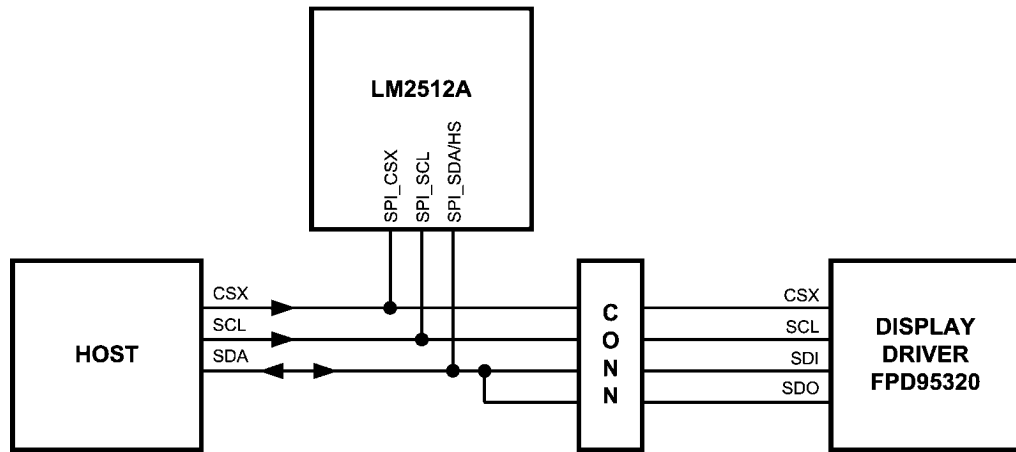
tion is lost for any reason, it searches for the incrementing pattern. Once found, it resynchronizes the output pixel data and timing signals. See MPL DES Datasheet for details on how the specific DES handles the Frame Sequence.

OPTIONAL DITHERING FEATURE

The LM2512A is a 2 or 3-Lane MPL Serializer, 24-bit RGB input data (8-bits/color channel) is internally dithered to 18-bits (6-bits/color channel) using a high-quality stochastic dithering process. This process has a "blue noise" characteristic that minimizes the visibility of the dither patterns. The resulting data stream of 18-bit data is then serialized and transmitted via MPL.

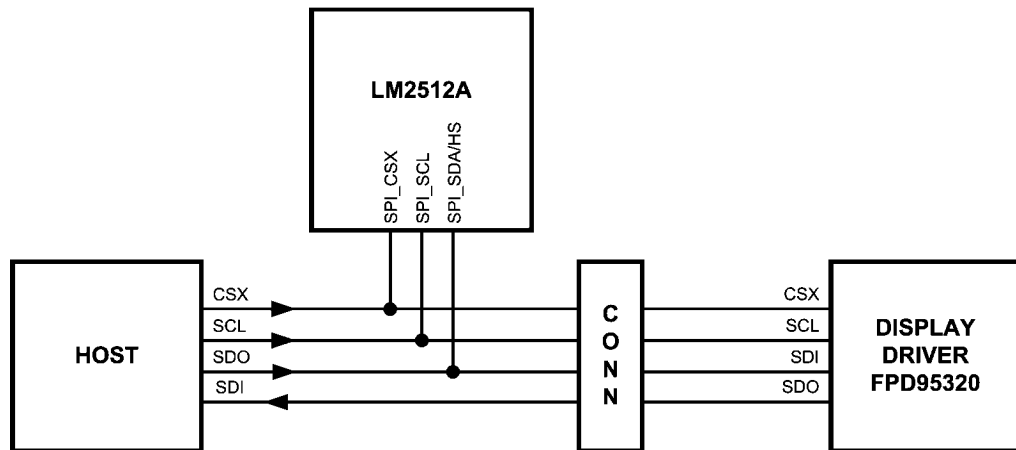
The Dither circuitry requires the VS control signal for proper operation. This signal is used to generate a internal signal that marks the start of the (video) frame. The serializer samples and sends the VS information unmodified.

Dithering parameters are controlled by two registers. When the dithering is bypassed, only RGB[7:2] is serialized and transmitted for 18-bit input RGB [5:0] (MSB aligned). RGB [1:0] should not be connected and the unused input should be tied low; do not leave input open.



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FIGURE 13. LM2512A WRITE & READ to 3-signal SPI HOST



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FIGURE 14. LM2512A WRITE only to 4-signal SPI HOST

LM2512A SPI Registers

Name	Address	Type	Description	Default
Command	0x00	R/W	Bit 0 = LUT Enable 0'b = LUT Disabled, 1'b = LUT Enabled Bit 4 = Special Register Access 0'b = SRA Locked, 1'b = SRA Unlocked For access to Registers 0x01, 0x08, 0x09, 0x0A, the Special Register Access bit must be unlocked. Must write all 8 bits.	00'h
Configuration (Note 13)	0x01	R/W	Bit 4 = MPL Edge Rate 0'b = normal edge, 1'b = slow edge All other bits reserved, must be written as 0s.	00'h
Red RAM Address	0x02	R/W	Red Address	00'h
Red RAM Data	0x03	R/W	Red Data	XX'h
Green RAM Address	0x04	R/W	Green Address	00'h
Green RAM Data	0x05	R/W	Green Data	XX'h
Blue RAM Address	0x06	R/W	Blue Address	00'h
Blue RAM Data	0x07	R/W	Blue Data	XX'h
Dither Configuration1 (Note 13)	0x08	R/W	Bit 0 - Dither Bypass 1'b = Bypass Dither, 0'b = Dither ON Bit 1 - DE INV 1'b = Active Low DE, 0'b = Active High DE Does not alter DE signal, dither block input only. Bit 2 - VS INV 1'b = Active Low VS signal, 0'b = Active High VS signal. Does not alter VS signal, dither block input only. Bit 3 - Reserved Bit 4 - Tempen0 1'b = Transposed Dither Pattern, 0'b = Even and odd frames use same dither pattern Bit 5 - Tempen1 1'b = Temporal Dithering is Enabled, 0'b = Disabled Bit 6 - Dith3 - Dither Amplitude 1'b = set to 3 bits, 0'b = set to 4 bits Bit 7 - Reserved	61'h
Dither Configuration2 (Note 13)	0x09	R/W	Dither Parameter Reserved , Default value recommended.	67'h
Lane Scale (Notes 13, 15)	0x0A	W	Bit[2:0] 000'b = Reserved 010'b = 2 MD Lanes (Default) 100'b = 3 MD Lanes all others= Reserved	02'h
Reserved (Note 14)	0x0B- 0x15	na	Reserved	
Device Select (Unlock/Lock)	0x16	R/W	0xFF'h enables LM2512A SPI All other values disables LM2512A SPI (0x00 to 0xFE)	00'h
Reserved (Note 14)	0x17- 0x7F	na	Reserved	

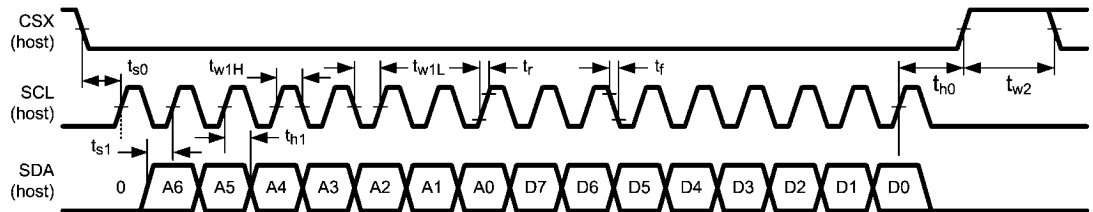
Note 12: If a WRITE is done to a reserved bits, data should be all 0's. If a READ is done to a reserved location, either 1's or 0's may be returned. Mask reserved data bits.

Note 13: This register must be unlocked first through bit 4 of register 0.

Note 14: DO NOT write to Reserved Registers.

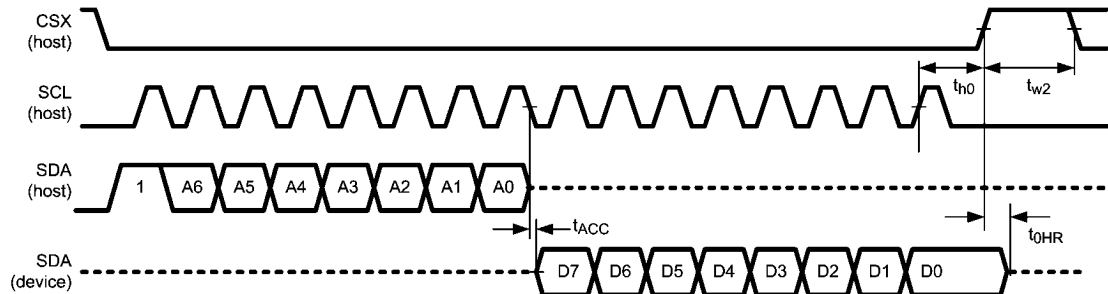
Note 15: WRITE ONLY Register, read of this register is not supported.

SPI Timing



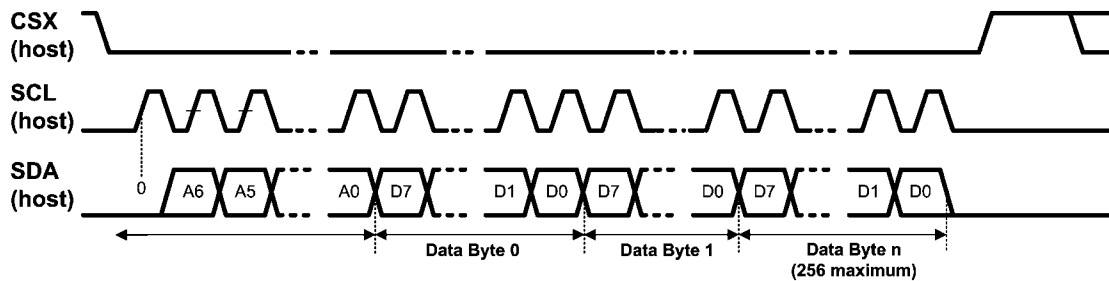
30015390

FIGURE 15. 16-bit SPI WRITE



30015391

FIGURE 16. 16-bit SPI READ



30015393

FIGURE 17. SPI PAGE WRITE

Power Up Sequence

The MPL Link must be powered up and enabled in a certain sequence for proper operation of the link and devices. The following list provides the recommended sequence:

1. Apply Power (See Power Supply Section)
2. PD* Input should be held low until Power is stable and within specification and PCLK is driven to a static level.
3. PD* is driven HIGH, SPI interface is now available.
4. To program the device via the SPI interface:
 - Select / Unlock the LM2512A, Write FF'h to REG 16'h
5. Condition the DES as required
6. Start PCLK, after the DES is calibrated and the SER PLL Locked, streaming data transmission will occur.

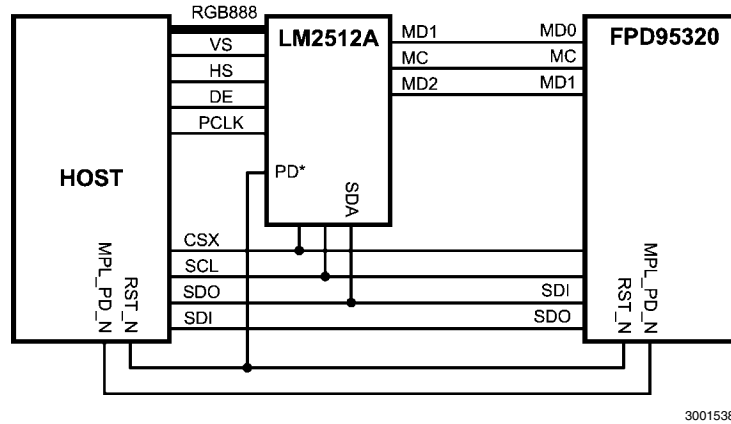


FIGURE 18. Typical Application Connection Diagram

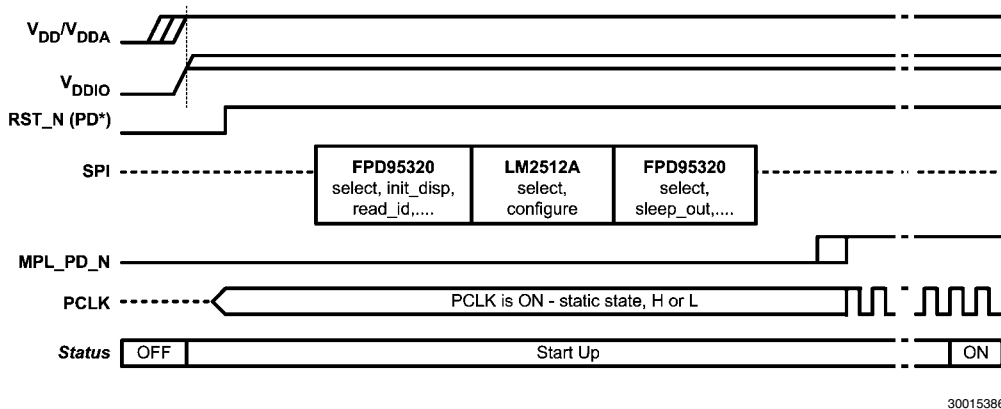


FIGURE 19. Power Up Sequence

A typical connection diagram is shown in Figure 18. The LM2512A SPI is configured to support write only transactions in this example. The FPD95320 can support both writes and reads on its SPI interface. Figure 19 shows a typical power up sequence using the shared SPI interface. Power is brought up first. The RST_N signal is held low until power to the FPD95320 (not shown) and the LM2512A is stable and within specifications. Next the RST_N signal is driven High, which allows access to the SPI interfaces. The PCLK should also be turned on and held at a static level (High or Low). The FPD95320 is selected first via a write to register 16'h (see FPD95320 datasheet) and the display is initialized. Next a write of FF'h to register 16'h. This command will Lock the FPD95320 SPI interface and Select / Unlock the LM2512A

SPI interface. By default, the LM2512A powers up in 2 MD lanes with the Dither and the LUT disabled. The Look-up Table - LUT is accessible by enabling bit 0 of the command register 00'h. The Special Register Access - SRA are also accessible for lane scaling by enabling bit 4 of the command register 00'h. To enable the LUT and unlock SRA, write of 11'h to register 00'h (See LM2512A SPI Register Table). To change to 3 MD lanes, write of 04'h to register 0A'h. Next additional commands are sent to the FPD95320 by issuing a Unlock command to the FPD95320 register 16'h which also de-selects / locks the LM2512A SPI. After the SPI commands are completed, the MPL_PD_N signal is driven High to arm the Deserializer for the MPL start sequence. The PCLK is started up, and the SER will calibrate the DES and lock to the

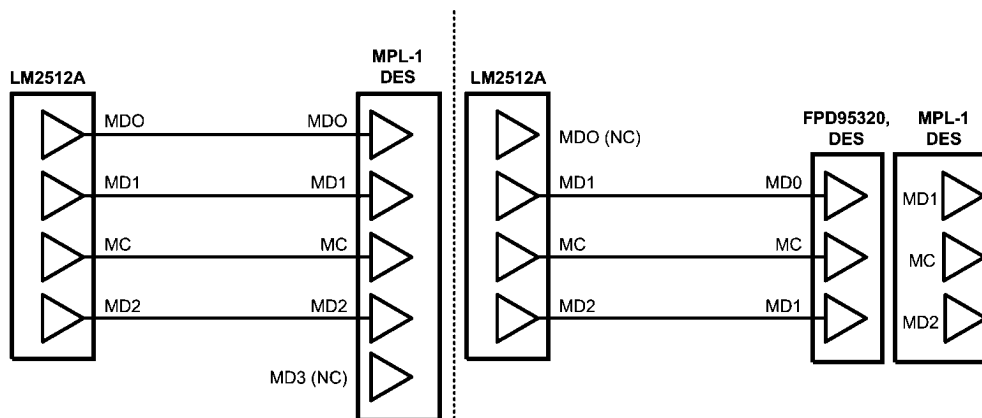
incoming PCLK signal. Once this is completed, video data transmission occurs and the link is ON.

Application Configurations

Many different application configurations are possible with the flexible LM2512A Serializer. These include:

- LM2512A - 2 MD Lane to FPD95320 Display Driver
- LM2512A - 2 MD Lane to LM2506 DES
- LM2512A - 3 MD Lane - Reserved for future use

Take care in reviewing the MPL signals and serial bit mapping to ensure proper connection between the devices.



30015387

FIGURE 20. Application Configurations

LM2512A Operation

POWER SUPPLIES

The V_{DD} and V_{DDA} (MPL and PLL) must be connected to the same potential between 1.6V and 2.0V. V_{DDIO} powers the logic interface and may be powered between 1.6V and 3.0V to be compatible with a wide range of host and target devices. V_{DD}/V_{DDA} should be powered ON at the same time as V_{DDIO} or before. V_{DDIO} then V_{DD}/V_{DDA} is not recommended.

BYPASS RECOMMENDATIONS

Bypass capacitors should be placed near the power supply pins of the device. Use high frequency ceramic (surface mount recommended) 0.1 μ F capacitors. A 2.2 to 4.7 μ F Tantalum capacitor is recommended near the SER V_{DDA} pin for PLL bypass. Connect bypass capacitors with wide traces and use dual or larger via to reduce resistance and inductance of the feeds. Utilizing a thin spacing between power and ground planes will provide good high frequency bypass above the frequency range where most typical surface mount capacitors are less effective. To gain the maximum benefit from this, low inductance feed points are important. Also, adjacent signal layers can be filled to create additional capacitance. Minimize loops in the ground returns also for improved signal fidelity and lowest emissions.

UNUSED/OPEN PINS

Unused inputs **must** be tied to the proper input level—do not float them.

PHASE-LOCKED LOOP

A PLL is enabled to generate the serial link clock. The Phase-locked loop system generates the serial data clock at 4X or 6X of the input clock depending upon the number of MD Lanes selected. The MC rate is limited to 80 MHz for this enhanced Class 0 MPL PHY.

POWER DOWN/OFF CONFIGURATION / OPTIONS AND CLOCK STOP

The LM2512A (SER) can be controlled by its PD^* input pin or via a auto power down mode that monitors the PCLK input signal.

For PD^* Input Power Down control, a GPO signal from the host is used to enable and disable the LM2512A and the DES. The LM2512A is enabled when the PD^* input is High and disabled when the PD^* input is Low.

When using the auto power down mode, the PD^* input needs to be held High. When the PCLK is held static, the SER will detect this condition and power down. When the PCLK is restarted, the SER powers up, The DES is calibrated, and the PLL locks to the incoming clock signal. Once this is complete, video data transmission can occur. See *Figures 3, 4 and Figure 9*. The stopping of the pixel clock should be done cleanly. The minimum clock stop gap should be at least 4 PCLK cycles wide. Floating of the PCLK input pin is not recommended. Consult the MPL DES datasheet to determine requirements that the DES requires.

LM2512A vs LM2512

The following list provides the differences between the LM2512 and the enhanced LM2512A.

- Increased I_{data} Current
- Enhanced Current Matching
- Enhanced MC Duty Cycle
- 2 MD Lane Default Configuration
- Dither Off Default
- LUT Default State (I_{DDZ})
- MPL Driver Edge Rate Control Option

Application Information

SYSTEM BANDWIDTH CALCULATIONS

For a HVGA (320 X 480) application with the following assumptions: 60 Hz +/-5% refresh rate, 10% blanking, RGB666, and 2 MD Lanes and following calculations can be made:

Calculate PCLK - $320 \times 480 \times 1.1 \times 60 \times 1.05 = 10.6 \text{ MHz}$
PCLK

Calculate MC rate - since the application is 2 MD lanes, PCLK X 6 is the MC rate or 63.87 MHz. Also check that this MC rate does not exceed the MC maximum rate for the chipset.

Calculate MD rate - MPL uses both edges of the MC to send serialized data, thus data rate is 2X the MC rate, or 127.7 Mbps per MD lane in our example.

Calculate the application throughput - using 2 MD lanes, throughput is 2 X of the MD rate or 255.5 Mbps of raw band width.

For a VGA (640 X 480) application with the following assumptions: 55 Hz +/-5% refresh rate, 10% blanking, RGB666, and 3 MD Lanes and following calculations can be made:

Calculate PCLK - $640 \times 480 \times 1.1 \times 55 \times 1.05 = 19.5 \text{ MHz}$
PCLK

Calculate MC rate - since the application is 3 MD lanes, PCLK X 4 is the MC rate or 78.1 MHz. Also check that this MC rate does not exceed the MC maximum rate for the chipset.

Calculate MD rate - MPL uses both edges of the MC to send serialized data, thus data rate is 2X the MC rate, or 156 Mbps per MD lane in our example.

Calculate the application throughput - using 3MD lanes, throughput is 3X of the MD rate or 468 Mbps of raw band width.

SYSTEM CONSIDERATIONS

When employing the MPL SER/DES chipset in place of a parallel video bus, a few system considerations must be taken into account. Before sending video data to the display, the SER/DES must be ready to transmit data across the link. The MPL link must be powered up, and the PLL must be locked and the DES calibrated.

FLEX CIRCUIT RECOMMENDATIONS

The MPL lines should generally run together to minimize any trace length differences (skew). For impedance control and also noise isolation (crosstalk), guard ground traces are recommended in between the signals. Commonly a Ground-Signal-Ground (GSGSGS) layout is used. Locate fast edge

rate and large swing signals further away to also minimize any coupling (unwanted crosstalk). In a stacked flex interconnect, crosstalk also needs to be taken into account in the above and below layers (vertical direction). To minimize any coupling locate MPL traces next to a ground layer. Power rails also tend to generate less noise than LVCMOS so they are also good candidates for use as isolation and separation.

The interconnect from the SER to the DES typically acts like a transmission line. Thus impedance control and ground returns are an important part of system design. Impedance should be in the 50 to 100 Ohm nominal range for the LM2512A. Testing has been done with cables ranging from 40 to 110 Ohms without error (BER Testing). To obtain the impedance, adjacent grounds are typically required (1 layer flex), or a ground shield / layer. Total interconnect length is intended to be in the 20cm range, however 30cm is possible at lower data rates. Skew should be less than 500ps to maximize timing margins.

GROUNDING

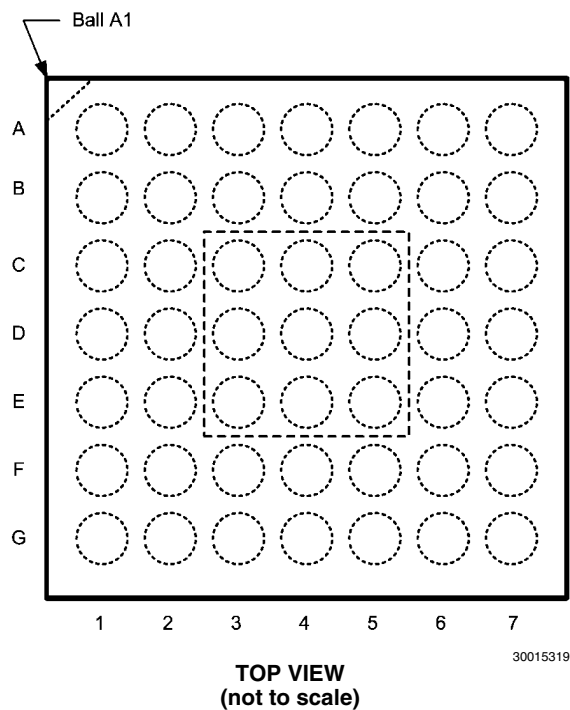
While the LM2512A employs three separate types of ground pins, these are intended to be connected together to a common ground plane. The separate ground pins help to isolate switching currents from different sections of the integrated circuit (IC). Also required is a nearby signal return (ground) for the MPL signals. These should be provided next to the MPL signals, as that will create the smallest current loop area. The grounds are also useful for noise isolation and impedance control.

PCB RECOMMENDATIONS

General guidelines for the PCB design:

- Floor plan, locate MPL SER near the connector to limit chance of cross talk to high speed serial signals.
- Route serial traces together, minimize the number of layer changes to reduce loading.
- Use ground lines as guards to minimize any noise coupling (guarantees distance).
- Avoid parallel runs with fast edge, large LVCMOS swings.
- Also use a GSGSG pinout in connectors (Board to Board or ZIF).
- DES device - follow similar guidelines.
- Bypass the device with MLC surface mount devices and thinly separated power and ground planes with low inductance feeds.
- High current returns should have a separate path with a width proportional to the amount of current carried to minimize any resulting IR effects.

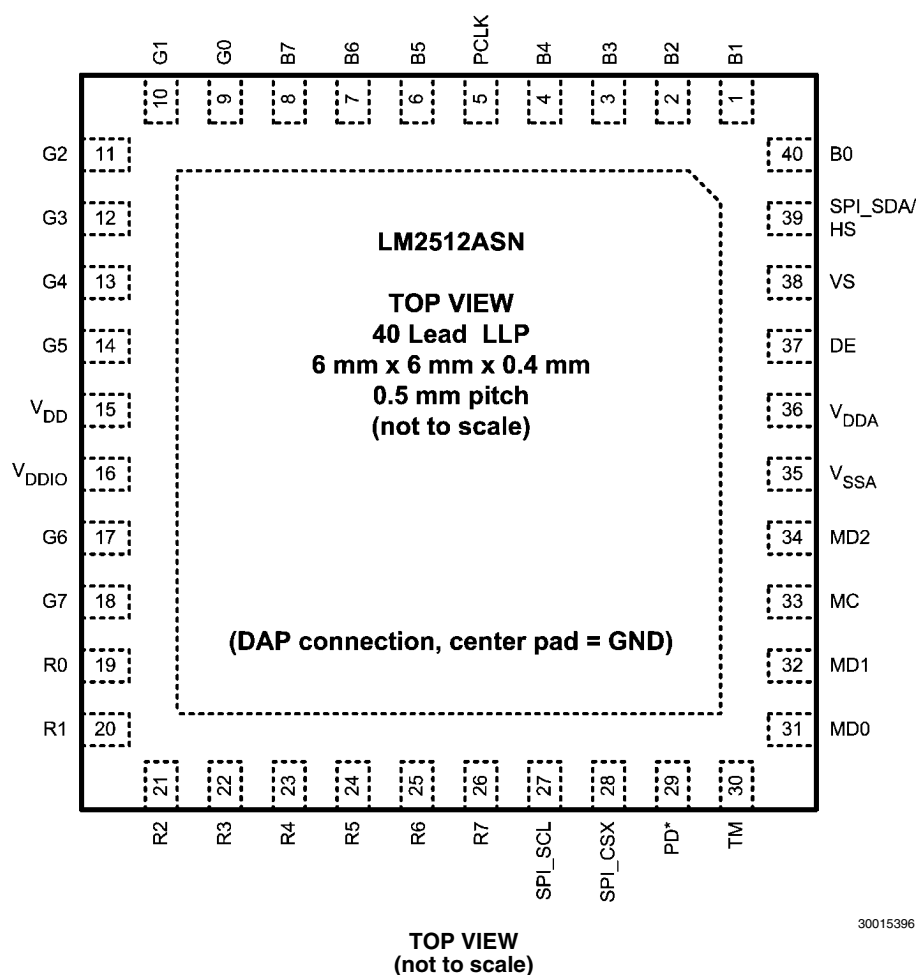
Connection Diagram 49 UFBGA
Package



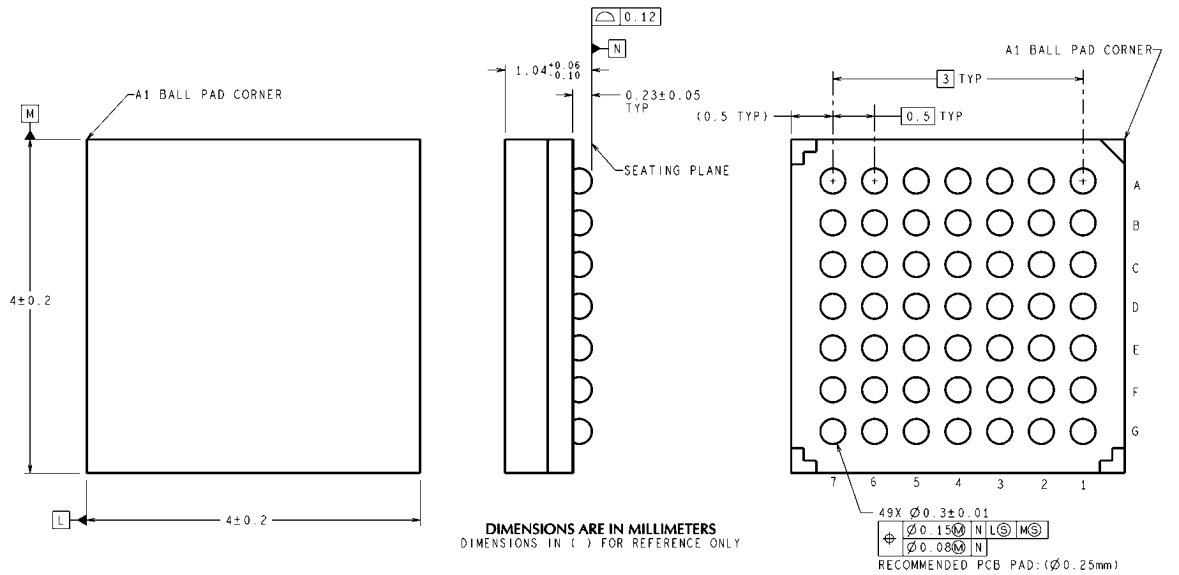
RGB SER Pinout

SER	1	2	3	4	5	6	7
A	B1	SPI_SDA/HS	RES1	NC	MD2	MD1	MD0
B	B2	B0	VS	V _{DDA}	MC	TM	PD*
C	PCLK	B3	DE	V _{SSA}	SPI_CSX	SPI_SCL	R7
D	V _{SSIO}	V _{DDIO}	B4	V _{SSIO}	V _{SSIO}	V _{DDIO}	R6
E	B6	B7	G5	B5	R1	R4	R5
F	G0	G1	G4	V _{DD}	G6	R0	R3
G	G2	G3	V _{SS}	V _{SSIO}	V _{DDIO}	G7	R2

Connection Diagram 40 LLP Package

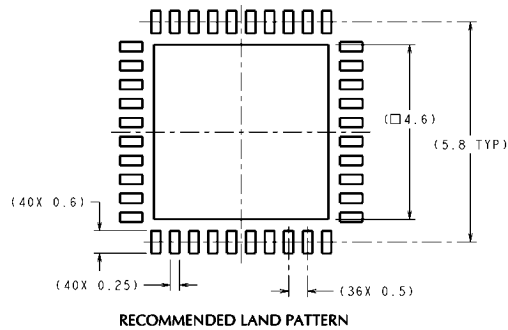


Physical Dimensions inches (millimeters) unless otherwise noted

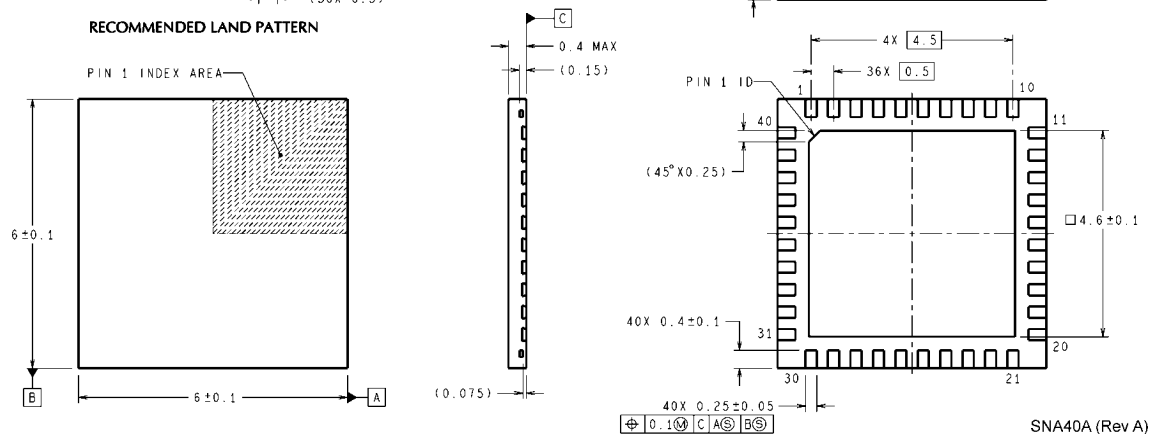


SLH49A (Rev D)

49L UFBGA, 0.5mm pitch
Order Number LM2512ASM
NS Package Number SLH49A



40L LLP, 0.5mm pitch
Order Number LM2512ASN
NS Package Number SNA40A



SNA40A (Rev A)

40L LLP, 0.5mm pitch
Order Number LM2512ASN
NS Package Number SNA40A

Notes

Notes

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