

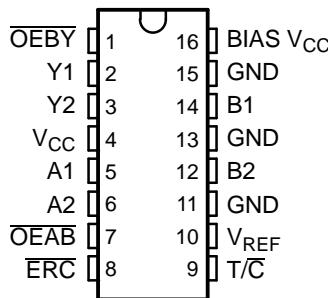
FEATURES

- TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels
- Split LVTTL Port Provides a Feedback Path for Control and Diagnostics Monitoring
- LVTTL Interfaces Are 5-V Tolerant
- High-Drive GTLP Outputs (100 mA)
- LVTTL Outputs (–24 mA/24 mA)
- Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal

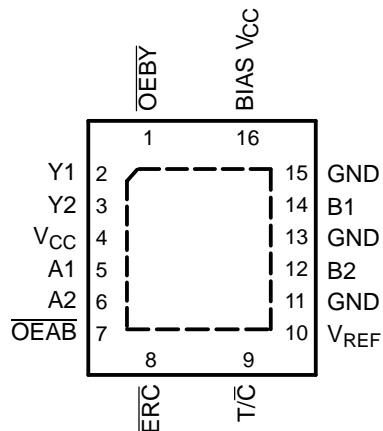
Data-Transfer Rate and Signal Integrity in Distributed Loads

- I_{off} , Power-Up 3-State, and BIAS V_{CC} Support Live Insertion
- Polarity Control Selects True or Complementary Outputs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

D, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74GTL1394RGYR
	SOIC – D	Tube	SN74GTL1394D
		Tape and reel	GTLP1394
	TSSOP – PW	Tape and reel	SN74GTL1394PWR
	TVSOP – DGV	Tape and reel	GP394

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TI-OPC, OEC, TI are trademarks of Texas Instruments.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74GTL1394 is a high-drive, 2-bit, 3-wire bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent and inverted transparent modes of data transfer with separate LVTTL input and LVTTL output pins, which provides a feedback path for control and diagnostics monitoring. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels, and is especially designed to work with the Texas Instruments (TI™) 1394 backplane physical-layer controllers. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuitry minimizes bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to $11\ \Omega$.

GTLP is the TI derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTL1394 is given only at the preferred higher noise margin GTLP, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2\text{ V}$ and $V_{REF} = 0.8\text{ V}$) or GTLP ($V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off} , power-up 3-state, and BIAS V_{CC} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (\overline{ERC}). Changing the \overline{ERC} input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTIONAL DESCRIPTION

The output-enable (\overline{OEAB}) input controls the activity of the B port. When \overline{OEAB} is low, the B-port outputs are active. When \overline{OEAB} is high, the B-port outputs are disabled.

Separate LVTTL input and output pins provide a feedback path for control and diagnostics monitoring. The \overline{OEBY} input controls the Y outputs. When \overline{OEBY} is low, the Y outputs are active. When \overline{OEBY} is high, the Y outputs are disabled.

The polarity-control (T/\overline{C}) input is provided to select polarity of data transmission in both directions. When T/\overline{C} is high, data transmission is true, and A data goes to the B bus and B data goes to the Y bus. When T/\overline{C} is low, data transmission is complementary, and inverted A data goes to the B bus and inverted B data goes to the Y bus.

FUNCTION TABLES

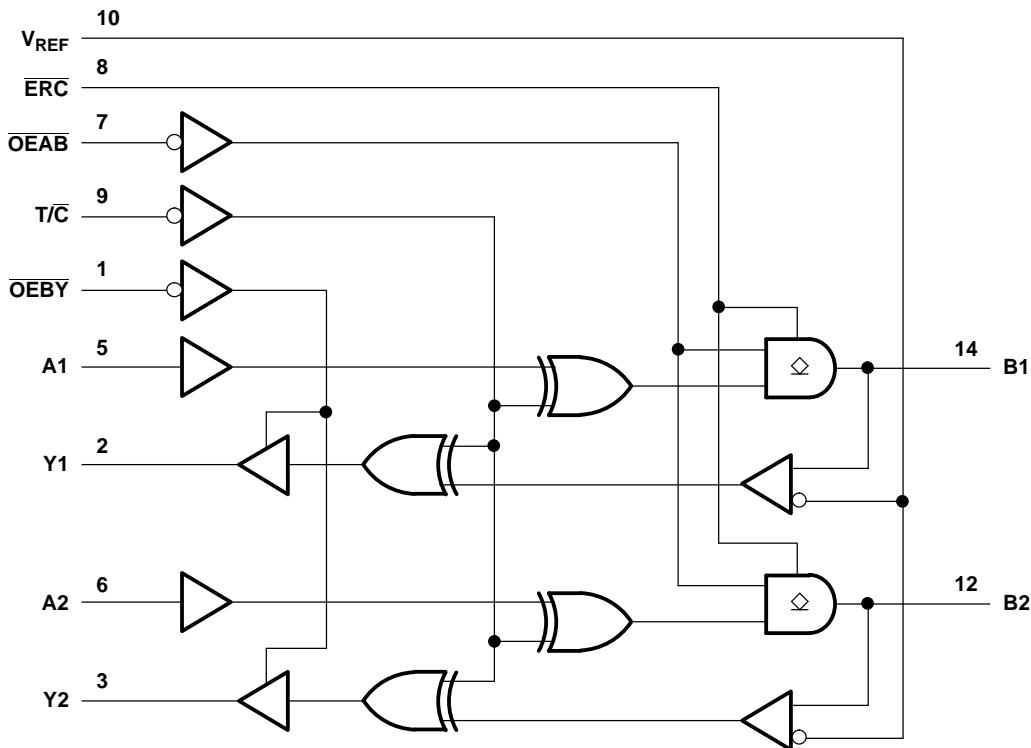
OUTPUT CONTROL

INPUTS			OUTPUT	MODE	
T/C	OEAB	OEBY			
X	H	H	Z		
H	L	H	A data to B bus		
H	H	L	B data to Y bus		
H	L	L	A data to B bus, B data to Y bus		
L	L	H	Inverted A data to B bus		
L	H	L	Inverted B data to Y bus		
L	L	L	Inverted A data to B bus, Inverted B data to Y bus		

OUTPUT EDGE-RATE CONTROL (ERC)

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V _{CC}	Fast

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	A inputs, \overline{ERC} , and control inputs	-0.5	7	V
		B port and V_{REF}	-0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	Y outputs	-0.5	7	V
		B port	-0.5	4.6	
I_O	Current into any output in the low state	Y outputs		48	mA
		B port		200	
I_O	Current into any output in the high state ⁽³⁾			48	mA
	Continuous current through each V_{CC} or GND			± 100	mA
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
θ_{JA}	Package thermal impedance	D package ⁽⁴⁾		73	°C/W
		DGV package ⁽⁴⁾		120	
		PW package ⁽⁴⁾		108	
		RGY package ⁽⁵⁾		39	
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.

(4) The package thermal impedance is calculated in accordance with JEDEC 51-7.

(5) The package thermal impedance is calculated in accordance with JEDEC 51-5.

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

			MIN	NOM	MAX	UNIT	
V_{CC} , BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V	
		GTLP	1.35	1.5	1.65		
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V	
		GTLP	0.87	1	1.1		
V_I	Input voltage	B port			V_{TT}	V	
		Except B port		V_{CC}	5.5		
V_{IH}	High-level input voltage	B port	$V_{REF} + 0.05$			V	
		ERC	$V_{CC} - 0.6$	V_{CC}	5.5		
		Except B port and ERC	2				
V_{IL}	Low-level input voltage	B port	$V_{REF} - 0.05$			V	
		ERC	GND				
		Except B port and ERC	0.8				
I_{IK}	Input clamp current		-18			mA	
I_{OH}	High-level output current	Y outputs	-24			mA	
I_{OL}	Low-level output current	Y outputs	24			mA	
		B port	100				
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	10			ns/V	
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			μs/V	
T_A	Operating free-air temperature		-40			°C	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS $V_{CC} = 3.3$ V first, I/O second, and $V_{CC} = 3.3$ V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
- (3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
- (4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} . TI-OPC circuitry is enabled in the A-to-B direction and is activated when $V_{TT} > 0.7$ V above V_{REF} . If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3.15 \text{ V}$, $I_I = -18 \text{ mA}$				-1.2	V
V_{OH}	Y outputs	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$, $I_{OH} = -100 \mu\text{A}$		$V_{CC} - 0.2$			V
		$V_{CC} = 3.15 \text{ V}$		$I_{OH} = -12 \text{ mA}$	2.4		
				$I_{OH} = -24 \text{ mA}$	2		
V_{OL}	Y outputs	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$, $I_{OL} = 100 \mu\text{A}$			0.2		V
		$V_{CC} = 3.15 \text{ V}$		$I_{OL} = 12 \text{ mA}$	0.4		
				$I_{OL} = 24 \text{ mA}$	0.5		
	B port	$V_{CC} = 3.15 \text{ V}$		$I_{OL} = 10 \text{ mA}$	0.2		
				$I_{OL} = 64 \text{ mA}$	0.4		
				$I_{OL} = 100 \text{ mA}$	0.55		
I_I	A-port and control inputs	$V_{CC} = 3.45 \text{ V}$, $V_I = 0 \text{ to } 5.5 \text{ V}$				± 10	μA
$I_{OZH}^{(2)}$	Y outputs	$V_{CC} = 3.45 \text{ V}$		$V_O = V_{CC}$		10	μA
	B port			$V_O = 1.5 \text{ V}$		10	
$I_{OZL}^{(2)}$	Y outputs and B port	$V_{CC} = 3.45 \text{ V}$, $V_O = \text{GND}$				-10	μA
I_{CC}	Y outputs and B port	$V_{CC} = 3.45 \text{ V}$, $I_O = 0$, V_I (A-port or control inputs) = V_{CC} or GND, V_I (B port) = V_{TT} or GND		Outputs high		20	mA
				Outputs low		20	
				Outputs disabled		20	
$\Delta I_{CC}^{(3)}$		$V_{CC} = 3.45 \text{ V}$, One A-port or control input at $V_{CC} - 0.6 \text{ V}$, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	A-port inputs	$V_I = 3.15 \text{ V or } 0$			3.5	4.5	pF
	Control inputs				4	5	
C_o	Y outputs	$V_O = 3.15 \text{ V or } 0$			4.5	5	pF
C_{io}	B port	$V_O = 1.5 \text{ V or } 0$			9	10.5	pF

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.(2) For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.(3) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.**Hot-Insertion Specifications for A Inputs and Y Outputs**

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{off}		$V_{CC} = 0$,	BIAS $V_{CC} = 0$,	V_I or $V_O = 0 \text{ to } 5.5 \text{ V}$	10	μA
I_{OZPU}		$V_{CC} = 0 \text{ to } 1.5 \text{ V}$,	$V_O = 0.5 \text{ V to } 3 \text{ V}$,	$\overline{OE} = 0$	± 30	μA
I_{OZPD}		$V_{CC} = 1.5 \text{ V to } 0$,	$V_O = 0.5 \text{ V to } 3 \text{ V}$,	$\overline{OE} = 0$	± 30	μA

Live-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
I_{off}		$V_{CC} = 0$,	BIAS $V_{CC} = 0$,	V_I or $V_O = 0 \text{ to } 1.5 \text{ V}$	10	μA
I_{OZPU}		$V_{CC} = 0 \text{ to } 1.5 \text{ V}$,	BIAS $V_{CC} = 0$,	$V_O = 0.5 \text{ V to } 1.5 \text{ V}$, $\overline{OE} = 0$	± 30	μA
I_{OZPD}		$V_{CC} = 1.5 \text{ V to } 0$,	BIAS $V_{CC} = 0$,	$V_O = 0.5 \text{ V to } 1.5 \text{ V}$, $\overline{OE} = 0$	± 30	μA
I_{CC} (BIAS V_{CC})	$V_{CC} = 0 \text{ to } 3.15 \text{ V}$	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$,	V_O (B port) = 0 to 1.5 V		5	mA
	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$				10	μA
V_O	$V_{CC} = 0$,	BIAS $V_{CC} = 3.3 \text{ V}$,	$I_O = 0$	0.95	1.05	V
I_O	$V_{CC} = 0$,	BIAS $V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$,	V_O (B port) = 0.6 V	-1		μA

Switching Characteristics

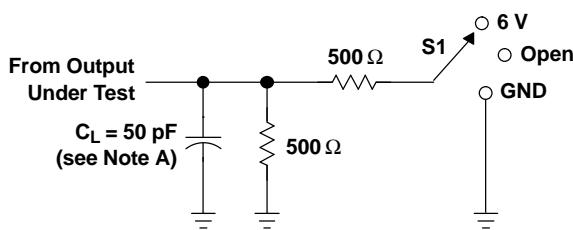
over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT	
t_{PLH}	A	B	Slow	3.3	5.9	ns		
t_{PHL}				3	6.6			
t_{PLH}	A	B	Fast	2.5	5.2	ns		
t_{PHL}				1.9	4.8			
t_{PLH}	A	Y	Slow	5.4	9	ns		
t_{PHL}				4.9	8.6			
t_{PLH}	A	Y	Fast	4.3	7.9	ns		
t_{PHL}				3.9	7.5			
t_{PLH}	T/C	B	Slow	3	6.5	ns		
t_{PHL}				3.1	6.6			
t_{PLH}	T/C	B	Fast	2.3	5.6	ns		
t_{PHL}				1.7	4.9			
t_{en}	OEAB	B	Slow	3.2	6.2	ns		
t_{dis}				3.2	6.4			
t_{en}	OEAB	B	Fast	1.9	5.3	ns		
t_{dis}				2.4	5.7			
t_r	Rise time, B outputs (20% to 80%)			Slow	2.7	ns		
				Fast	1.5			
t_f	Fall time, B outputs (80% to 20%)			Slow	3.2	ns		
				Fast	2.1			
t_{PLH}	B	Y		1.6	4.6	ns		
t_{PHL}				1.4	3.9			
t_{PLH}	T/C	Y		1	4.5	ns		
t_{PHL}				1.2	4.1			
t_{en}	OEBY	Y		1	4.1	ns		
t_{dis}				1.3	4.6			

(1) Slow ($\overline{ERC} = GND$) and Fast ($\overline{ERC} = V_{CC}$)

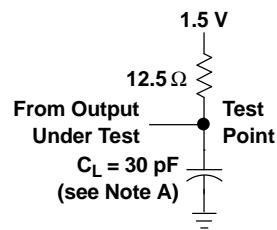
(2) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$.

PARAMETER MEASUREMENT INFORMATION

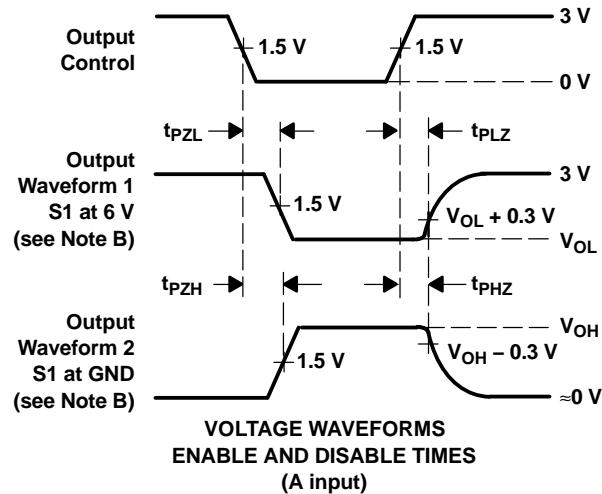
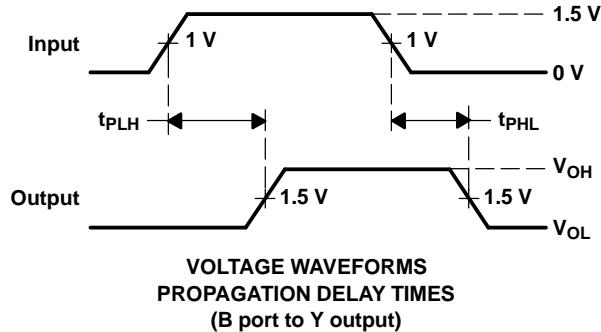
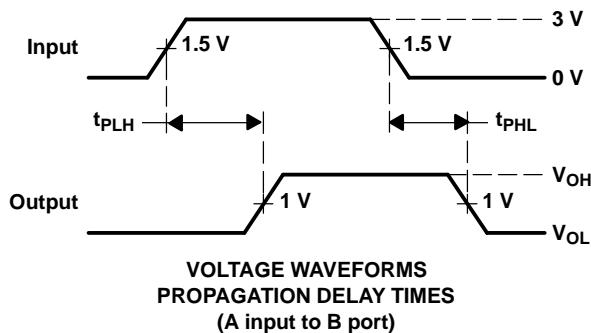


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT FOR Y OUTPUTS



LOAD CIRCUIT FOR B OUTPUTS



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50 \Omega$, $t_r \approx 2$ ns, $t_f \approx 2$ ns.
- The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

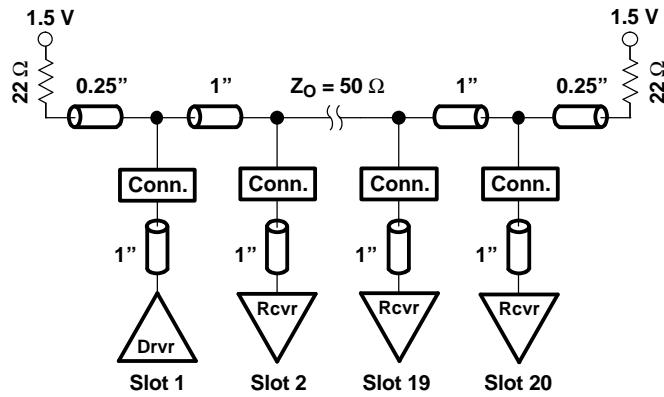


Figure 2. High-Drive Test Backplane

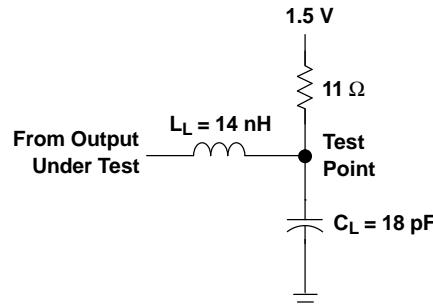


Figure 3. High-Drive RLC Network

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE ⁽¹⁾	TYP ⁽²⁾	UNIT	
t_{PLH}	A	B	Slow	4.2	ns	
t_{PHL}				4.2		
t_{PLH}	A	B	Fast	3.6	ns	
t_{PHL}				3.6		
t_{PLH}	A	Y	Slow	5.8	ns	
t_{PHL}				5.8		
t_{PLH}	A	Y	Fast	5.2	ns	
t_{PHL}				5.2		
t_{PLH}	T/C	B	Slow	4.4	ns	
t_{PHL}				4.4		
t_{PLH}	T/C	B	Fast	3.8	ns	
t_{PHL}				3.8		
t_{en}	\overline{OEAB}	\overline{B}	Slow	4.2	ns	
t_{dis}				4.3		
t_{en}	\overline{OEAB}	\overline{B}	Fast	3.6	ns	
t_{dis}				3.3		
t_r	Rise time, B outputs (20% to 80%)		Slow	2	ns	
			Fast	1.2		
t_f	Fall time, B outputs (80% to 20%)		Slow	2.5	ns	
			Fast	1.8		

(1) Slow ($\overline{ERC} = GND$) and Fast ($\overline{ERC} = V_{CC}$)

(2) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ C$. All values are derived from TI-SPICE models.

APPLICATION INFORMATION

Operational Description

The GTLP1394 is designed specifically for use with the TI 1394 backplane layer controller family to transmit the 1394 backplane serial bus across parallel backplanes. But, it is a versatile 2-bit device that also is being used to provide multiple single-bit clocks or an ATM read and write clock in multislot parallel backplane applications.

The 1394-1995 is an IEEE designation for a high-performance serial bus. This serial bus defines both a backplane (e.g., GTLP, VME, FB+, CPCI, etc.) physical layer and a point-to-point cable-connected virtual bus. The backplane version operates at 25, 50, or 100 Mbps, whereas the cable version supports data rates of 100, 200, and 400 Mbps. Both versions are compatible at the link layer and above. The interface standard defines the transmission method, media in the cable version, and protocol. The primary application of the cable version is the interconnection of digital A/V equipment and integration of I/O connectivity at the back panel of personal computers using a low-cost, scalable, high-speed serial interface. The primary application of the backplane version is to provide a robust control interface to each daughter card. The 1394 standard also provides new services, such as real-time I/O and live connect/disconnect capability for external devices.

Electrical

The 1394 standard is a transaction-based packet technology for cable- or backplane-based environments. Both chassis and peripheral devices can use this technology. The 1394 serial bus is organized as if it were memory space interconnected between devices, or as if devices resided in slots on the main backplane. Device addressing is 64 bits wide, partitioned as ten bits for bus ID, six bits for node ID, and 48 bits for memory addresses. The result is the capability to address up to 1023 buses, with each having up to 63 nodes, each with 281 terabytes of memory. Memory-based addressing, rather than channel addressing, views resources as registers or memory that can be accessed with processor-to-memory transactions. Each bus entity is termed a unit, to be individually addressed, reset, and identified. Multiple nodes can reside physically in a single module, and multiple ports can reside in a single node.

Some key features of the 1394 topology are multimaster capabilities, live connect/disconnect (hot plugging) capability, genderless cabling connectors on interconnect cabling, and dynamic node address allocation as nodes are added to the bus. A maximum of 63 nodes can be connected to one network.

The cable-based physical interface uses dc-level line states for signaling during initialization and arbitration. Both environments use dominant mode addresses for arbitration. The backplane environment does not have the initialization requirements of the cable environment because it is a physical bus and does not contain repeaters. Due to the differences, a backplane-to-cable bridge is required to connect these two environments.

The signals transmitted on both the cable and backplane environments are NRZ with data-strobe (DS) encoding. DS encoding allows only one of the two signal lines to change each data bit-period, essentially doubling the jitter tolerance, with very little additional circuitry overhead in the hardware.

APPLICATION INFORMATION

Protocol

Both asynchronous and isochronous data transfers are supported. The asynchronous format transfers data and transaction-layer information to an explicit address. The isochronous format broadcasts data based on channel numbers, rather than specific addressing. Isochronous packets are issued on the average of each 125 μ s in support of time-sensitive applications. Providing both asynchronous and isochronous formats on the same interface allows both non-real-time and real-time critical applications on the same bus. The cable environment's tree topology is resolved during a sequence of events, triggered each time a new node is added or removed from the network. This sequence starts with a bus reset phase, where previous information about a topology is cleared. The tree ID sequence determines the actual tree structure, and a root node is dynamically assigned, or it is possible to force a particular node to become the root. After the tree is formed, a self-ID phase allows each node on the network to identify itself to all other nodes. During the self-ID process, each node is assigned an address. After all the information has been gathered on each node, the bus goes into an idle state, waiting for the beginning of the standard arbitration process.

The backplane physical layer shares some commonality with the cable physical layer. Common functions include: bus state determination, bus access protocols, encoding and decoding functions, and synchronization of received data to a local clock.

Backplane Features

- 25-, 50-, and 100-Mbps data rates for backplane environments
- Live connection/disconnection possible without data loss or interruption.
- Configuration ROM and status registers supporting plug and play
- Multidrop or point-to-point topologies supported.
- Specified bandwidth assignments for real-time applications

Applicability and Typical Application for IEEE Std 1394 Backplane

The 1394 backplane serial bus (BPSB) plays a supportive role in backplane systems, specifically GTLP, FutureBus+, VME64, and proprietary backplane bus systems. This supportive role can be grouped into three categories:

- Diagnostics
 - Alternate control path to the parallel backplane bus
 - Test, maintenance, and troubleshooting
 - Software debug and support interface
- System enhancement
 - Fault tolerance
 - Live insertion
 - CSR access
 - Auxiliary 2-bit bus with a 64-bit address space to the parallel backplane bus
- Peripheral monitoring
 - Monitoring of peripherals (disk drives, fans, power supplies, etc.) in conjunction with another externally wired monitor bus, such as defined by the Intelligent Platform Management Interface (IPMI)

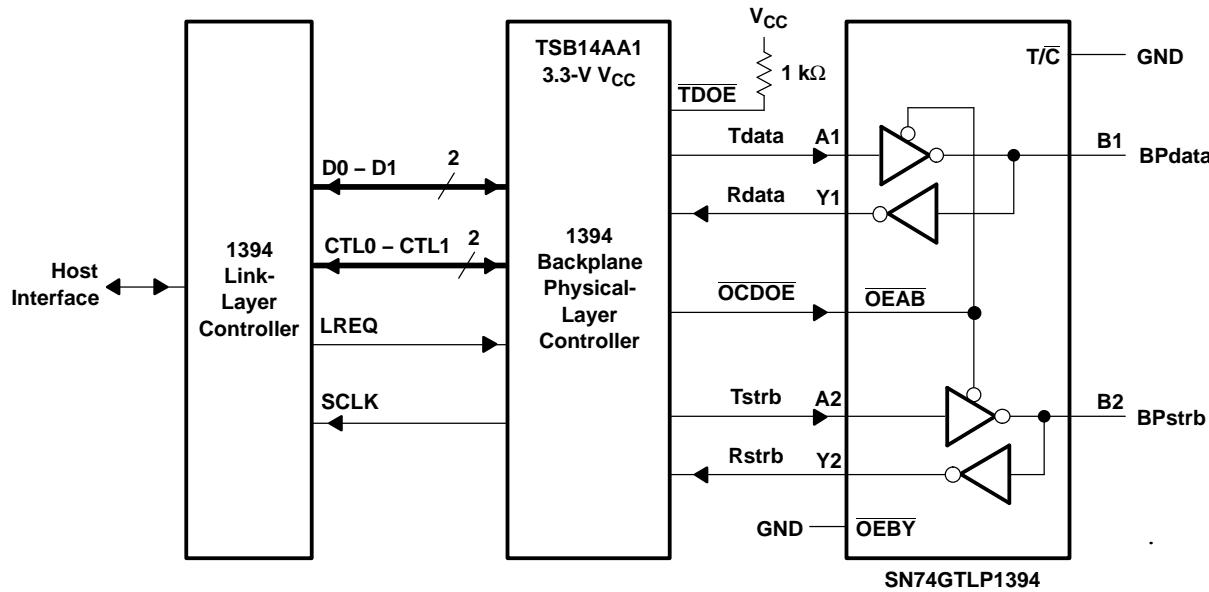
The 1394 backplane physical layer (PHY) and the SN74GTLPI394 provide a cost-effective way to add high-speed 1394 connections to every daughter card in almost any backplane. More information on the backplane physical layer devices and how to implement the 1394 standard in backplane and cable applications can be found at www.ti.com/sc/1394.

APPLICATION INFORMATION

SN74GTL1394 Interface With the TSB14AA1 1394 Backplane PHY

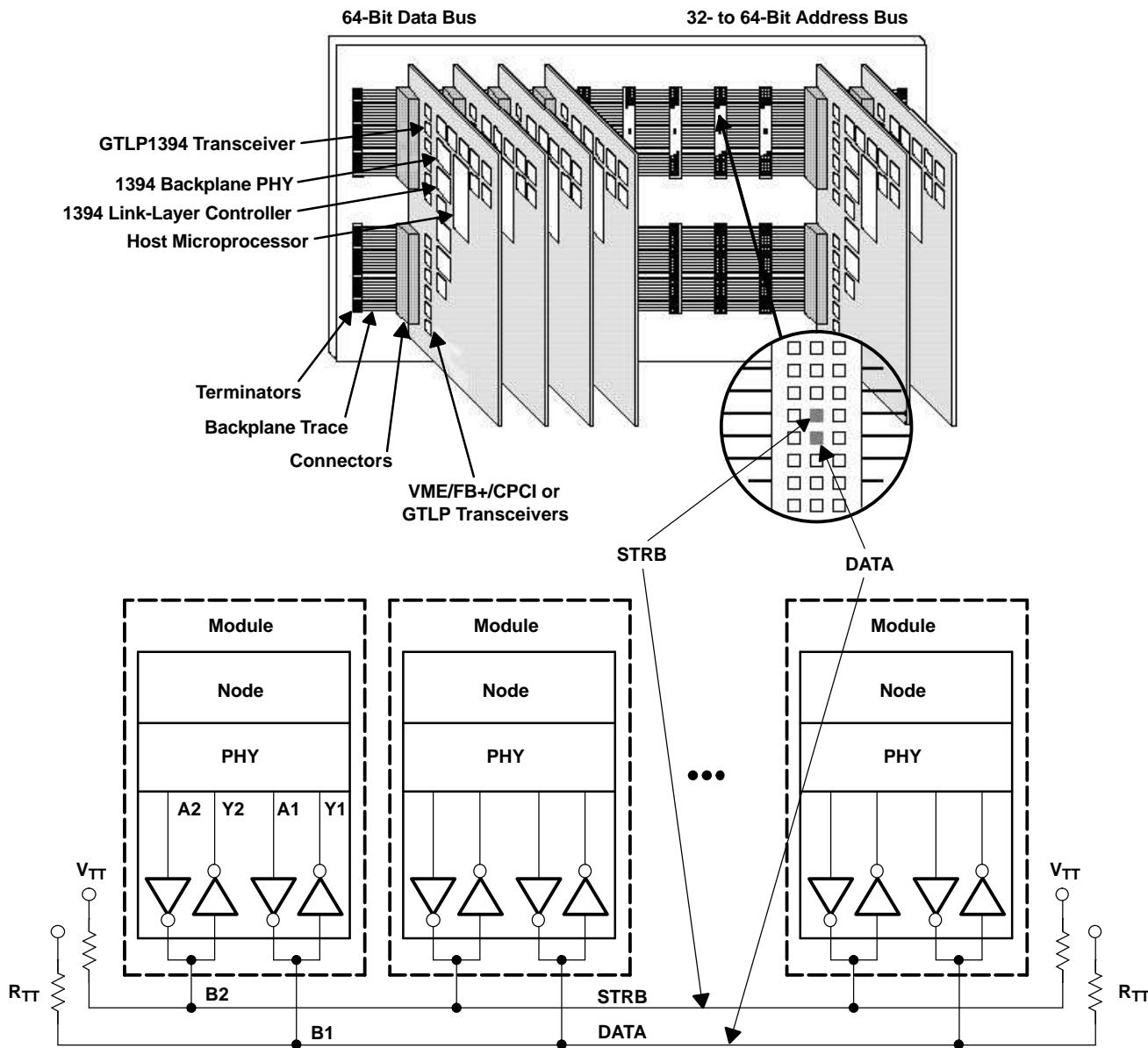
- A1, B1, and Y1 are used for the PHY data signals.
- A2, B2, and Y2 are used for the PHY strobe signals.
- PHY N_OEB_D or \overline{OCDOE} connects to \overline{OEAB} , which controls the PHY transmit signals.
- \overline{OEY} is connected to GND, since the transceiver always must be able to receive signals from the backplane and relay them to the PHY.
- T/\overline{C} is connected to GND for inverted signals.
- V_{CC} is nominal 3.3 V.
- BIAS V_{CC} is connected to nominal 3.3 V to support live insertion.
- V_{REF} normally is 2/3 of V_{TT} .
- \overline{ERC} normally is connected to GND for slow edge-rate operation because frequencies of only 50 MHz (S100) and 25 MHz (S50) are required.

LOGICAL REPRESENTATION



APPLICATION INFORMATION

PHYSICAL REPRESENTATION



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74GTL1394DGVR4	ACTIVE	TVSOP	DGV	16		TBD	Call TI	Call TI	-40 to 85	GP394	Samples
74GTL1394DGVRG4	ACTIVE	TVSOP	DGV	16		TBD	Call TI	Call TI	-40 to 85	GP394	Samples
SN74GTL1394D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLP1394	Samples
SN74GTL1394DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLP1394	Samples
SN74GTL1394DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLP1394	Samples
SN74GTL1394DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLP1394	Samples
SN74GTL1394DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLP1394	Samples
SN74GTL1394DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GTLP1394	Samples
SN74GTL1394PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GP394	Samples
SN74GTL1394PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GP394	Samples
SN74GTL1394PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GP394	Samples
SN74GTL1394PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GP394	Samples
SN74GTL1394PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GP394	Samples
SN74GTL1394PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	GP394	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

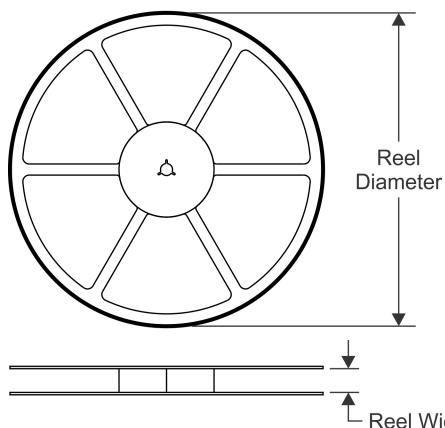
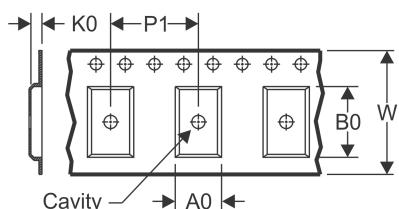
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

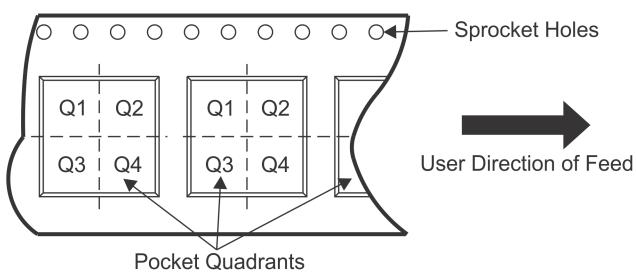
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

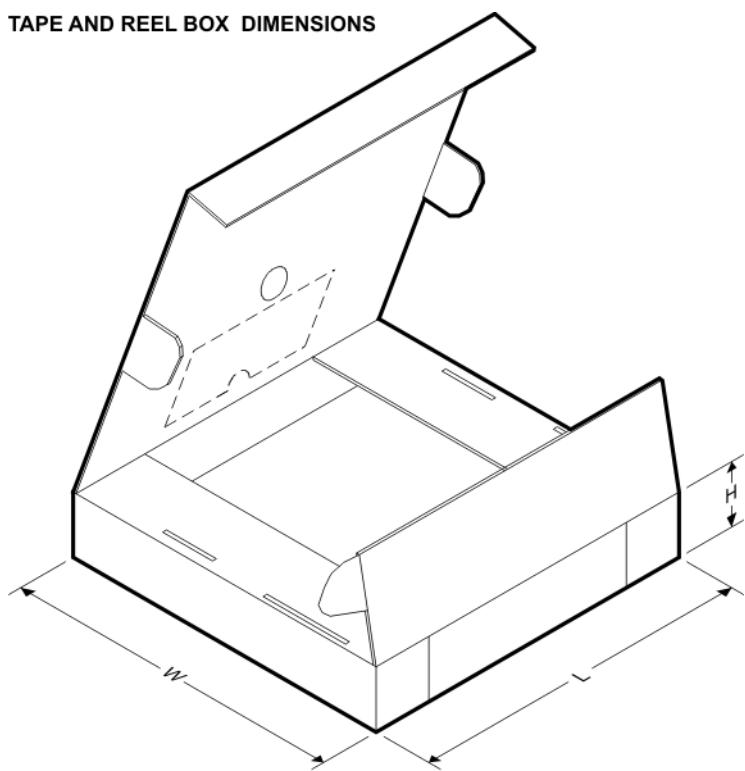
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL1394DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74GTL1394PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


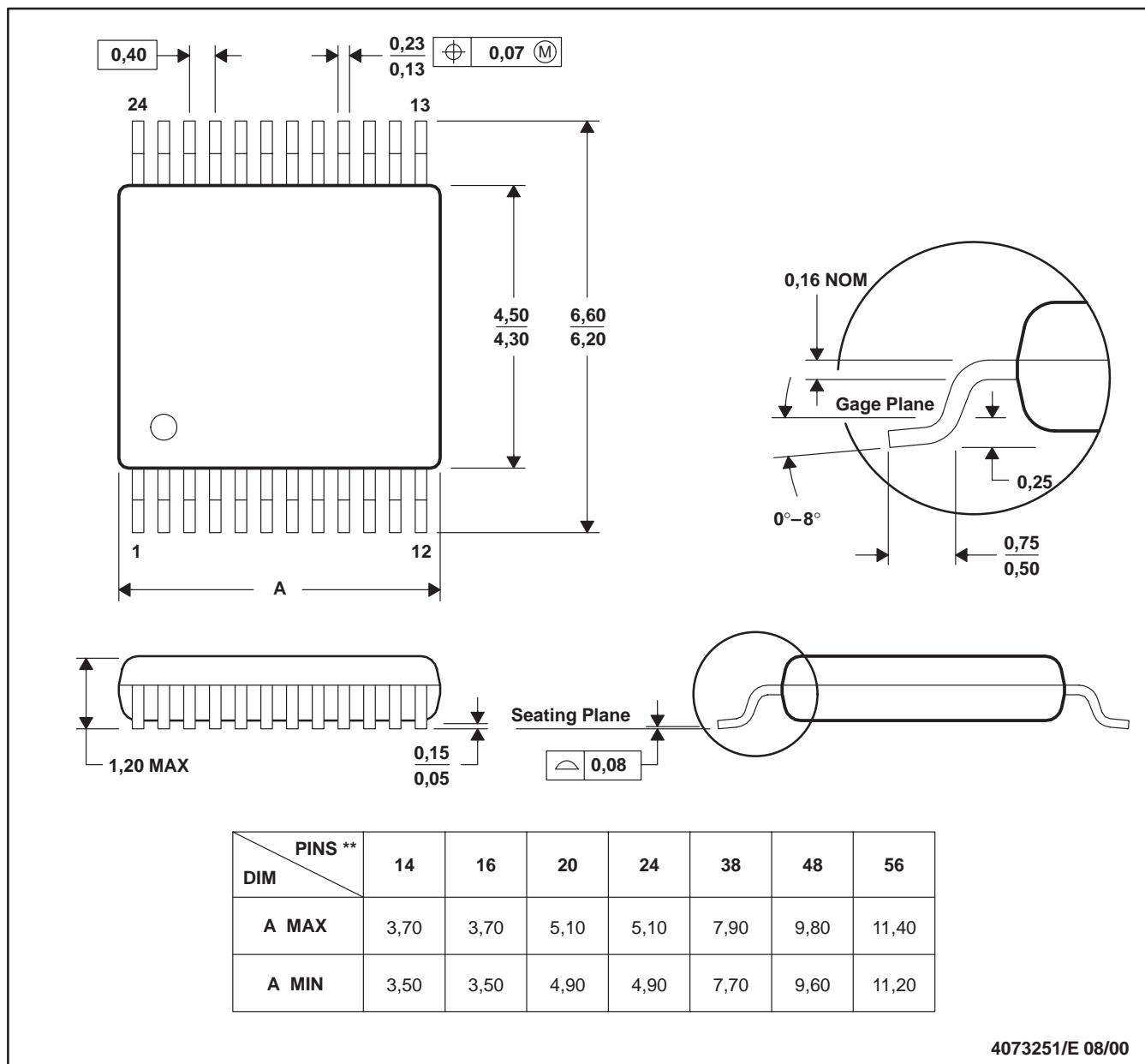
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL1394DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74GTL1394PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

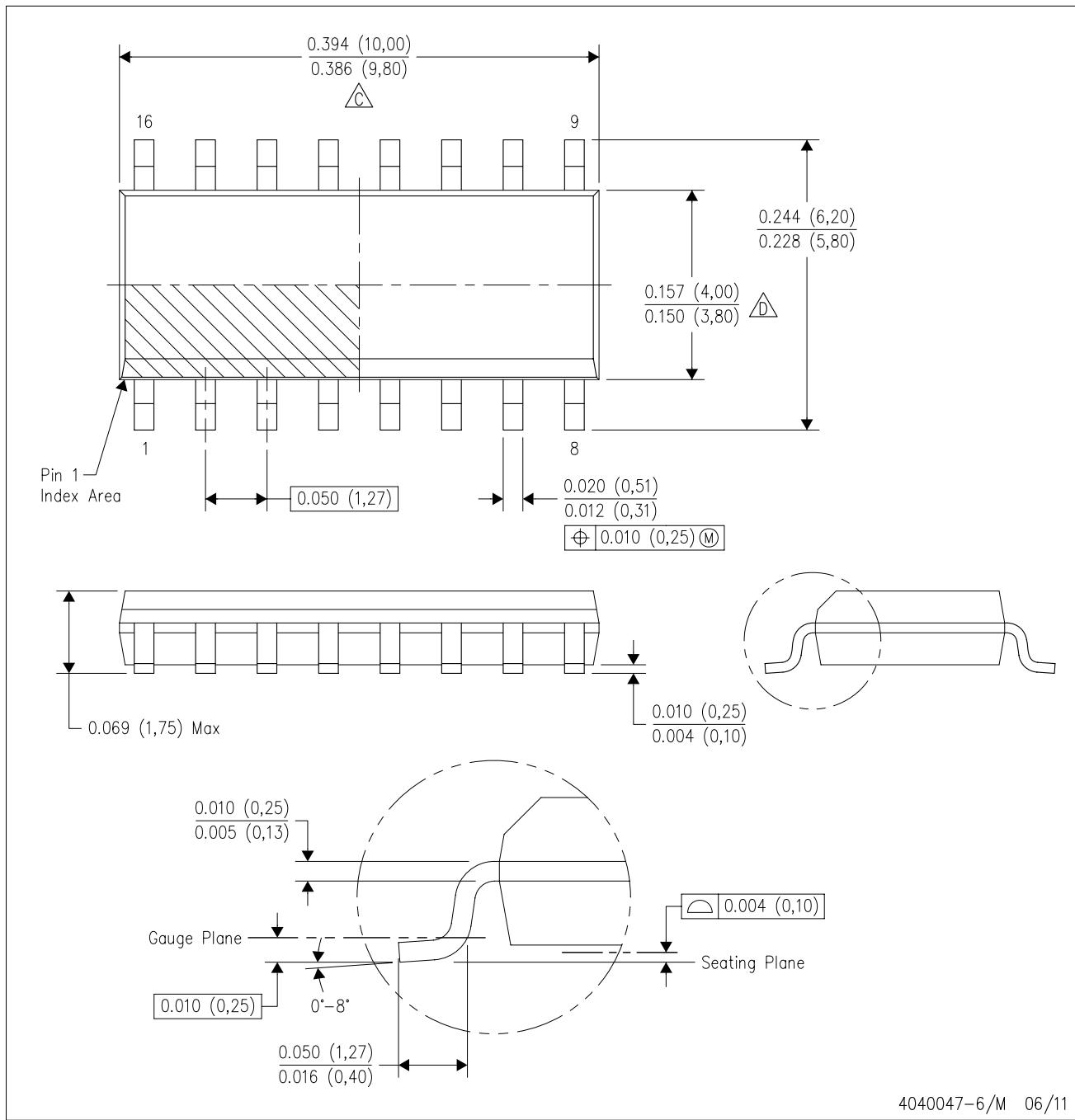
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

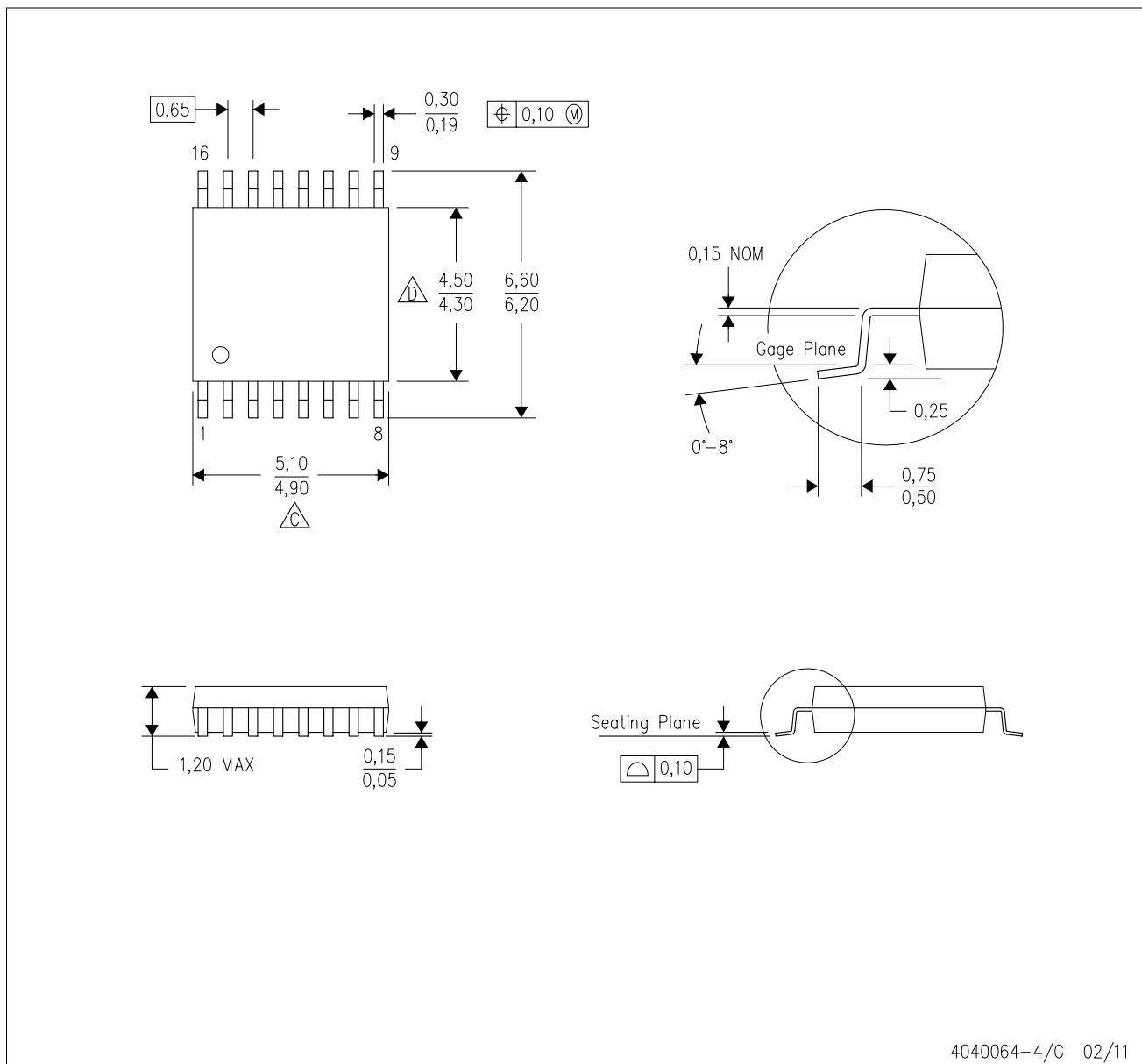
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

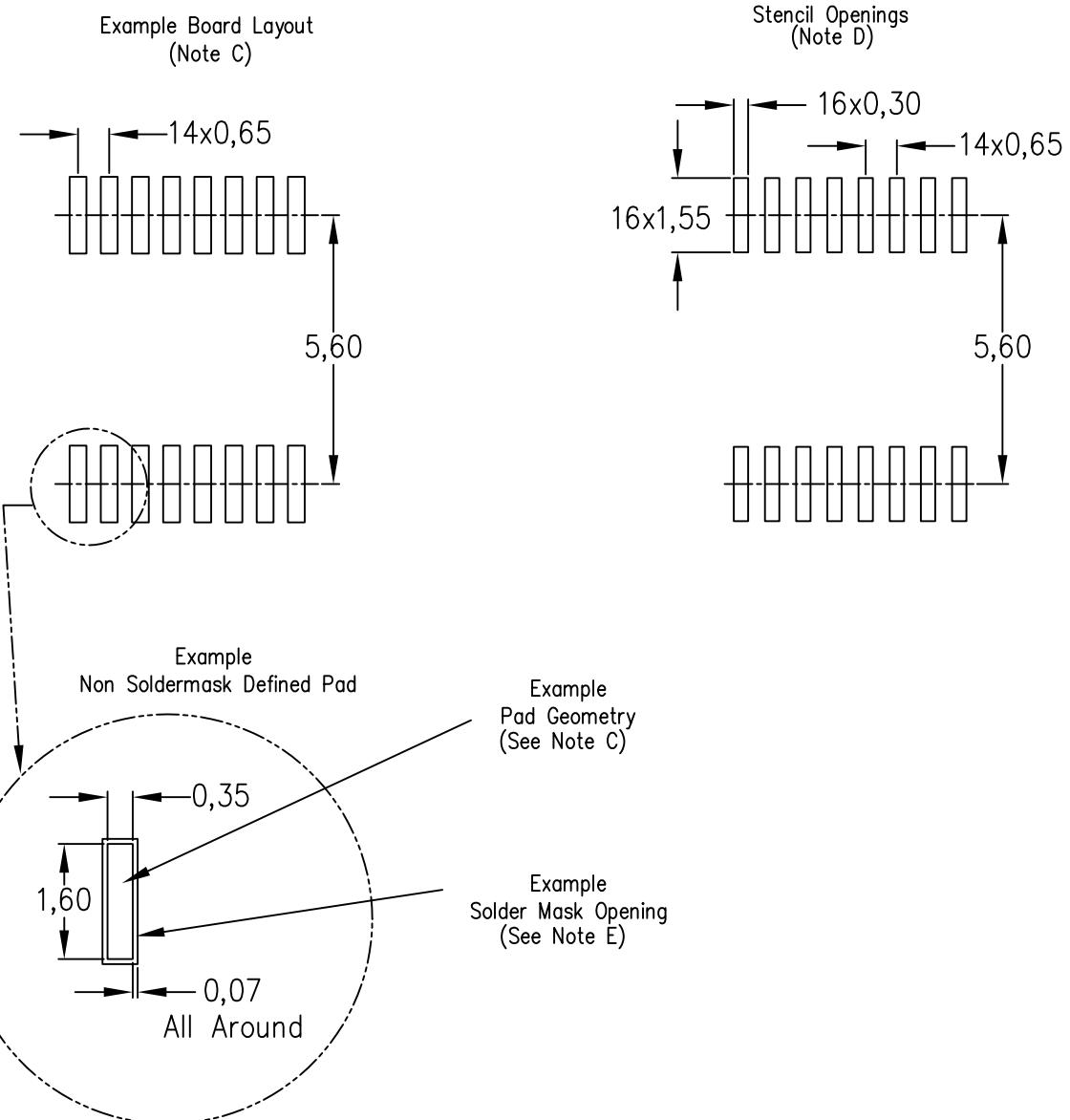
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

4040064-4/G 02/11

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity
	TI E2E Community
	e2e.ti.com