

74LV541AT

Octal buffer/line driver; 3-state

Rev. 4 — 4 July 2024

Product data sheet

1. General description

The 74LV541AT is an 8-bit buffer/line driver with 3-state outputs and TTL inputs. The device features two output enables ($\overline{OE}1$ and $\overline{OE}2$). A HIGH on $\overline{OE}n$ causes the associated outputs to assume a high-impedance OFF-state.

Designed to operate over a V_{CC} range from 4.5 V to 5.5 V, the inputs are TTL compatible, which allows the device to be used to translate from 3.3 V to 5 V.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial Power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

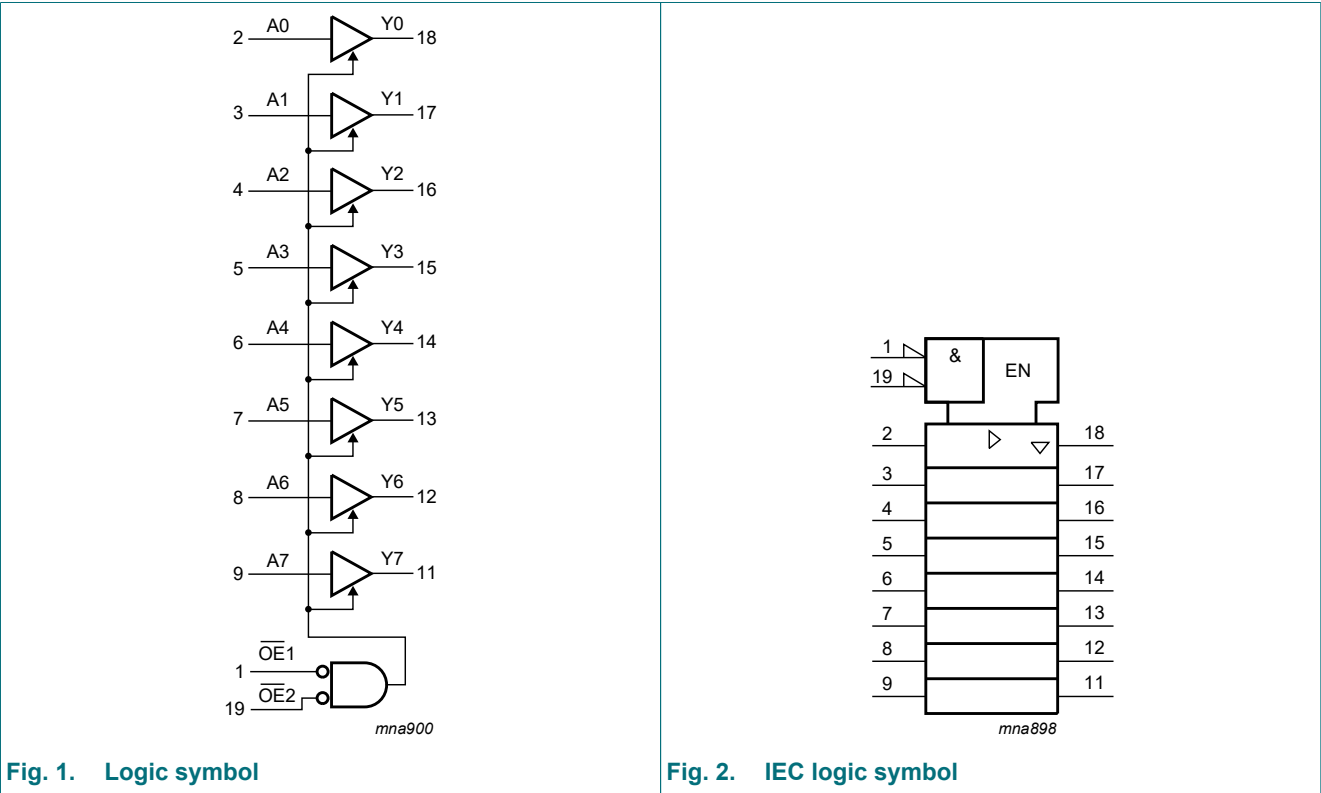
- Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical t_{pd} of 2.8 ns at 5 V
- Typical $V_{OL(p)} < 0.8$ V at $V_{CC} = 5$ V, $T_{amb} = 25$ °C
- Typical $V_{OH(v)} > 2.3$ V at $V_{CC} = 5$ V, $T_{amb} = 25$ °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 3000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

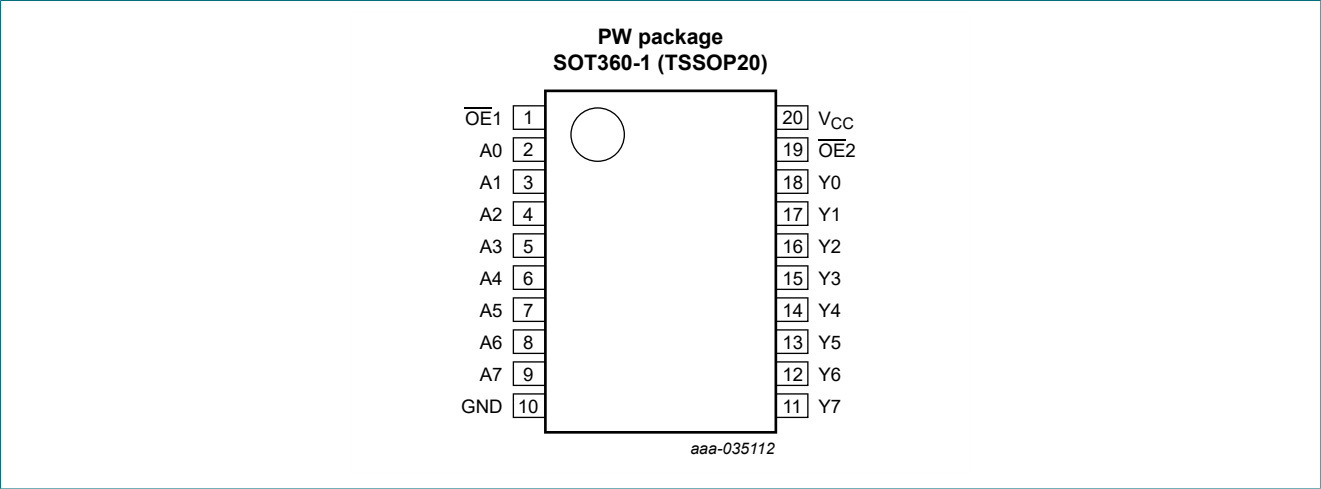
Type number	Package			
	Temperature range	Name	Description	Version
74LV541ATPW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
OE1	1	output enable input (active LOW)
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	18, 17, 16, 15, 14, 13, 12, 11	data output
OE2	19	output enable input (active LOW)
VCC	20	supply voltage

6. Functional description

Table 3. Functional table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control		Input	Output
OE1	OE2	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	active mode [2][3]	-0.5	V _{CC} + 0.5	V
		power-down or 3-state mode [2]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-20	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±35	mA
I _{CC}	supply current		-	70	mA
I _{GND}	ground current		-70	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [4]	-	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] This value is limited to 7.0 V maximum.
[4] For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		4.5	5.5	V
V _I	input voltage		0	5.5	V
V _O	output voltage	active mode	0	V _{CC}	V
		power-down or 3-state mode	0	5.5	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 5.0 V ± 0.5 V	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2	-	-	2	-	2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -16 mA	3.94	-	-	3.8	-	3.8	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 16mA	-	-	0.44	-	0.55	-	0.55	V
I _{OZ}	OFF-state output current	V _{CC} = 5.5 V; V _I = V _{IH} or V _{IL} ; V _O = GND to 5.5 V	-	-	±0.25	-	±2.5	-	±2.5	µA
I _{OFF}	power-off leakage current	V _I or V _O = GND to 5.5 V; V _{CC} = 0 V	-	-	0.5	-	5	-	5	µA
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2	-	20	-	20	µA
ΔI _{CC}	additional supply current	per input pin; V _I = 3.4 V; I _O = 0 A; other pins at V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$. For test circuit see Fig. 5.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	An to Yn; see Fig. 3 [2]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	2.8	6.9	1	8	1	9	ns
		$C_L = 50\text{ pF}$	-	4	7.9	1	9	1	10	ns
t_{en}	enable time	$\overline{OE}n$ to Yn; see Fig. 4								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	3.9	11.3	1	13	1	14	ns
		$C_L = 50\text{ pF}$	-	5.2	12.3	1	14	1	15.2	ns
t_{dis}	disable time	$\overline{OE}n$ to Yn; see Fig. 4 [2]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	3.6	7.5	1	8	1	8.5	ns
		$C_L = 50\text{ pF}$	-	5.7	11.9	1	13.5	1	14	ns
$t_{sk(o)}$	skew	$V_{CC} = 4.5\text{ V to }5.5\text{ V};$ $C_L = 50\text{ pF}$	-	-	1	-	1	-	1	ns
C_I	input capacitance	$V_I = V_{CC}$ or GND; $V_{CC} = 5\text{ V}$	-	2	6	-	6	-	6	pF
C_O	output capacitance	$V_O = V_{CC}$ or GND; $V_{CC} = 5\text{ V}$	-	5	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50\text{ pF};$ [3] $f = 10\text{ MHz}; V_I = \text{GND to } V_{CC}$	-	11	-	-	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 5\text{ V}$.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

Table 8. Noise characteristics

$GND = 0\text{ V}$. For test circuit see Fig. 5.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
V _{CC} = 5 V; C _L = 50 pF						
V _{OL(p)}	LOW-level output voltage (peak)		-	0.6	1.5	V
V _{OL(v)}	LOW-level output voltage (valley)		-1.5	-0.6	-	V
V _{OH(v)}	HIGH-level output voltage (valley)		-	4.0	-	V
V _{IH(AC)}	AC HIGH-level input voltage (dynamic)		2	-	-	V
V _{IL(AC)}	AC LOW-level input voltage (dynamic)		-	-	0.8	V

10.1. Waveforms and test circuit

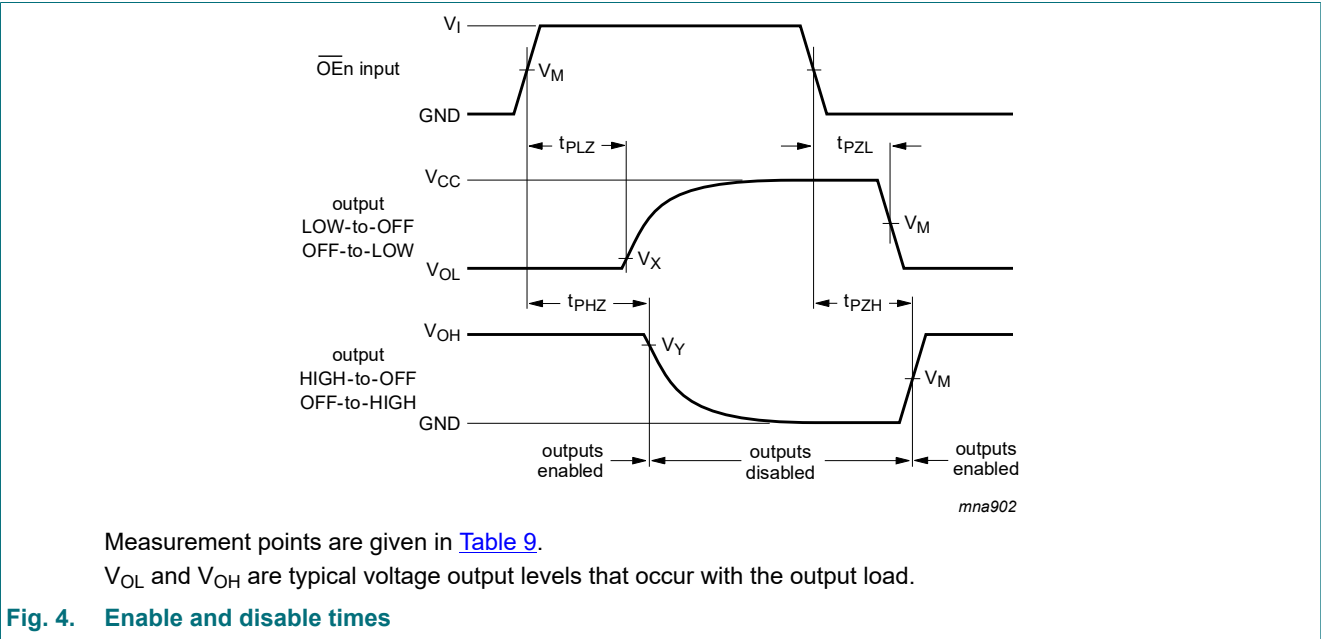
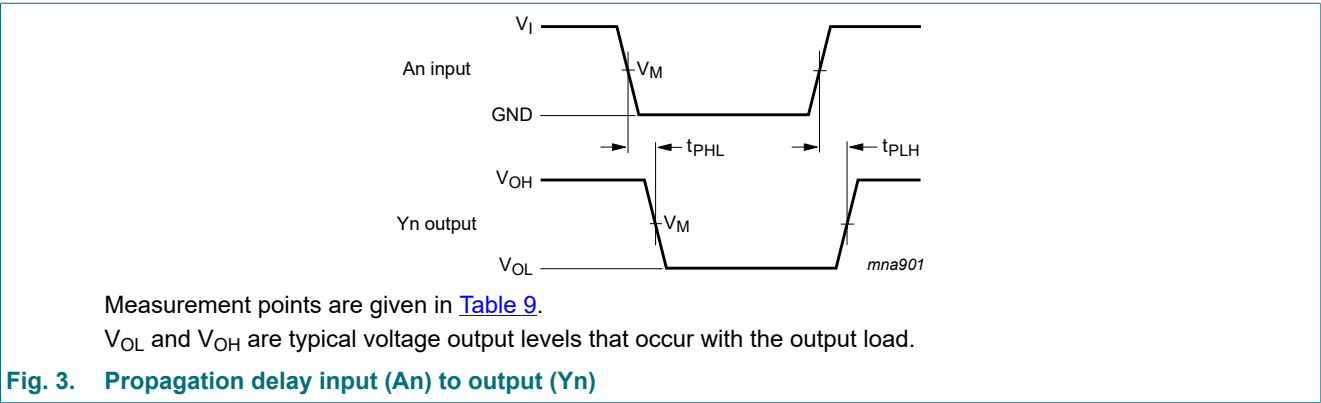


Table 9. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	$0.5 \times V_{CC}$	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

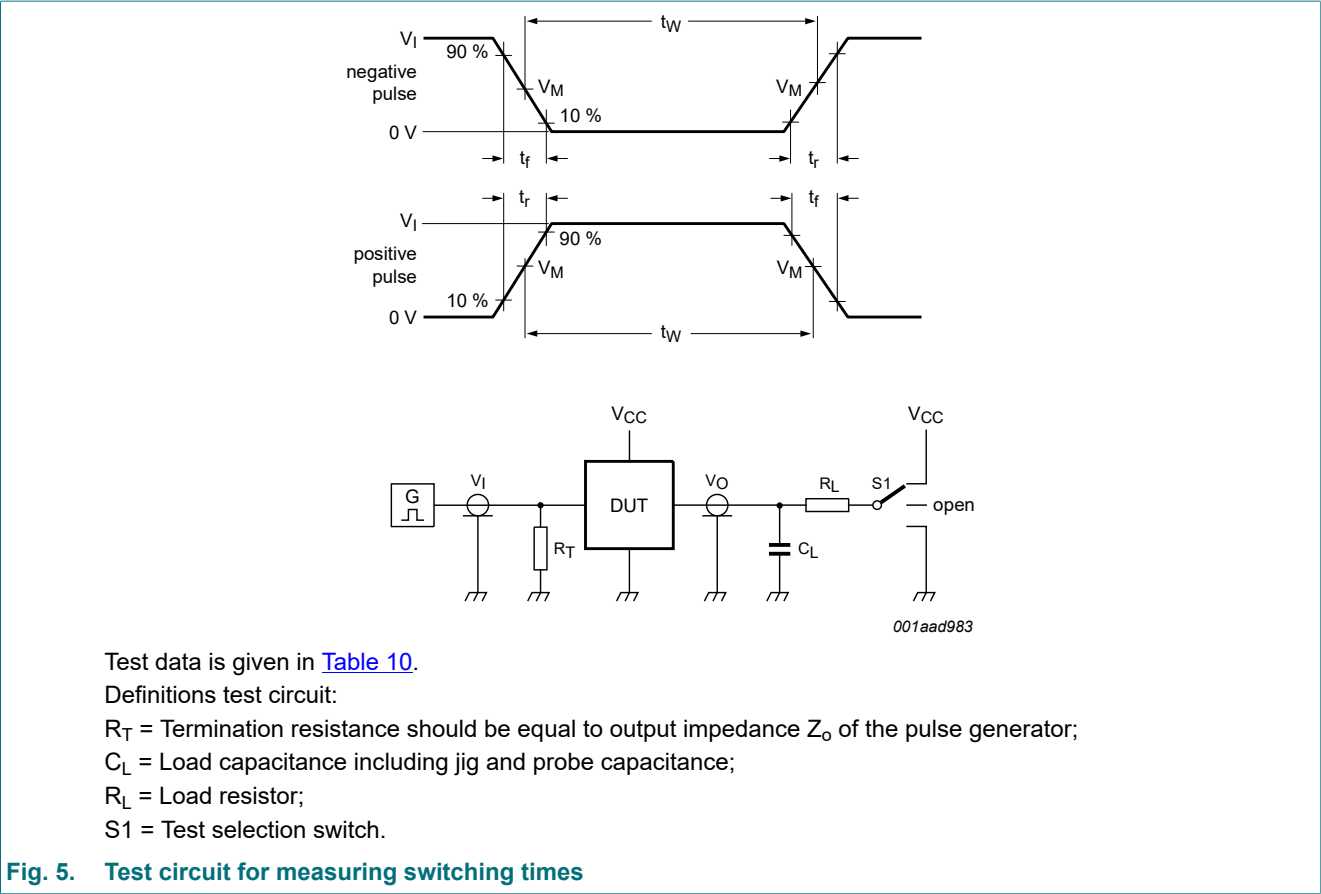


Table 10. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
GND to 3.0 V	3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

11. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

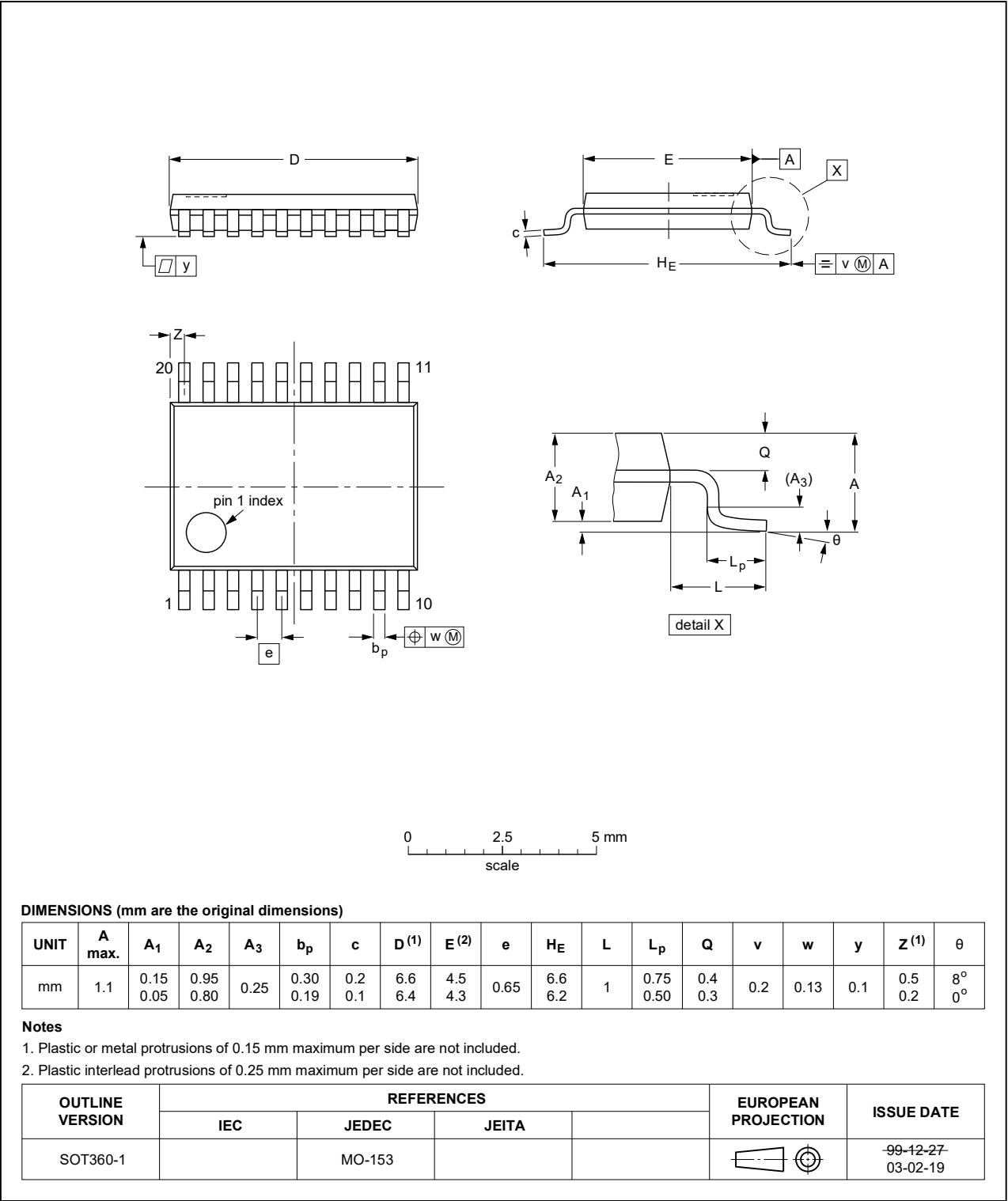


Fig. 6. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV541AT v.4	20240704	Product data sheet	-	74LV541AT v.3
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate.			
74LV541AT v.3	20161103	Product data sheet	-	74LV541AT v.2
Modifications:	Type number 74LV541ATBQ removed.			
74LV541AT v.2	20160527	Product data sheet	-	74LV541AT v.1
Modifications:	Table 6: conditions for additional supply current (ΔI_{CC}) corrected.			
74LV541AT v.1	20151221	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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