

HD-6409/883

CMOS Manchester Encoder-Decoder

FN2959
Rev 1.00
March 1997

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Converter or Repeater Mode
- Independent Manchester Encoder and Decoder Operation
- Static to One Megabit/Sec Data Rate Guaranteed
- Low Bit Error Rate
- Digital PLL Clock Recovery
- On Chip Oscillator
- Low Operating Power: 50mW Typical at +5V
- Available in 20 Lead Dual-In-Line and 20 Pad LCC Package

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PKG. NO.
HD1-6409/883	-55°C to +125°C	CERDIP	F20.3
HD4-6409/883	-55°C to +125°C	CLCC	J20.A

Description

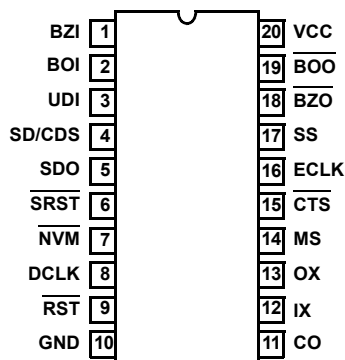
The HD-6409/883 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Nonreturn-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

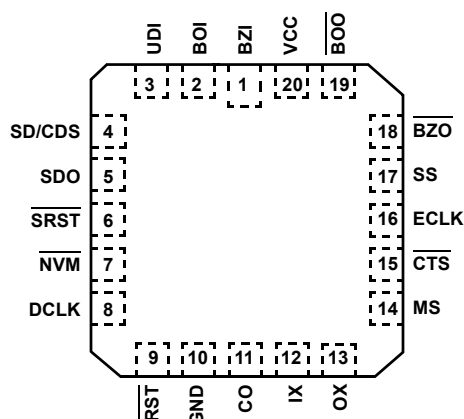
Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409/883 easily interfaces to protocol controllers.

Pinouts

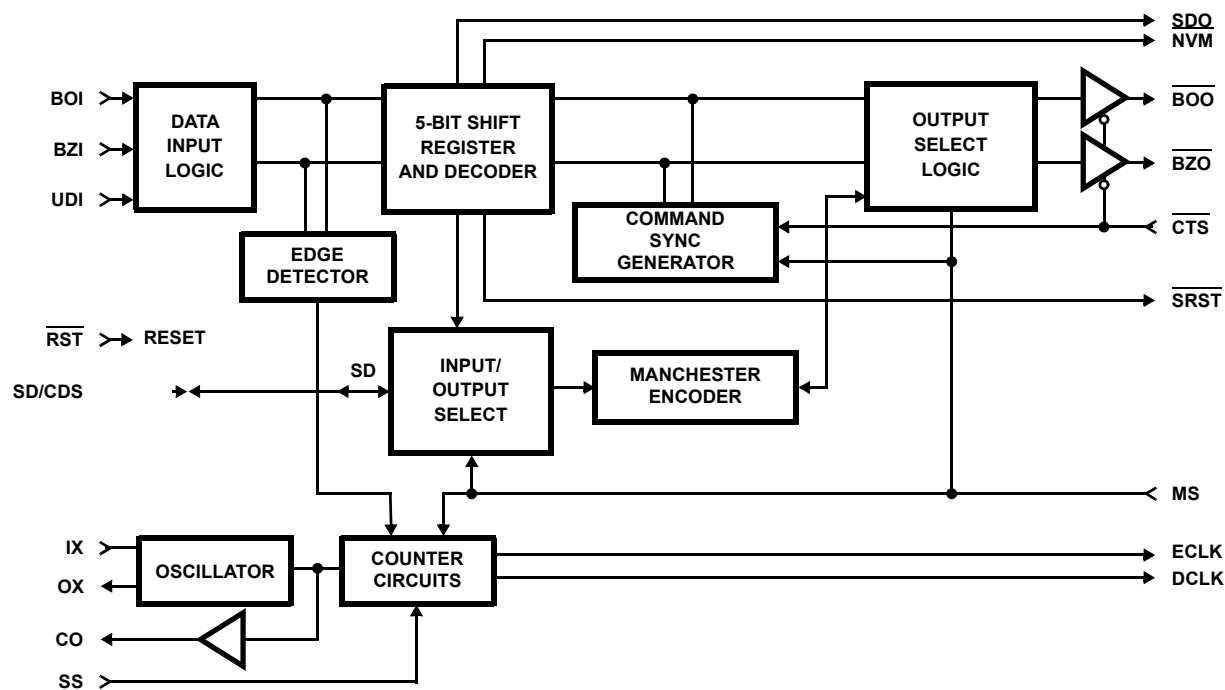
HD1-6409/883 (CERDIP)
TOP VIEW



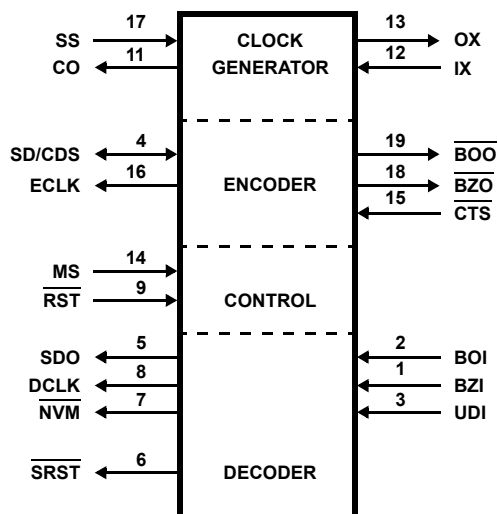
HD4-6409/883 (CLCC)
TOP VIEW



Block Diagram



Logic Symbol



Absolute Maximum Ratings

Supply Voltage +7.0V
 Input, Output or I/O Voltage Applied GND -0.5V to VCC +0.5V
 ESD Classification Class 1

Operating Conditions

Operating Temperature Range -55°C to +125°C
 Operating Voltage Range +4.5V to +5.5V
 Input Rise and Fall Times 50ns Max
 Sync. Transition Span (t₂) 1.5 DBP Typical, (Notes 1, 2)
 Short Data Transition Span (t₄) 0.5 DBP Typical, (Notes 1, 2)
 Long Data Transition Span (t₅) 1.0 DBP Typical, (Notes 1, 2)
 Zero Crossing Tolerance (t_{CD5}) (Note 3)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. DBP - Data Bit Period. Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X; one DBP = 32 Clock Cycles.
2. The input conditions specified are nominal values, the actual input waveforms transition spans may vary by ± 2 IX clock cycles (16X mode) or ± 6 IX clock cycles (32X mode).
3. The maximum zero crossing tolerance is ± 2 IX clock cycles (16X mode) or ± 6 IX clock cycles (32X mode) from the nominal.

Thermal Information

Thermal Resistance θ_{JA} (°C/W) θ_{JC} (°C/W)
 CERDIP Package 83 23
 CLCC Package 95 26
 Storage Temperature Range -65°C to +150°C
 Maximum Junction Temperature +175°C
 Maximum Lead Temperature (Soldering 10s) +300°C

Die Characteristics

Gate Count 250 Gates

TABLE 1. HD-6409/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Logic "1" Input Voltage	VIH	VCC = 4.5V	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	70% VCC	-	V
Logic "0" Input voltage	VIL	VCC = 4.5V	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	-	20% VCC	V
Logic "1" Input Voltage (RST)	VIHR	VCC = 5.5V	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	VCC -0.5	-	V
Logic "0" Input Voltage (RST)	VILR	VCC = 4.5V	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	-	GND +0.5	V
Logic "1" Input Voltage (IX)	VIHC	VCC = 5.5V	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	VCC -0.5	-	V
Logic "0" Input Voltage (IX)	VILC	VCC = 4.5V	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	-	GND +0.5	V
Input Leakage Current (Except IX)	II	VIN = VCC or GND VCC = 5.5V	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	-1.0	+1.0	μA
Input Leakage Current (IX)	II	VIN = VCC or GND VCC = 5.5V	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	-20	+20	μA
I/O Leakage Current	IO	VOUT = VCC or GND VCC = 5.5V	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	-10	+10	μA
Output HIGH Voltage (All except OX)	VOH	IOH = -2.0mA VCC = 4.5V (Note 1)	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	VCC -0.4	-	V
Output LOW Voltage (All except OX)	VOL	IOL = +2.0mA VCC = 4.5V (Note 1)	1, 2, 3	-55°C $\leq$ T _A $\leq$ +125°C	-	0.4	V

TABLE 1. HD-6409/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Standby Power Supply Current	ICCSB	VIN = VCC or GND, VCC = 5.5V, Outputs Open	1, 2, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	100	μA
Operating Power Supply Current	ICCOP	f = 16.0MHz, VIN = VCC or GND VCC = 5.5V, CL = 50pF	1, 2, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	18.0	mA
Functional Test	FT	(Note 2)	7, 8	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	-	-

NOTES:

- Interchanging of force and sense conditions is permitted.
- Tested as follows: f = 16MHz, VIH = 70% VCC, VIL = 20% VCC, VOH $\geq$ VCC/2, and VOL $\leq$ VCC/2, VCC = 4.5V and 5.5V.

TABLE 2. HD-6409/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Clock Frequency	fC		9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	16	MHz
Clock Period	tC		9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	1/fC	-	sec
Bipolar Pulse Width	t1		9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	tC + 10	-	ns
One-Zero Overlap	t3		9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	tC - 10	ns
Clock High Time	tCH	f = 16.0MHz	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	20	-	ns
Clock Low Time	tCL	f = 16.0MHz	9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	20	-	ns
Serial Data Setup Time	tCE1		9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	120	-	ns
Serial Data Hold Time	tCE2		9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	0	-	ns
DCLK to SDO, $\overline{\text{NVM}}$	tCD2		9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	40	ns
ECLK to $\overline{\text{BZO}}$	tR2		9, 10, 11	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	40	ns

NOTES:

- AC Testing as follows: f = 4.0MHz, VIH = 70% VCC, VIL = 20% VCC, Speed Select = 16X; VOH $\geq$ VCC/2, VOL $\leq$ VCC/2; VCC = 4.5V and 5.5V; Input rise and fall times driven at 1 ns/V, Output load = 50pF.

TABLE 3. HD-6409/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VCC = Open, f = 1MHz	1, 2	$T_A = +25^{\circ}\text{C}$	-	10	pF
I/O Capacitance	CI/O	All Measurements are referenced to device GND	1, 2	$T_A = +25^{\circ}\text{C}$	-	12	pF
Output Rise Time (All except CO)	tr	From 1.0 to 3.5V CL = 50pF	1, 2	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	50	ns

TABLE 3. HD-6409/883 ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Fall Time (All except CO)	tf	From 3.5 to 1.0V CL = 50pF	1, 2	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	50	ns
CO Rise Time	tr	From 1.0 to 3.5V CL = 20pF	1, 2	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	11	ns
CO Fall Time	tf	From 3.5 to 1.0V CL = 20pF	1, 2	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	11	ns
ECLK to $\overline{\text{BZO}}$, $\overline{\text{BOO}}$	tCE3		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	0.5	1.0	DBP
$\overline{\text{CTS}}$ Low to $\overline{\text{BZO}}$ $\overline{\text{BOO}}$ Enabled	tCE4		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	0.5	1.5	DBP
$\overline{\text{CTS}}$ Low to ECLK Enabled	tCE5		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	10.5	11.5	DBP
$\overline{\text{CTS}}$ High to ECLK Disabled	tCE6		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	-	1.0	DBP
$\overline{\text{CTS}}$ High to $\overline{\text{BZO}}$ $\overline{\text{BOO}}$ Disabled	tCE7		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	1.5	2.5	DBP
UDI to SDO, $\overline{\text{NVM}}$	tCD1		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	2.5	3.0	DBP
$\overline{\text{RST}}$ Low to DCLK, SDO, $\overline{\text{NVM}}$ Low	tCD3		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	0.5	1.5	DBP
$\overline{\text{RST}}$ High to DCLK, Enabled	tCD4		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	0.5	1.5	DBP
UDI to $\overline{\text{BZO}}$, $\overline{\text{BOO}}$	tR1		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	0.5	1.0	DBP
UDI to SDO, $\overline{\text{NVM}}$	tR3		1, 3	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	2.5	3.0	DBP

NOTES:

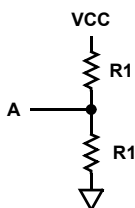
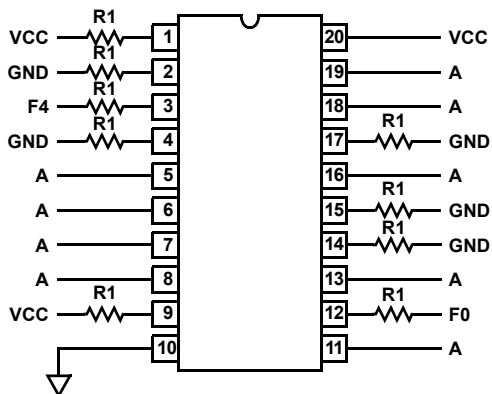
1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested.
2. Guaranteed via characterization at initial device design and after major process and/or design changes.
3. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.

TABLE 4. APPLICABLE SUBGROUPS

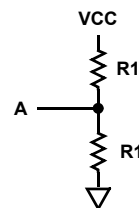
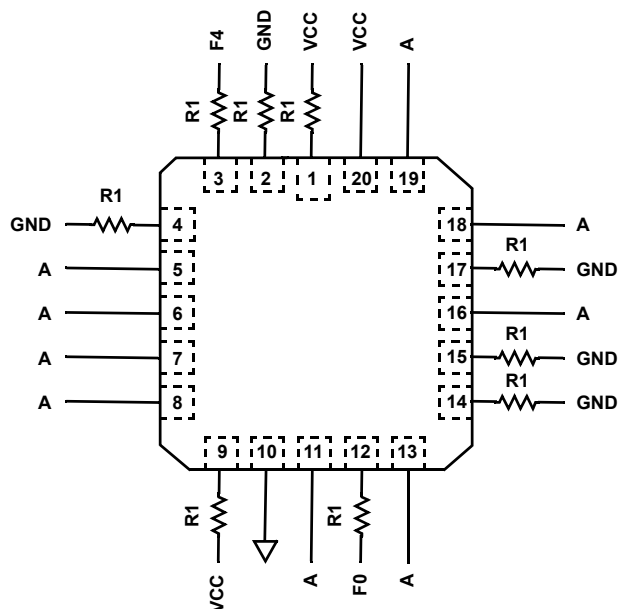
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuits

HD-6409/883 Cerdip



HD-6409/883 CLCC



NOTES:

1. VCC = 5.5V $\pm$ 0.5V
2. VIH = 4.5V $\pm$ 10%
3. VIL = -0.2V to 0.4V
4. R1 = 47k Ω $\pm$ 5%
5. F0 = 100kHz $\pm$ 10%
6. F4 = F0/16

Die Characteristics

DIE DIMENSIONS:

88 x 78 x 19 $\pm$ 1mils

METALLIZATION:

Type: Silicon - Aluminum

Thickness: Metal 1: 8kÅ $\pm$ 1kÅ
Metal 2: 16kÅ $\pm$ 1kÅ

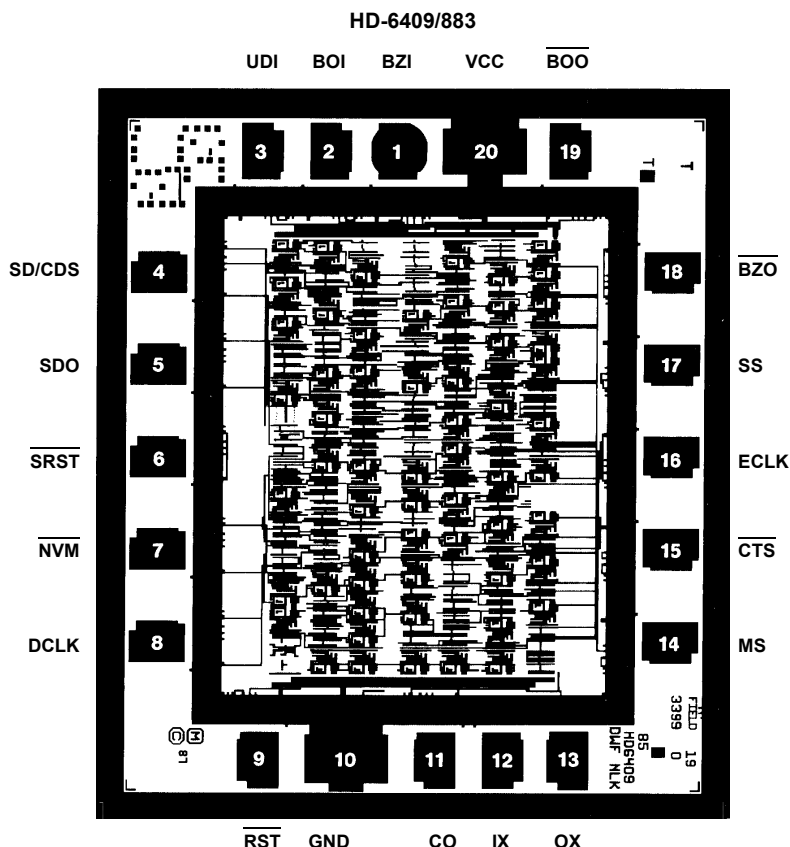
GLASSIVATION:

Type: Si₃N₄ • SiOXThickness: 10kÅ $\pm$ 2kÅ

WORST CASE CURRENT DENSITY:

0.8 x 10⁵ A/cm²

Metallization Mask Layout



© Copyright Intersil Americas LLC 2002. All Rights Reserved.

All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.htmlIntersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com