Toshiba CMOS Digital Integrated Circuit   Silicon Monolithic

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Octal Bus Switch

The TC7MB3244FK provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 4-bit low-impedance switches with separate output-enable ($\overline{\text{OE}}$) inputs. When $\overline{\text{OE}}$ is low, the switch is on and data can flow from port A to port B, or vice versa. When $\overline{\text{OE}}$ is high, the switch is open and a high-impedance state exists between the two ports.

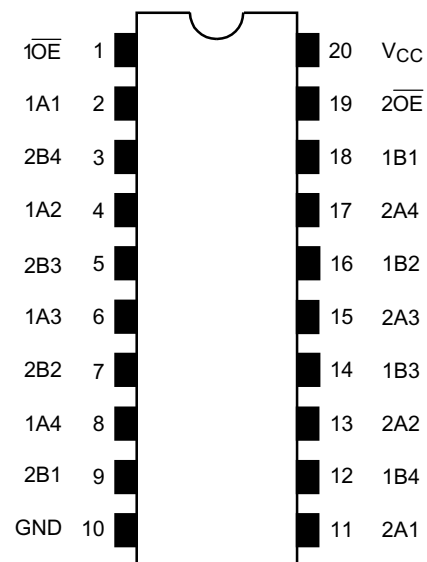All inputs are equipped with protection circuits against static discharge.

VSSOP20-P-0030-0.50
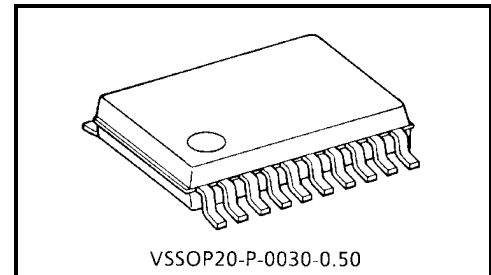
Weight: 0.03 g (typ.)

Features

- Operating voltage: $V_{CC} = 4.5{\sim}5.5$ V
- High speed: $t_{pd} = 0.25$ ns (max)
- Low on resistance: $R_{ON} = 5\ \Omega$ (typ.)
- ESD performance: Human body model > ±2000 V
  Machine model > ±200 V
- Compatible with TTL outputs (control inputs)
- Package: VSSOP (US20)
- Pin compatible with the 74xx244 type.
  Functionally equivalent to (FST/CBT) 3244.
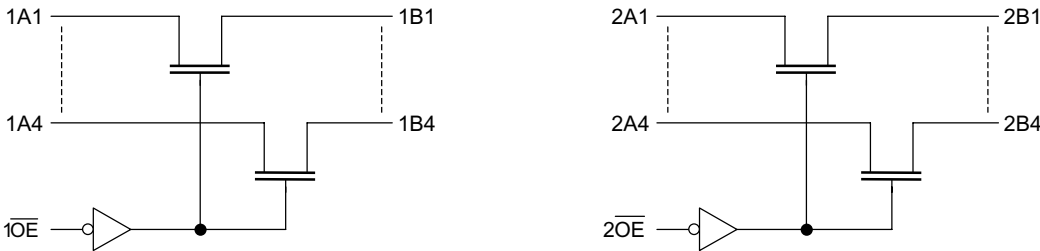
Pin Assignment (top view)

Pin	Name		Pin	Name
1	$1\overline{\text{OE}}$		20	V_{CC}
2	1A1		19	$2\overline{\text{OE}}$
3	2B4		18	1B1
4	1A2		17	2A4
5	2B3		16	1B2
6	1A3		15	2A3
7	2B2		14	1B3
8	1A4		13	2A2
9	2B1		12	1B4
10	GND		11	2A1

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Truth Table

Inputs	Function
$\overline{OE}$	
L	A port = B port
H	Disconnect

System Diagram

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply range	V_{CC}	−0.5~7.0	V
DC input voltage	V_{IN}	−0.5~7.0	V
DC switch voltage	V_S	−0.5~7.0	V
Input diode current	I_{IK}	−50	mA
Continuous channel circuit	I_S	128	mA
Power dissipation	P_D	180	mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65~150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5~5.5	V
Input voltage	V_{IN}	0~5.5	V
Switch voltage	V_S	0~5.5	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

Electrical Characteristics

DC Characteristics (Ta = −40~85°C)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Typ. (Note1)	Max	Unit
Input voltage	"H" level	V_{IH}	—		4.5~5.5	2.0	—	—	V
	"L" level	V_{IL}	—		4.5~5.5	—	—	0.8	
Input leakage current		I_{IN}	V_{IN} = 0~5.5 V		4.5~5.5	—	—	±1.0	µA
Power off leakage current		I_{OFF}	A, B, $\overline{OE}$ = 0~5.5 V		0	—	—	±1.0	µA
Off-STATE leakage current (switch off)		I_{SZ}	A, B = 0~5.5 V, $\overline{OE}$ = V_{CC}		4.5~5.5	—	—	±1.0	µA
ON resistance (Note2)		R_{ON}	V_{IS} = 0 V	I_{IS} = 64 mA	4.5	—	5	7	Ω
				I_{IS} = 30 mA	4.5	—	5	7	
			V_{IS} = 2.4 V, I_{IS} = 15 mA		4.5	—	10	15	
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0		5.5	—	—	10	µA
Increase in I_{CC} per input		ΔI_{CC}	V_{IN} = 3.4 V (one input)		5.5	—	—	2.5	mA

Note 1: Typical values are at V_{CC} = 5 V, Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = −40~85°C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Propagation delay time (bus to bus)	t_{pLH} t_{pHL}	Figure 1, Figure 2	(Note3)	4.5	—	0.25	ns
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 3		4.5	—	5.0	ns
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 3		4.5	—	5.0	ns

Note 3: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Typ.	Unit
Control pin input capacitance	C_{IN}		(Note4)	5.0	3	pF
Switch terminal capacitance	$C_{I/O}$	$\overline{OE}$ = V_{CC}	(Note4)	5.0	10	pF

Note 4: Parameter guaranteed by design.

AC Test Circuit

Switch — Open / 7.0 V / GND

R_L

Output — Measure

C_L R_L

$C_L = 50\ pF$
$R_L = 500\ \Omega$

Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	7.0 V
t_{pHZ}, t_{pZH}	Open

Figure 1

AC Waveform

t_r 2.5 ns t_f 2.5 ns

Input (A, B)   90% 1.5 V   3.0 V   10%   GND

Output (B, A) V_{OH} 1.5 V V_{OL}

t_{pLH} t_{pHL}

Figure 2 t_{pLH}, t_{pHL}

t_r 2.5 ns t_f 2.5 ns

Output Enable ($\overline{OE}$)   90% 1.5 V   3.0 V   10%   GND

t_{pLZ} t_{pZL}

Output (A, B) Low to Off to Low   3.5 V   1.5 V V_{OL}

$V_{OL} + 0.3\ V$

t_{pHZ} t_{pZH}

Output (A, B) High to Off to High $V_{OH} - 0.3\ V$ V_{OH} 1.5 V   GND

Outputs enabled   Outputs disabled   Outputs enabled
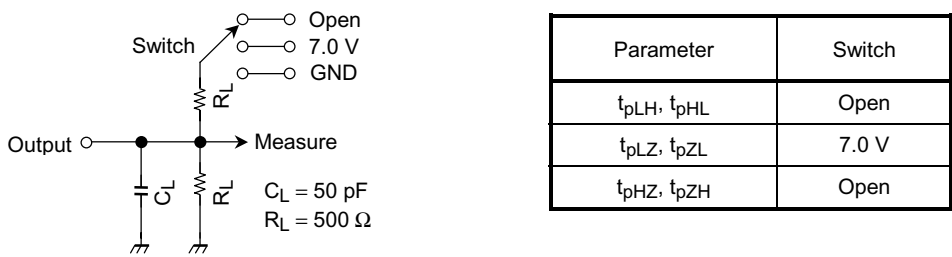
Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

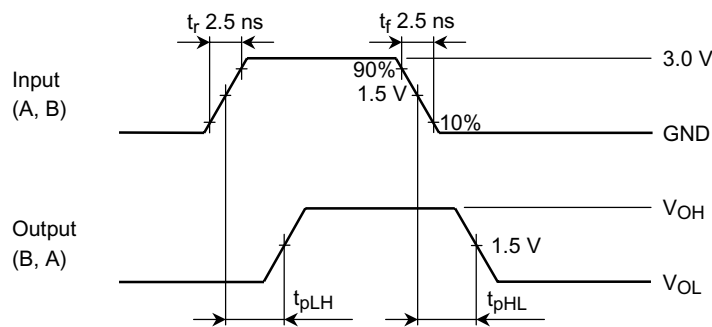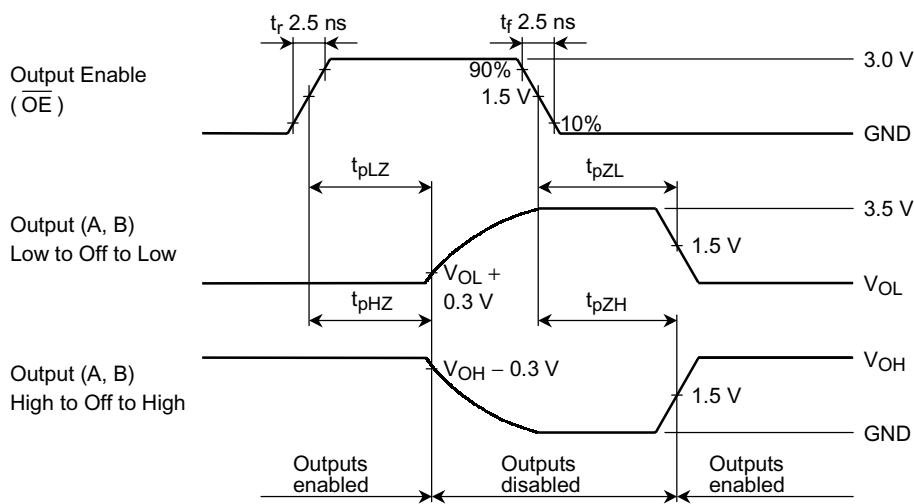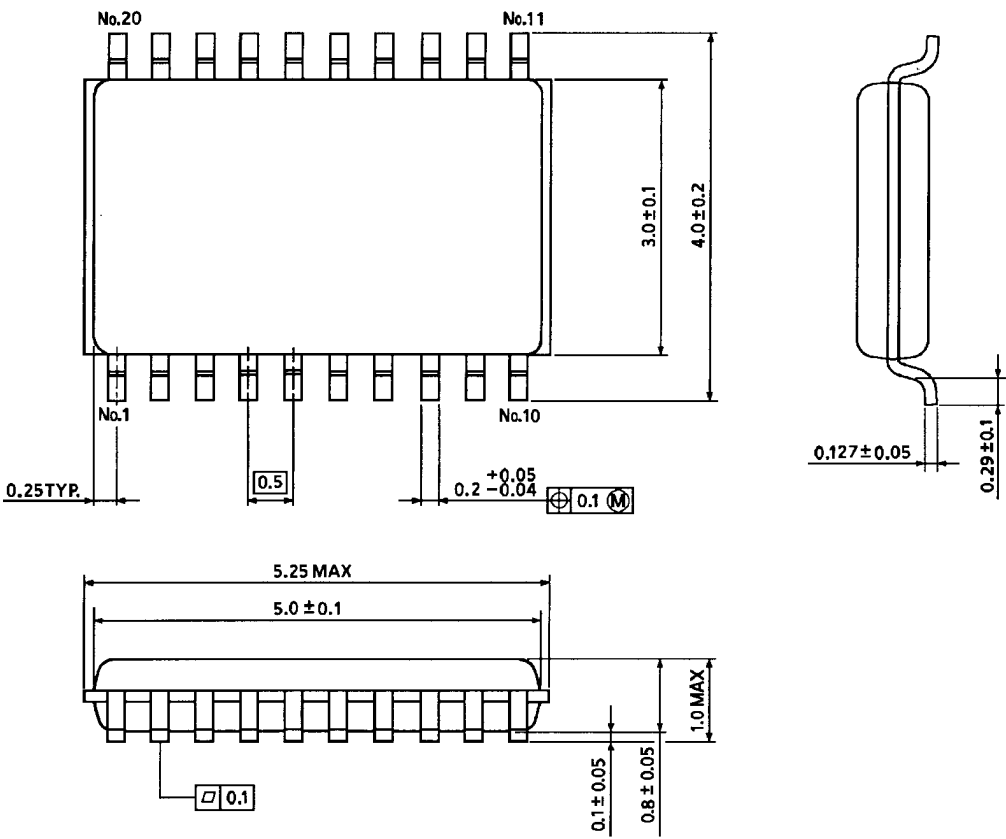## Package Dimensions

VSSOP20-P-0030-0.50   Unit : mm

Weight: 0.03 g (typ.)