



MOS FET
MTM231232LBF

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Silicon P-channel MOSFET
For Switching

MTM76123 in SMini3 type package

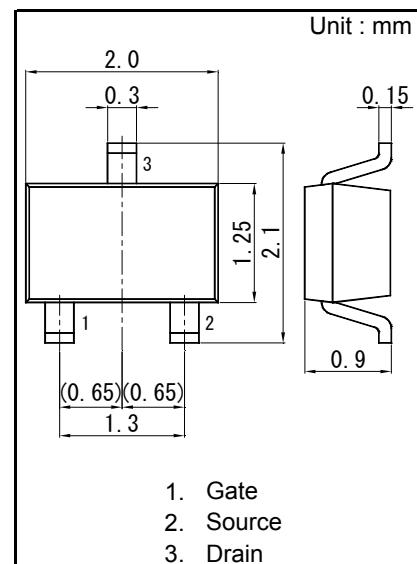
■ Features

- Low Drain-source On-state Resistance : $R_{DS(on)}$ typ. = $40\text{ m}\Omega$ ($V_{GS} = -4\text{ V}$)
- Low Drive Voltage : 2.5 V Drive
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol : BL

■ Packaging

Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)



1. Gate
2. Source
3. Drain

Panasonic	SMini3-G1-B
JEITA	SC-70
Code	SOT-323

■ Absolute Maximum Ratings $T_a = 25\text{ }^{\circ}\text{C}$

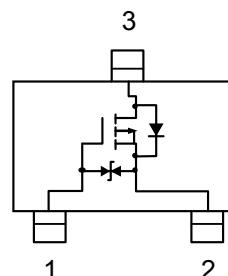
Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DS}	-20	V
Gate to Source Voltage	V_{GS}	± 10	V
Drain Current	I_D	-3	A
Drain Current (Pulsed) ^{*1}	I_{Dp}	-16	A
Total Power Dissipation ^{*2}	P_D	500	mW
Channel Temperature	T_{ch}	150	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^{\circ}\text{C}$

Note ^{*1} Pulse width $\leq 10\text{ }\mu\text{s}$, Duty cycle $\leq 1\%$

^{*2} Measuring on ceramic board at $40\text{ mm} \times 38\text{ mm} \times 0.1\text{ mm}$.

Absolute maximum rating P_D Non-heat sink shall be made 150 mW.

Internal Connection



Pin Name

1. Gate
2. Source
3. Drain

■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

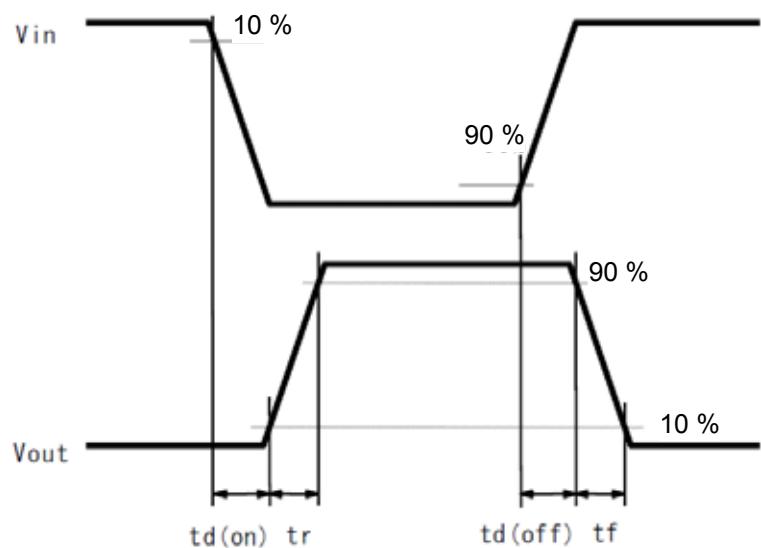
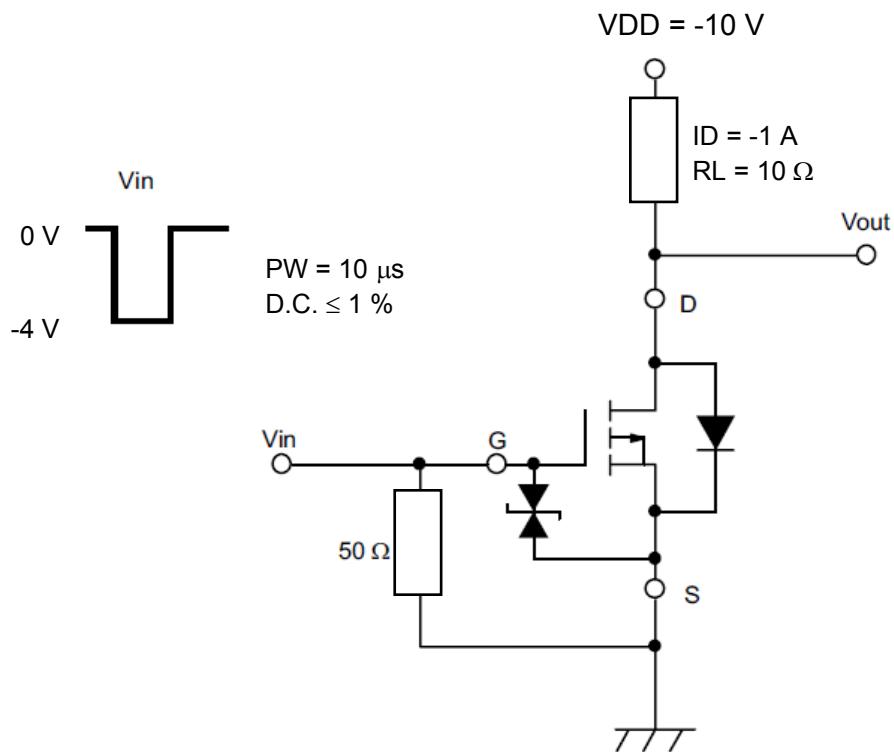
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = -1 mA, VGS = 0 V	-20			V
Zero Gate Voltage Drain Current	IDSS	VDS = -20 V, VGS = 0 V			-1	μA
Gate-source Leakage Current	IGSS	VGS = ± 8 V, VDS = 0 V			± 10	μA
Gate-source Threshold Voltage	Vth	ID = -1 mA, VDS = -10 V	-0.4	-0.85	-1.3	V
Drain-source On-state Resistance ^{*1}	RDS(on)1	ID = -1 A, VGS = -4 V		40	55	$\text{m}\Omega$
	RDS(on)2	ID = -0.5 A, VGS = -2.5 V		45	70	
Forward transfer admittance ^{*1}	Yfs	ID = -1 A, VDS = -10 V, f = 1 kHz	3.5			S
Input Capacitance	Ciss	VDS = -10 V, VGS = 0 V f = 1 MHz	1 000			pF
Output Capacitance	Coss			120		
Reverse Transfer Capacitance	Crss			120		
Turn-on Delay Time ^{*2}	td(on)	VDD = -10 V, VGS = 0 to -4 V ID = -1 A	25			ns
Rise Time ^{*2}	tr			25		
Turn-off Delay Time ^{*2}	td(off)	VDD = -10 V, VGS = -4 to 0 V ID = -1 A	120			ns
Fall Time ^{*2}	tf			70		

Note : Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Pulse test : Pulse width $\leq 300 \mu\text{s}$, Duty cycle $\leq 2\%$

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

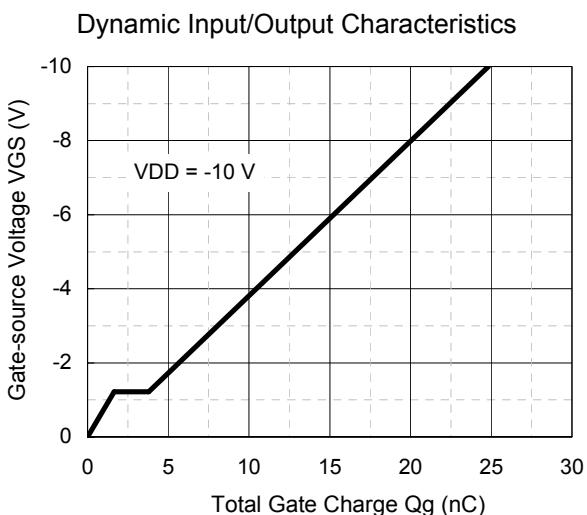
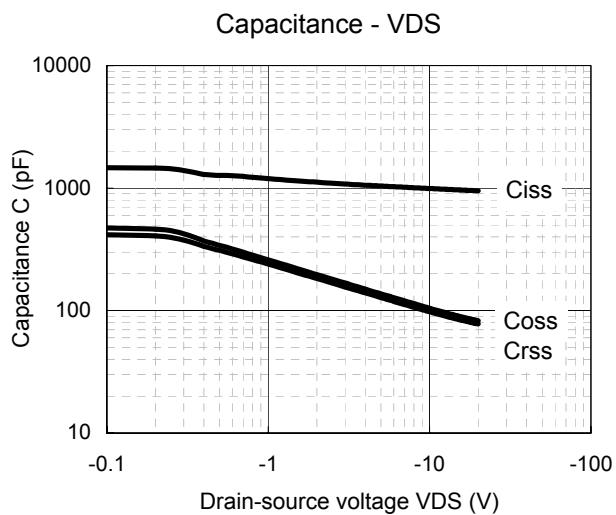
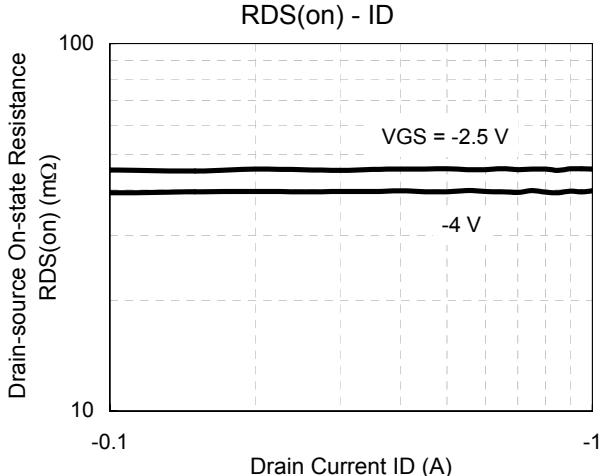
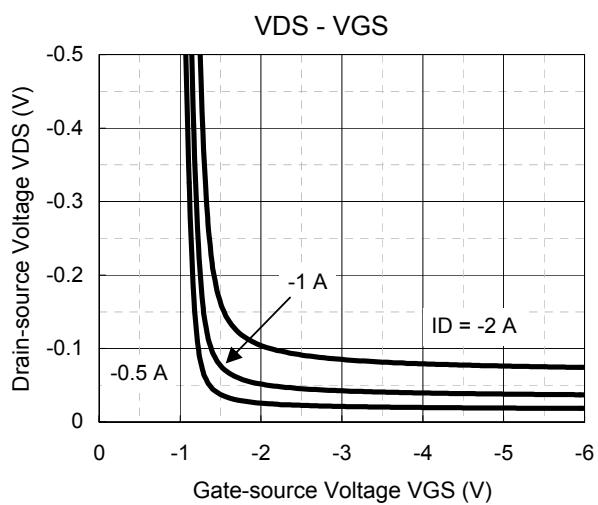
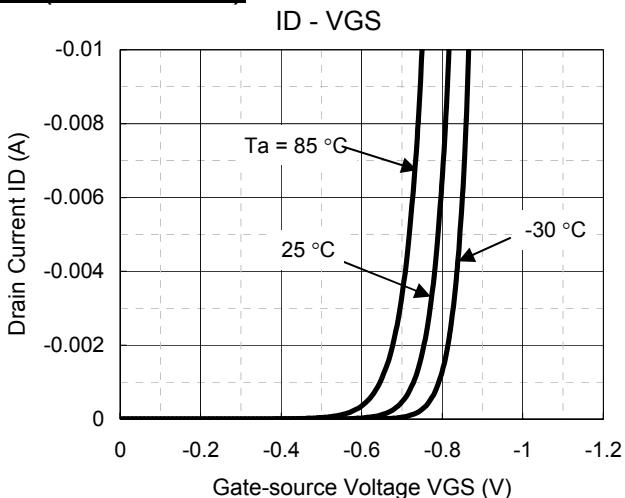
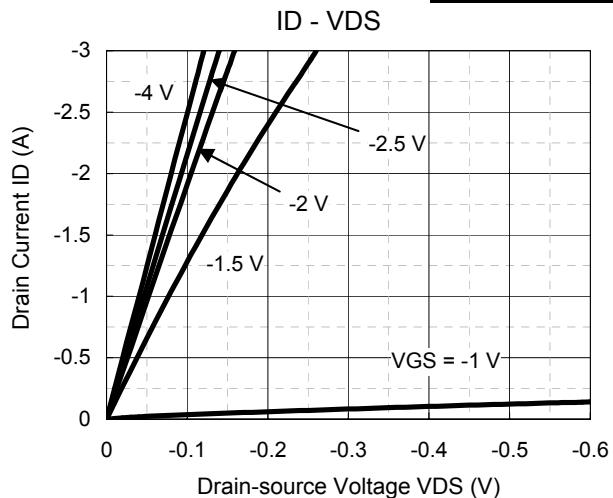
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



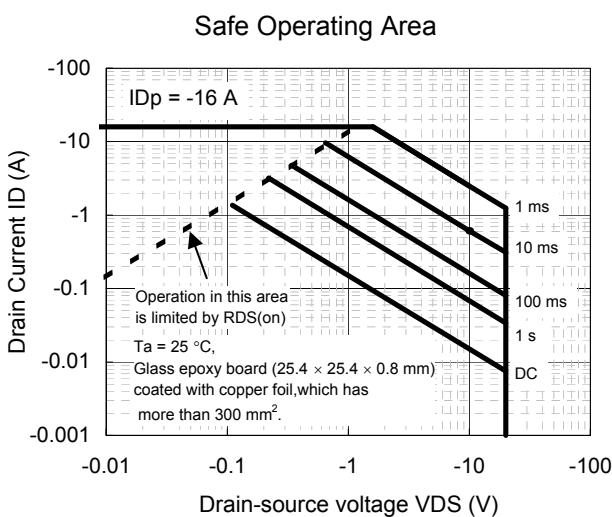
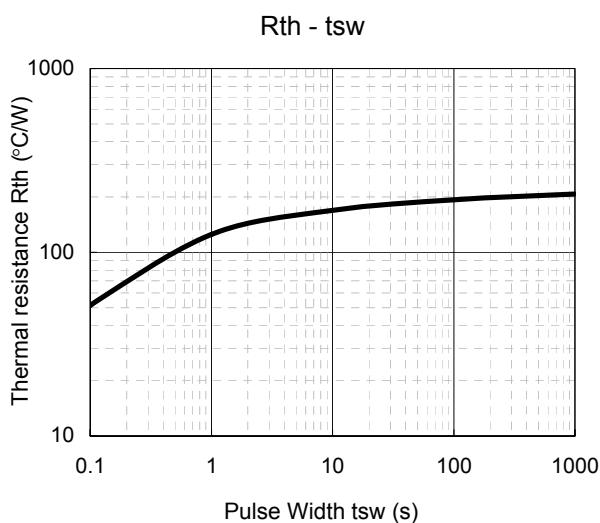
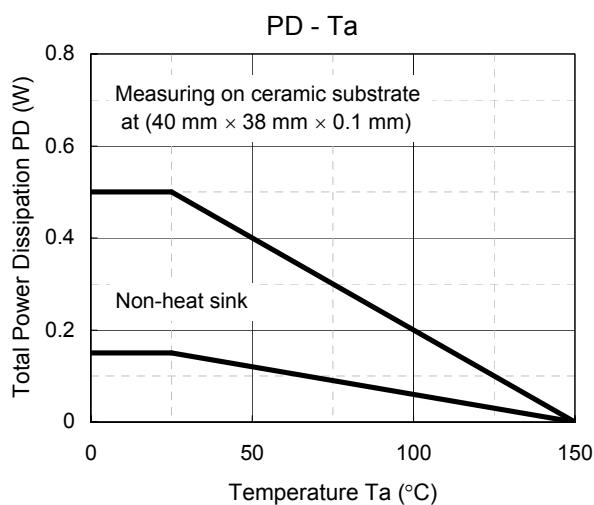
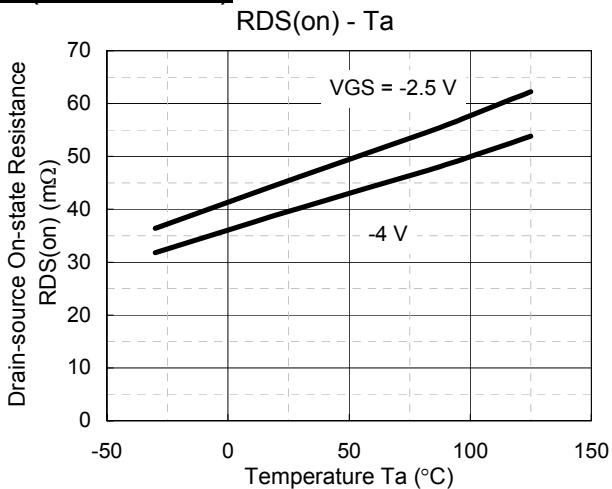
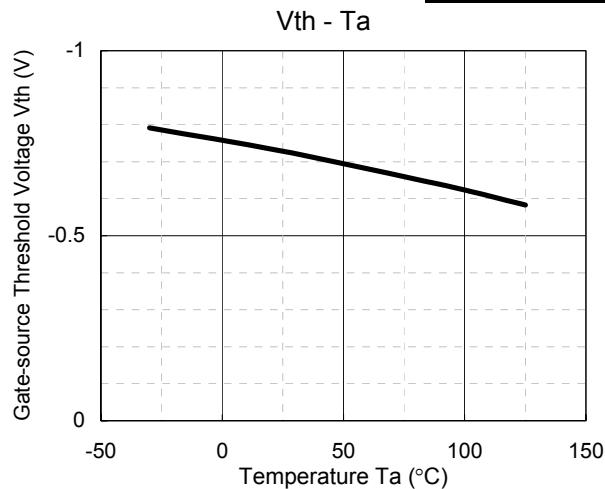


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Technical Data (reference)



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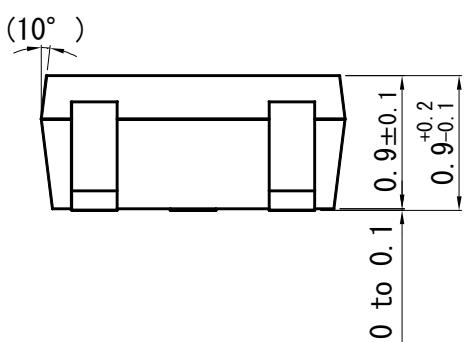
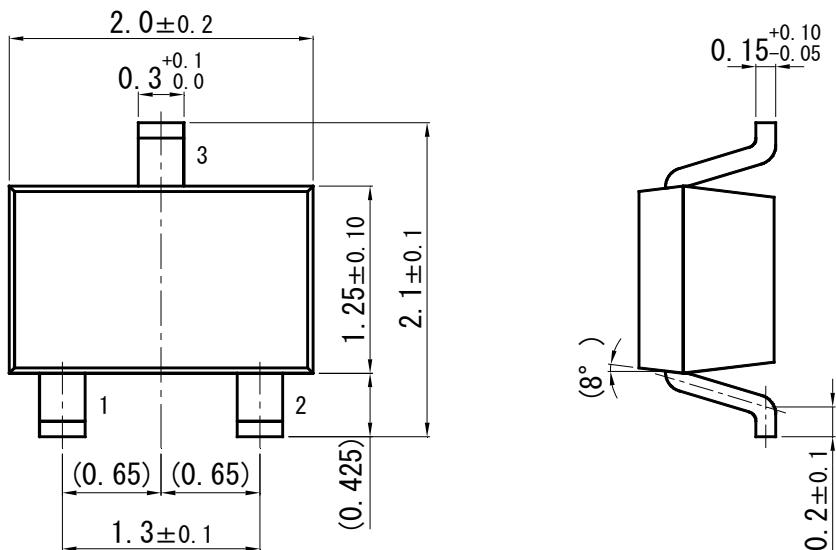


Panasonic

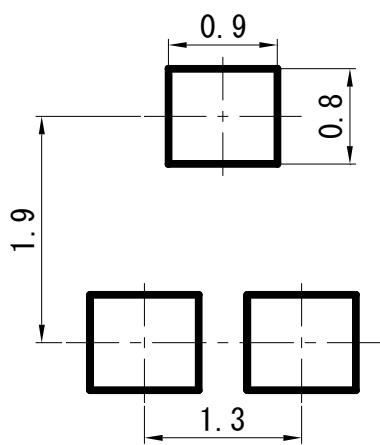
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SMini3-G1-B

Unit : mm



■ Land Pattern (Reference) (Unit : mm)



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