

## General Description

The 810251I is a high performance, low jitter/low phase noise VCXO. The 810251I uses a low frequency and low cost pullable crystal to achieve jitter attenuation for synchronous Ethernet applications. The 810251I can take an input of either 25MHz or 125MHz and produce a single LVCMOS output of 25MHz.

The device is packaged in a small 16 lead TSSOP package and is ideal for use on space constrained boards typically encountered in most synchronous ethernet applications.

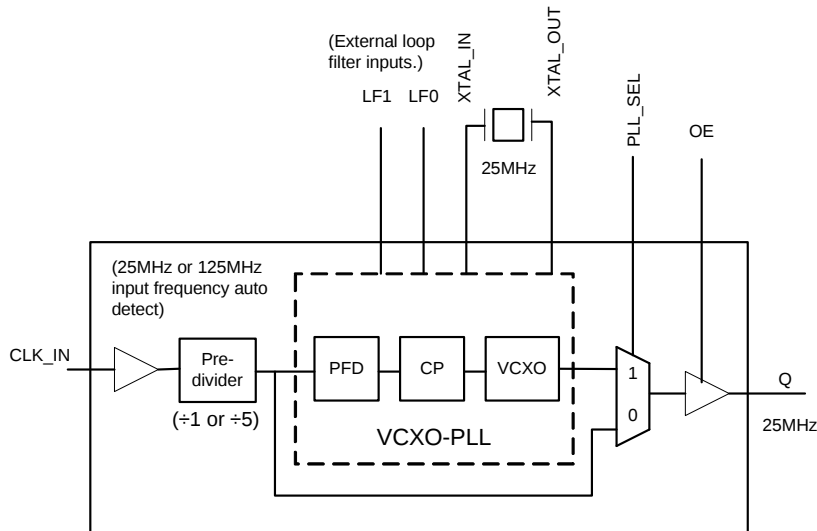
## Applications

- Synchronous Ethernet v0.39a
- End equipment compliant with Std IEEE 802.039a

## Features

- One single-ended output (LVCMOS or LVTTTL levels), output Impedance: 15Ω
- Phase jitter attenuation by the VCXO-PLL using a 25MHz pullable external crystal (XTAL)
- Input frequencies: 25MHz or 125MHz
- Output frequency: 25MHz
- PLL loop bandwidth adjustable by external components
- 25MHz or 125MHz auto input frequency detect
- Full 3.3V or 2.5V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignment

|          |   |    |          |
|----------|---|----|----------|
| PLL_SEL  | 1 | 16 | CLK_IN   |
| GND      | 2 | 15 | VDD      |
| Reserved | 3 | 14 | LF1      |
| Q        | 4 | 13 | LF0      |
| VDDO     | 5 | 12 | GND      |
| OE       | 6 | 11 | XTAL_IN  |
| VDDA     | 7 | 10 | XTAL_OUT |
| VDD      | 8 | 9  | GND      |

**810251I**

**16-Lead TSSOP**  
**4.4mm x 5.0mm x 0.925mm**  
 package body  
 G Package  
 Top View

**Table 1. Pin Descriptions**

| Number   | Name              | Type                 |          | Description                                                                                                        |
|----------|-------------------|----------------------|----------|--------------------------------------------------------------------------------------------------------------------|
| 1        | PLL_SEL           | Input                | Pullup   | When logic HIGH, the VCXO-PLL is enabled. When LOW, the VCXO-PLL is in bypass mode. LVCMOS/LVTTL interface levels. |
| 2, 9, 12 | GND               | Power                |          | Power supply ground.                                                                                               |
| 3        | Reserved          | Reserved             |          | Reserved pin. Do not connect.                                                                                      |
| 4        | Q                 | Output               |          | Single-ended clock output. LVCMOS/ LVTTL interface levels.                                                         |
| 5        | V <sub>DDO</sub>  | Power                |          | Output power supply pin.                                                                                           |
| 6        | OE                | Input                | Pullup   | Output enable pin for Q output. LVCMOS/LVTTL interface levels.                                                     |
| 7        | V <sub>DDA</sub>  | Power                |          | Analog supply pin.                                                                                                 |
| 8, 15    | V <sub>DD</sub>   | Power                |          | Core supply pins.                                                                                                  |
| 10, 11   | XTAL_OUT, XTAL_IN | Input                |          | VCXO crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.                                   |
| 13, 14   | LF0, LF1          | Analog Input/ Output |          | Loop filter connection node pins.                                                                                  |
| 16       | CLK_IN            | Input                | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels.                                                           |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter                     | Test Conditions                             | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------------|---------------------------------------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance             |                                             |         | 4       |         | pF    |
| C <sub>PD</sub>       | Power Dissipation Capacitance | V <sub>DD</sub> , V <sub>DDO</sub> = 3.465V |         | 8       |         | pF    |
|                       |                               | V <sub>DD</sub> , V <sub>DDO</sub> = 2.625V |         | 5       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor         |                                             |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor       |                                             |         | 51      |         | kΩ    |
| R <sub>OUT</sub>      | Output Impedance              | V <sub>DDO</sub> = 3.3V±5%                  |         | 15      |         | Ω     |
|                       |                               | V <sub>DDO</sub> = 2.5V±5%                  |         | 20      |         | Ω     |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item                                     | Rating                   |
|------------------------------------------|--------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                     |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, $V_O$                           | -0.5V to $V_{DD} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 92.4°C/W (0 mps)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol    | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | $V_{DD} - 0.07$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 3.135           | 3.3     | 3.465    | V     |
| $I_{DD}$  | Power Supply Current  |                 |                 |         | 40       | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |                 |         | 7        | mA    |
| $I_{DDO}$ | Output Supply Current | No Load         |                 |         | 5        | mA    |

**Table 3B. Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol    | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 2.375           | 2.5     | 2.625    | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | $V_{DD} - 0.07$ | 2.5     | $V_{DD}$ | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 2.375           | 2.5     | 2.625    | V     |
| $I_{DD}$  | Power Supply Current  |                 |                 |         | 35       | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |                 |         | 7        | mA    |
| $I_{DDO}$ | Output Supply Current | No Load         |                 |         | 5        | mA    |

**Table 3C. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol   | Parameter                   |             | Test Conditions                               | Minimum | Typical | Maximum        | Units   |
|----------|-----------------------------|-------------|-----------------------------------------------|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage          |             | $V_{DD} = 3.465V$                             | 2       |         | $V_{DD} + 0.3$ | V       |
|          |                             |             | $V_{DD} = 2.625V$                             | 1.7     |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage           |             | $V_{DD} = 3.465V$                             | -0.3    |         | 0.8            | V       |
|          |                             |             | $V_{DD} = 2.625V$                             | -0.3    |         | 0.7            | V       |
| $I_{IH}$ | Input High Current          | CLK_IN      | $V_{DD} = V_{IN} = 3.465V$ or $2.625V$        |         |         | 150            | $\mu A$ |
|          |                             | OE, PLL_SEL | $V_{DD} = V_{IN} = 3.465V$ or $2.625V$        |         |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current           | CLK_IN      | $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -5      |         |                | $\mu A$ |
|          |                             | OE, PLL_SEL | $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -150    |         |                | $\mu A$ |
| $V_{OH}$ | Output High Voltage; NOTE 1 |             | $V_{DDO} = 3.3V \pm 5\%$                      | 2.6     |         |                | V       |
|          |                             |             | $V_{DDO} = 2.5V \pm 5\%$                      | 1.8     |         |                | V       |
| $V_{OL}$ | Output Low Voltage; NOTE 1  |             | $V_{DDO} = 3.3V \pm 5\%$                      |         |         | 0.6            | V       |
|          |                             |             | $V_{DDO} = 2.5V \pm 5\%$                      |         |         | 0.5            | V       |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information section. *Load Test Circuit diagrams.*

## AC Electrical Characteristics

**Table 4A. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol            | Parameter                         | Test Conditions                                    | Minimum | Typical | Maximum | Units |
|-------------------|-----------------------------------|----------------------------------------------------|---------|---------|---------|-------|
| $f_{REF}$         | Input Reference Frequency         |                                                    |         | 25      |         | MHz   |
|                   |                                   |                                                    |         | 125     |         | MHz   |
| $f_{VCO}$         | VCXO-PLL Frequency                |                                                    |         | 25      |         | MHz   |
| $f_{OUT}$         | Output Frequency                  |                                                    |         | 25      |         | MHz   |
| $t_{JIT(CC)}$     | Cycle-to-Cycle Jitter; NOTE 1     |                                                    |         |         | 45      | ps    |
| $t_{jit(\theta)}$ | RMS Phase Jitter (Random); NOTE 2 | $f_{OUT} = 25MHz$ , Integration Range: 1kHz – 1MHz |         | 0.22    |         | ps    |
| $t_{JIT(PER)}$    | Period jitter                     |                                                    |         |         | 5       | ps    |
| $t_R / t_F$       | Output Rise/Fall Time             | 20% to 80%                                         | 500     |         | 1200    | ps    |
| odc               | Output Duty Cycle; NOTE 3         |                                                    | 48      |         | 52      | %     |
| odc               | Output Duty Cycle; NOTE 4         |                                                    | 45      |         | 55      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. Device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Characterized using a 616Hz bandwidth filter.

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Please refer to the Phase Noise Plot.

NOTE 3: Specified with the VCXO-PLL free running high.

NOTE 4: Specified with the VCXO-PLL locked.

**Table 4B. AC Characteristics,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol         | Parameter                         | Test Conditions                                    | Minimum | Typical | Maximum | Units |
|----------------|-----------------------------------|----------------------------------------------------|---------|---------|---------|-------|
| $f_{REF}$      | Input Reference Frequency         |                                                    |         | 25      |         | MHz   |
|                |                                   |                                                    |         | 125     |         | MHz   |
| $f_{VCO}$      | VCXO-PLL Frequency                |                                                    |         | 25      |         | MHz   |
| $f_{OUT}$      | Output Frequency                  |                                                    |         | 25      |         | MHz   |
| $t_{JIT(CC)}$  | Cycle-to-Cycle Jitter; NOTE 1     |                                                    |         |         | 35      | ps    |
| $t_{jit}$      | RMS Phase Jitter (Random); NOTE 2 | $f_{OUT} = 25MHz$ , Integration Range: 1kHz – 1MHz |         | 0.24    |         | ps    |
| $t_{JIT(PER)}$ | Period jitter                     |                                                    |         |         | 10      | ps    |
| $t_R / t_F$    | Output Rise/Fall Time             | 20% to 80%                                         | 700     |         | 2200    | ps    |
| odc            | Output Duty Cycle; NOTE 3         |                                                    | 48      |         | 52      | %     |
| odc            | Output Duty Cycle; NOTE 4         |                                                    | 44      |         | 56      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. Device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Characterized using a 616Hz bandwidth filter.

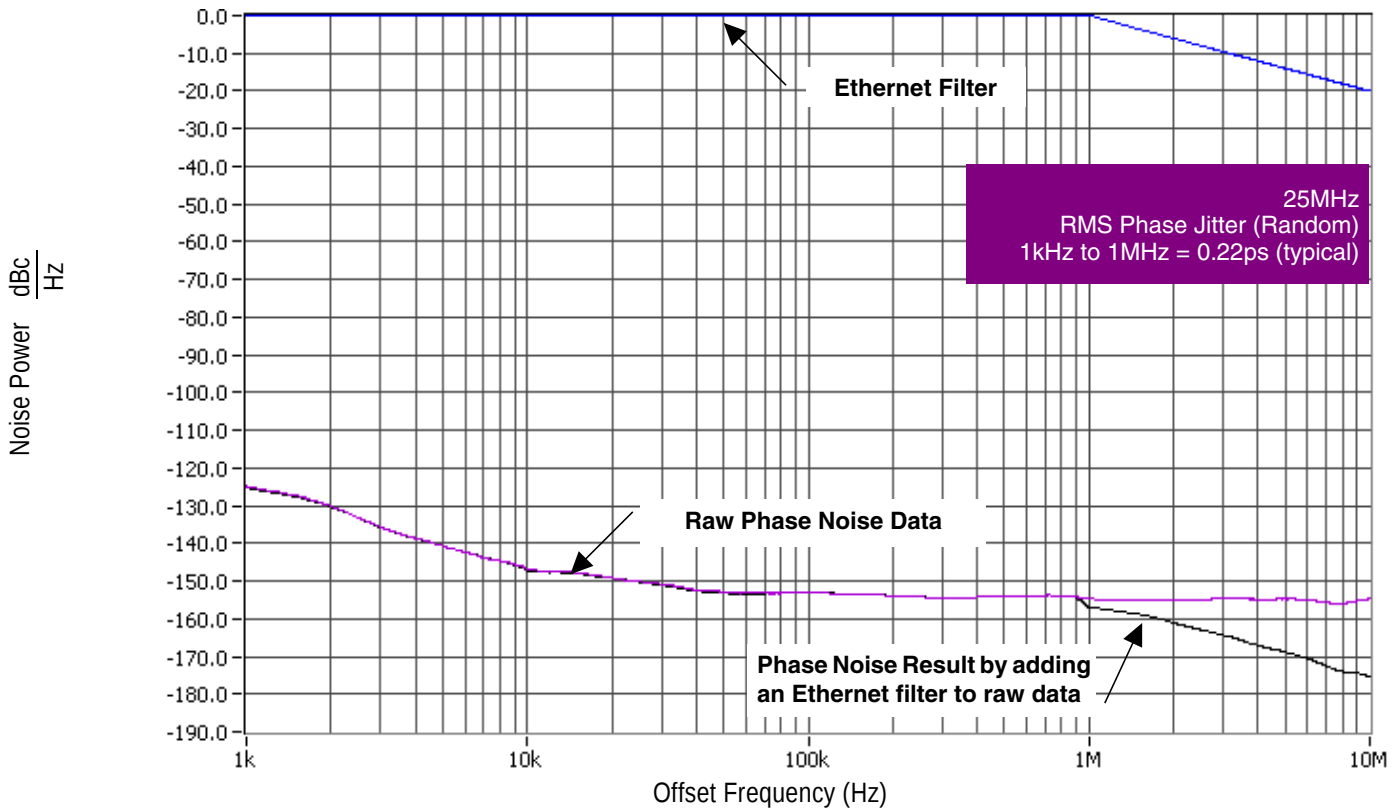
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Please refer to the Phase Noise Plot.

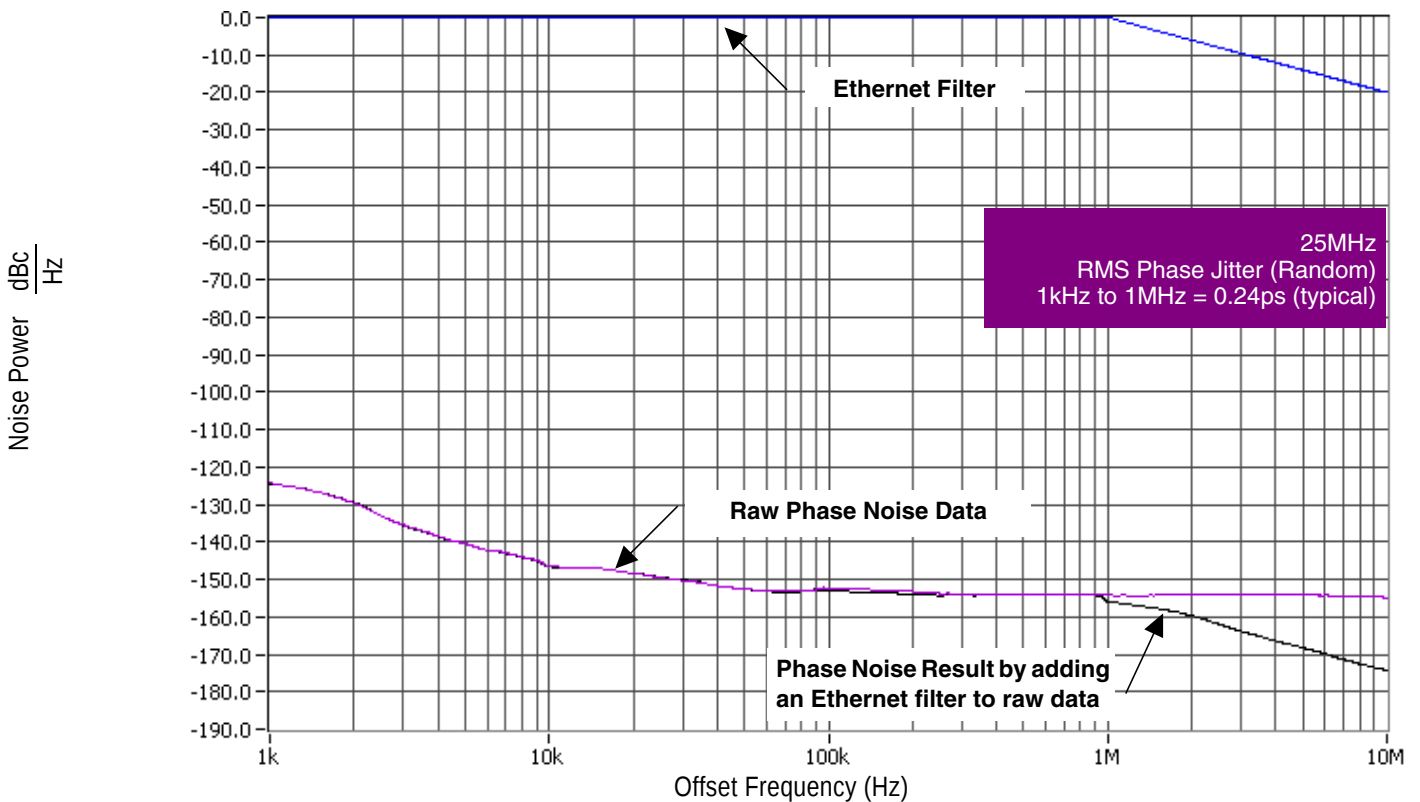
NOTE 3: Specified with the VCXO-PLL free running high.

NOTE 4: Specified with the VCXO-PLL locked.

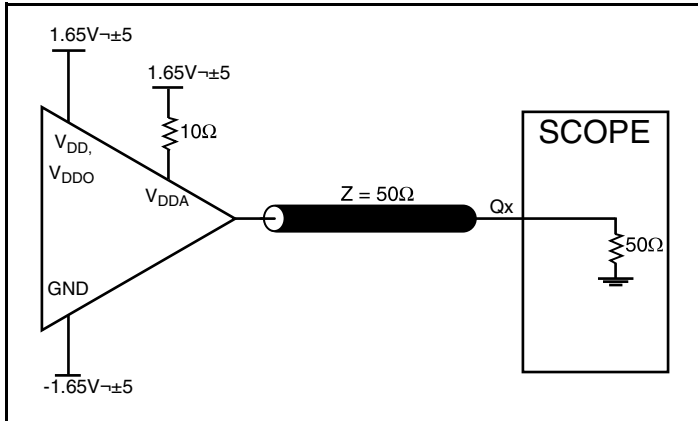
## Typical Phase Noise at 25MHz (3.3V)



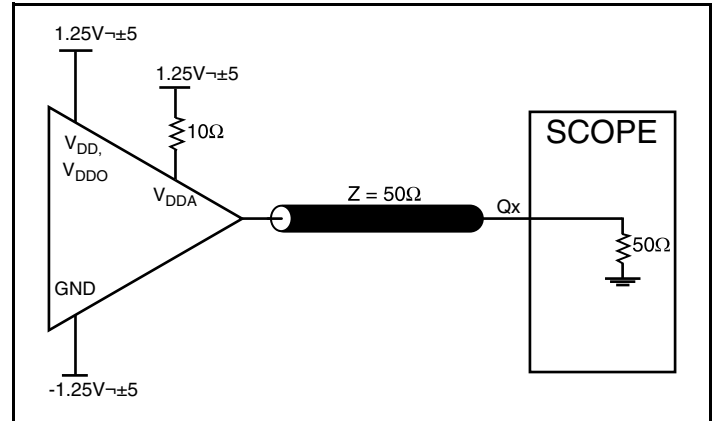
## Typical Phase Noise at 25MHz (2.5V)



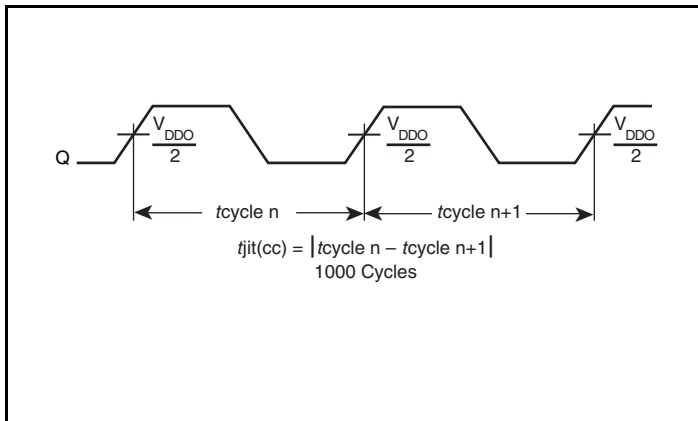
## Parameter Measurement Information



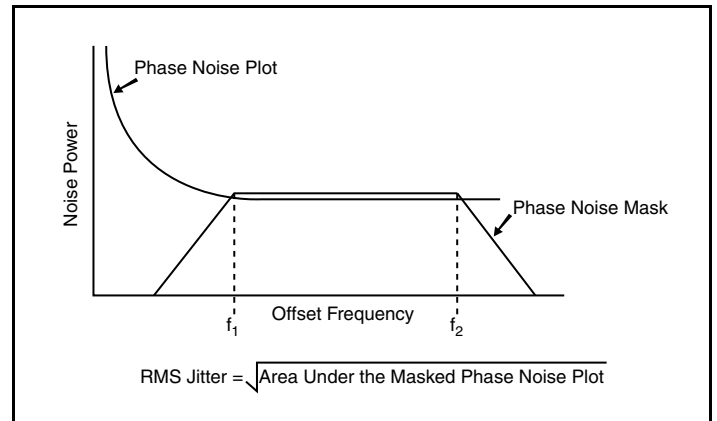
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



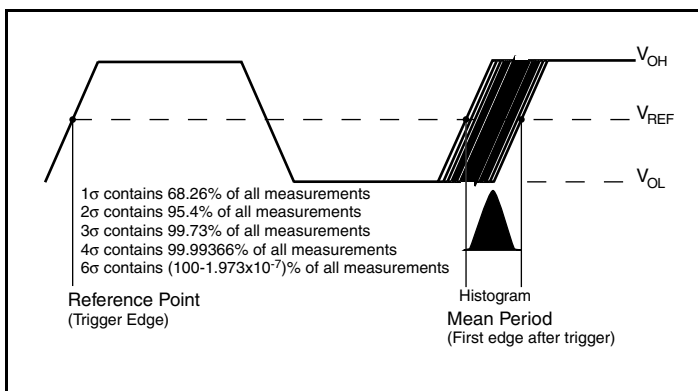
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



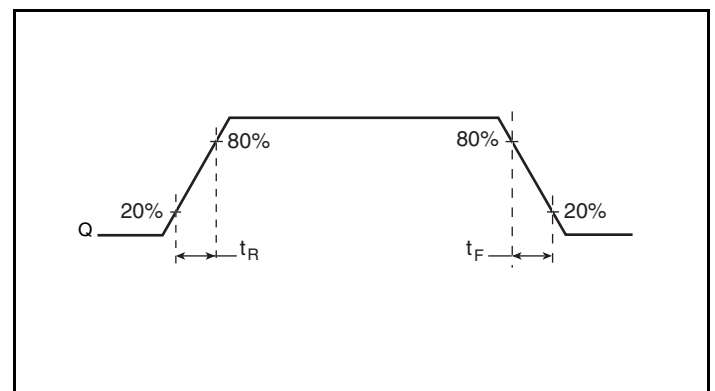
Cycle-to-Cycle Jitter



RMS Phase Jitter

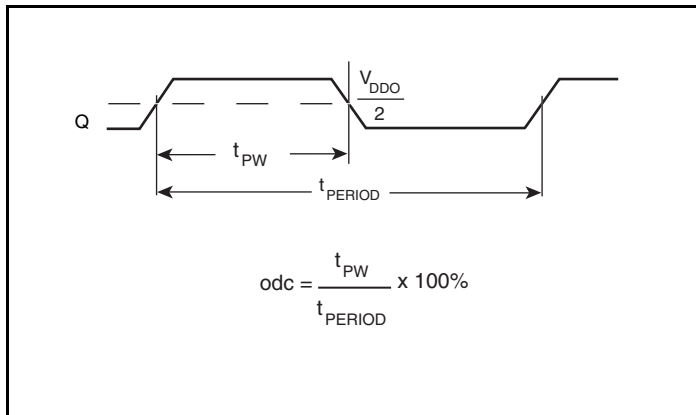


Period Jitter



Output Rise/Fall Time

## Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

## Application Information

### Recommendations for Unused Input Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Figure 1 shows an example of the 810251I application schematic. In this example, the device is operated either at  $V_{DD} = 3.3V$  or  $2.5V$ . The decoupling capacitors should be located as close as possible to the power pin. The input is driven by an LVCMOS driver. An optional

Revision B March 3, 2016

## VCXO-PLL EXTERNAL COMPONENTS

Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance ( $C_L$ ). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note*.

The crystal's load capacitance  $C_L$  characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors ( $C_{TUNE}$ ).

If the crystal  $C_L$  is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal  $C_L$  is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of  $C_L$  is dependant on the characteristics of the VCXO. The recommended  $C_L$  in the *Crystal Parameter Table* balances the tuning range by centering the tuning curve.

### VCXO Characteristics Table

| Symbol        | Parameter                 | Typical | Units |
|---------------|---------------------------|---------|-------|
| $k_{VCXO}$    | VCXO Gain                 | 15000   | Hz/V  |
| $C_{V\_LOW}$  | Low Varactor Capacitance  | 9.8     | pF    |
| $C_{V\_HIGH}$ | High Varactor Capacitance | 22.7    | pF    |

### VCXO-PLL Loop Bandwidth Selection Table

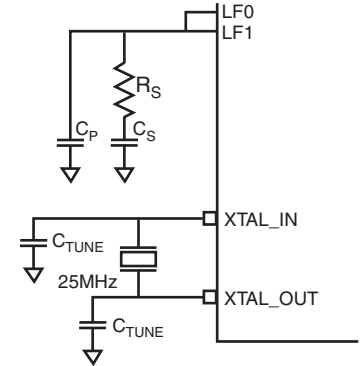
| Bandwidth     | Crystal Frequency (MHz) | $R_S$ (k $\Omega$ ) | $C_S$ ( $\mu$ F) | $C_P$ ( $\mu$ F) |
|---------------|-------------------------|---------------------|------------------|------------------|
| 246Hz (Low)   | 25                      | 0.4                 | 10               | 0.01             |
| 616Hz (Mid)   | 25                      | 1.0                 | 10               | 0.001            |
| 1000Hz (High) | 25                      | 1.65                | 10               | 0.001            |

### Crystal Characteristics

| Symbol      | Parameter                    | Test Conditions | Minimum     | Typical | Maximum          | Units        |
|-------------|------------------------------|-----------------|-------------|---------|------------------|--------------|
|             | Mode of Oscillation          |                 | Fundamental |         |                  |              |
| $f_N$       | Frequency                    |                 |             | 25      |                  | MHz          |
| $f_T$       | Frequency Tolerance          |                 |             |         | $\pm 20$         | ppm          |
| $f_S$       | Frequency Stability          |                 |             |         | $\pm 20$         | ppm          |
|             | Operating Temperature Range  |                 | -40         |         | +85              | $^{\circ}$ C |
| $C_L$       | Load Capacitance             |                 |             | 10      |                  | pF           |
| $C_O$       | Shunt Capacitance            |                 |             | 4       |                  | pF           |
| $C_O / C_1$ | Pullability Ratio            |                 |             | 220     | 240              |              |
| ESR         | Equivalent Series Resistance |                 |             |         | 20               | $\Omega$     |
|             | Drive Level                  |                 |             |         | 1                | mW           |
|             | Aging @ 25 $^{\circ}$ C      |                 |             |         | $\pm 3$ per year | ppm          |

The frequency of oscillation in the third overtone mode is not necessarily at exactly three times the fundamental frequency. The mechanical properties of the quartz element dictate the position of the overtones relative to the fundamental. The oscillator circuit may excite both the fundamental and overtone modes simultaneously. This will cause a nonlinearity in the tuning curve. This potential problem is why VCXO crystals are required to be tested for absence of any activity inside a  $\pm 200$  ppm window at three times the fundamental frequency. Refer to  $F_{L\_3OVT}$  and  $F_{L\_3OVT\_spurs}$  in the crystal Characteristics table.

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



## Power Considerations

This section provides information on power dissipation and junction temperature for the 810251I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 810251I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD} + I_{DDA} + I_{DDO}) = 3.465V * (40mA + 7mA + 5mA) = \mathbf{180.18mW}$
- Output Impedance  $R_{OUT}$  Power Dissipation due to Loading  $50\Omega$  to  $V_{DD}/2$   
Output Current  $I_{OUT} = V_{DD\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 15\Omega)] = \mathbf{26.7mA}$
- Power Dissipation on the  $R_{OUT}$  per LVCMOS output  
Power  $(R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 15\Omega * (26.7mA)^2 = \mathbf{10.7mW}$  per output

### Dynamic Power Dissipation at 25MHz

$$\text{Power (25MHz)} = C_{PD} * \text{Frequency} * (V_{DD})^2 = 8pF * 25MHz * (3.465V)^2 = \mathbf{2.4mW}$$
 per output

### Total Power Dissipation

- Total Power**  
= Power (core)<sub>MAX</sub> + Power ( $R_{OUT}$ ) + Power (25MHz)  
= 180.18mW + 10.7mW + 2.4mW  
= **193.28mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and it directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92.4°C/W per Table 5 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.193W * 92.4^\circ\text{C/W} = 102.8^\circ\text{C}.$$
 This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 5. Thermal Resistance  $\theta_{JA}$  for 16 Lead TSSOP, Forced Convection**

| $\theta_{JA}$ by Velocity                   |          |          |          |
|---------------------------------------------|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 92.4°C/W | 88.0°C/W | 85.9°C/W |

## Reliability Information

Table 6.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead TSSOP

| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---------------------------------------------|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 92.4°C/W | 88.0°C/W | 85.9°C/W |

## Transistor Count

The transistor count for 810251I: 937

## Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

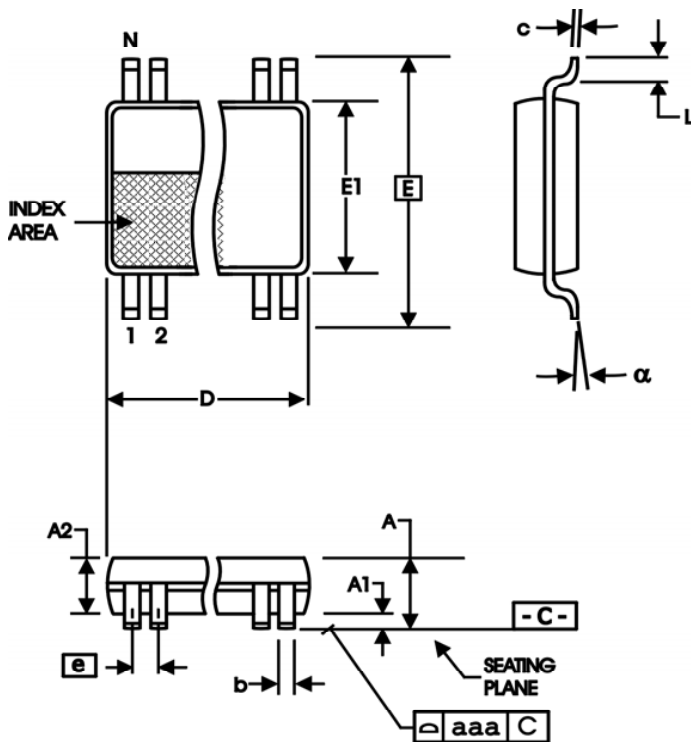


Table 7. Package Dimensions for 16 Lead TSSOP

| All Dimensions in Millimeters |            |         |
|-------------------------------|------------|---------|
| Symbol                        | Minimum    | Maximum |
| N                             | 16         |         |
| A                             |            | 1.20    |
| A1                            | 0.5        | 0.15    |
| A2                            | 0.80       | 1.05    |
| b                             | 0.19       | 0.30    |
| c                             | 0.09       | 0.20    |
| D                             | 4.90       | 5.10    |
| E                             | 6.40 Basic |         |
| E1                            | 4.30       | 4.50    |
| e                             | 0.65 Basic |         |
| L                             | 0.45       | 0.75    |
| $\alpha$                      | 0°         | 8°      |
| aaa                           |            | 0.10    |

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

Table 8. Ordering Information

| Part/Order Number | Marking  | Package                   | Shipping Packaging | Temperature   |
|-------------------|----------|---------------------------|--------------------|---------------|
| 810251AGILF       | 10251AIL | 16 Lead "Lead-Free" TSSOP | Tube               | -40°C to 85°C |
| 810251AGILFT      | 10251AIL | 16 Lead "Lead-Free" TSSOP | Tape & Reel        | -40°C to 85°C |

## Revision History Sheet

| Rev | Table | Page | Description of Change                                                                                                                                                              | Date      |
|-----|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| A   | T8    | 1    | Updated Figure 1, Schematic layout.                                                                                                                                                | 7/28/09   |
|     |       | 10   | VCXO-PLL External Components section, reworded second from last paragraph "The frequency of oscillation in the third overtone mode....".                                           |           |
|     |       | 14   | Changed marking from 810251AL to 10251AL.<br>Changed datasheet header/footer format.                                                                                               |           |
| B   | T4A   | 1    | Features List: deleted 'Absolute pull range is $\pm 50$ ppm (using the internal oscillator)'                                                                                       | 7/17/2012 |
|     |       | 4    | 3.3V AC Characteristics Table - Added additional odc row with specs of 45min and 55max.<br>Added Notes 3 & 4.                                                                      |           |
|     | T4B   | 5    | 2.5V AC Characteristics Table - Added additional odc row with specs of 44min and 56max.<br>Added Notes 3 & 4.<br>HiPerClock references have been deleted throughout the datasheet. |           |
| B   | T4A   | 4    | Added 'high' to Note 3.                                                                                                                                                            | 10/5/2012 |
|     | T4B   | 5    | Added 'high' to Note 3.                                                                                                                                                            |           |
|     | T8    | 13   | Deleted quantity from Tape and Reel.                                                                                                                                               |           |
| B   |       |      | Removed ICS from the part number where needed.<br>Updated data sheet header and footer.                                                                                            | 3/3/16    |

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