S2060

APPLICATION NOTE

Application Notes and Reference Diagrams

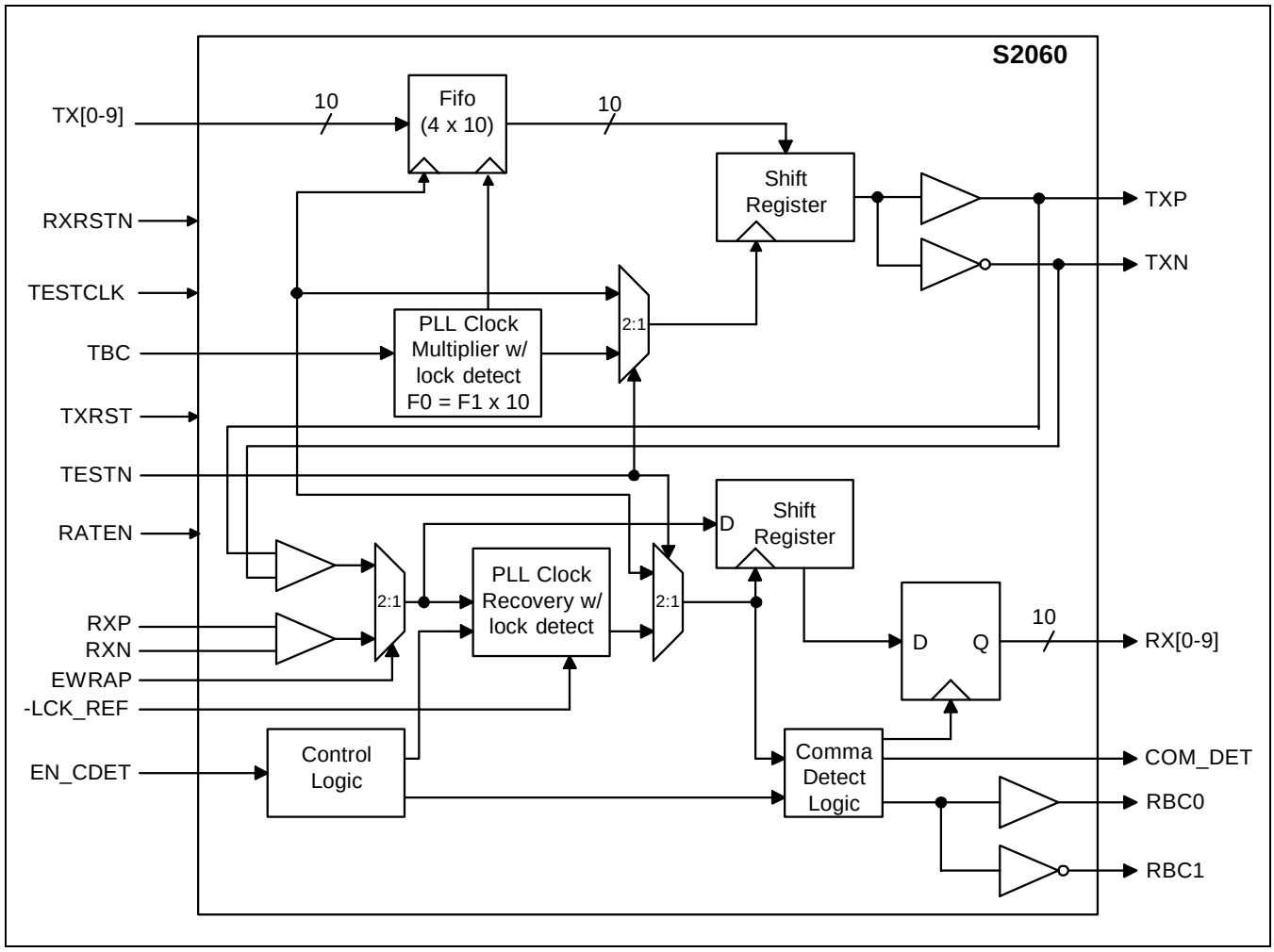
INTRODUCTION

The S2060 transmitter and receiver chip facilitates high-speed serial transmission of data over fiber optic, coax, or twinax interfaces. The device conforms to the requirements of the IEEE 802.3z Gigabit Ethernet specification, and runs at 1.25 Gbps data rates with an associated 10-bit data word. The S2060 is capable of driving up to 30 meters of Twinax cable directly.

The chip provides parallel-to-serial and serial-to-parallel conversion, clock generation/recovery, and framing for block encoded data. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip receive PLL performs clock recovery and data re-timing on the serial bit stream. The transmitter and receiver each support differential LVPECL compatible I/O for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a 3.3 V power supply.

The S2060 can be used for a variety of applications including Gigabit Ethernet, serial backplanes, and proprietary point-to-point links. Figure 1 shows the functional block diagram.

Figure 1. Functional Block Diagram



Power and Ground Connections

Recommended power and ground connections are shown below in Figure 2 and Table 1.

Figure 2. Power and Ground Connections

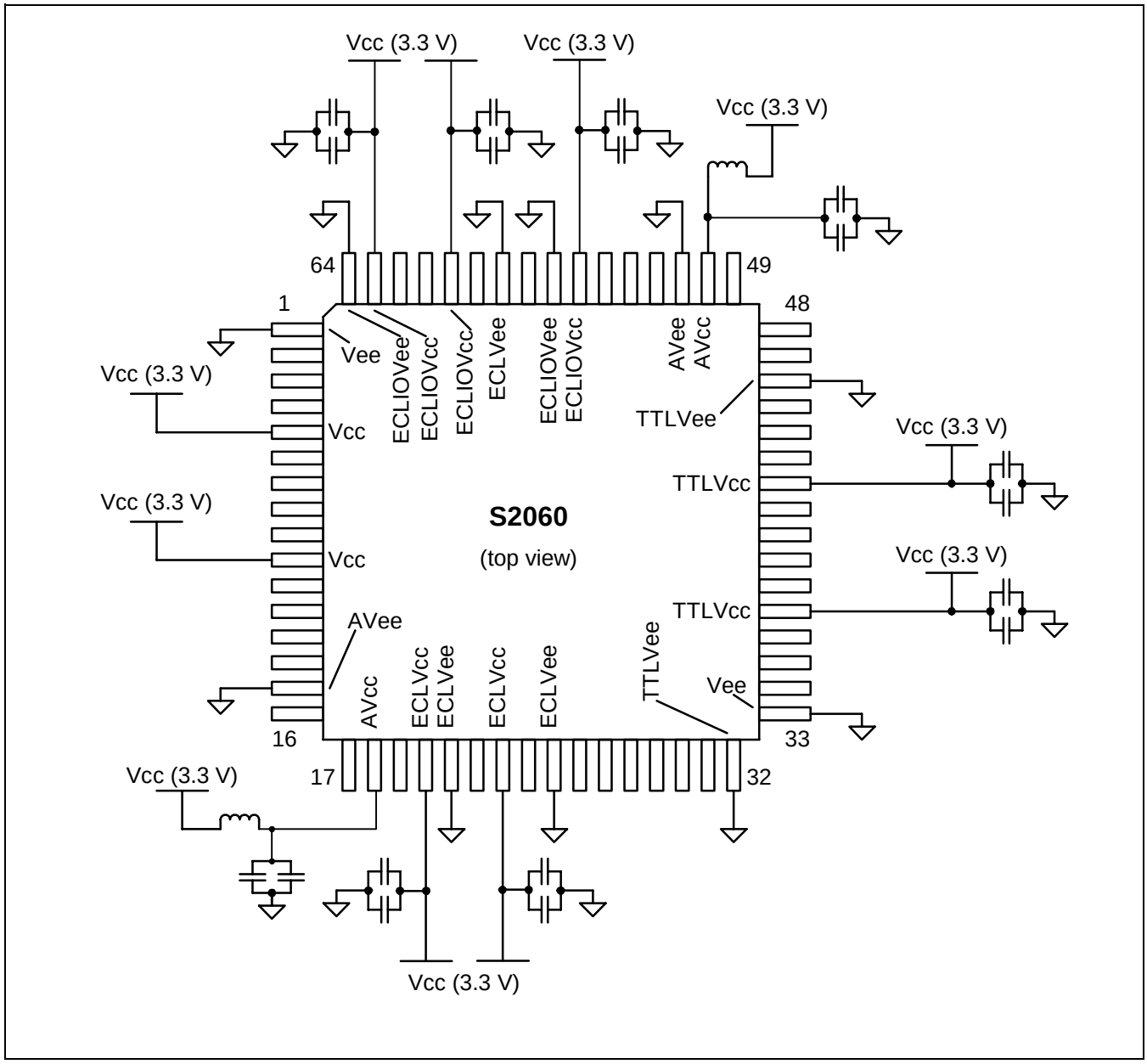


Table 1. Power and Ground Application Information

Function	Pinout Name	Instructions
ANALOG	AVCC	Connect to low noise or filtered 3.3 V supply through a ferrite bead (600 Ω at 100 MHz: Murrata BLM31B601S or equivalent). Provide dual local HF bypassing to AVEE (0.1 µF, 100 pf) for low inductance and resistance. A single low inductance 0.1 µF capacitor can be substituted for the pair (Vishay VJ0612 or equivalent, < 0.5 nH max inductance).
	AVEE	Connect to ground plane.
LVPECL I/O	ECLIOVCC	Provide low impedance connection to 3.3 V. Provide dual local bypassing to GND plane (0.1 µf and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µF cap).
	ECLIOVEE	Connect to ground plane.
CORE	ECLVCC	Provide low impedance connection to 3.3 V. Provide dual local bypassing to GND plane (0.1 µf and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µF cap).
	ECLVEE	Connect to ground plane.
TTL I/O	TTLVCC	Provide low impedance connection to 3.3 V. Provide dual local bypassing to GND plane (0.1 µF and 100 pf in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µF cap).
	TTLVEE	Connect to ground plane.

Serial Input/Output Connections

Figure 3 shows the basic coupling termination scheme for the S2060 high-speed serial inputs. The serial inputs are internally DC biased to $V_{CC\ -1.3\ V}$. External connections include 0.01 µF AC coupling capacitors and a line-to-line termination resistor. The termination resistor is required for lines lengths greater than ~1 cm. Line lengths greater than ~1 cm exhibit transmission line effects at these high speeds. The termination must match the characteristic impedance of the differential lines to minimize signal reflections. The 100 Ω value shown assumes characteristic line impedance of 50 Ω (if the lines are 75 Ω, the line-to-line termination resistor should be 150 Ω). The AC coupling capacitors allow the DC bias point to be set internally by the input stage. The DC bias can be set externally by implementing a resistor divider network on each line, but this is not recommended since it increases the part count and does not provide performance improvement.

The biasing scheme represented in Figure 3 should be used for copper interface applications. Fiber Optic (FO) transceivers require a different approach. When the fiber is disengaged, the noise from the FO device is often nearly as large in amplitude as a good signal. Figure 4 shows a connection to a fiber optic transceiver. The Loss-of-Signal output of the FO transceiver drives the SYNC_EN and -LCK_REF inputs of the S2060. This ensures that the PLL will lock to the reference clock and the Receive Byte Clock (RBC) output clocks will not stretch due to false comma characters. Alternately, the ASIC controller may govern these inputs.

Figure 5 shows the connection diagram for high-speed serial outputs. The 150 Ω pull-down resistors set the drive current of the output stage. The value of 150 Ω provides compatibility with competing products from other manufacturers. As a CMOS design, the S2060 will perform well with pull-down resistor values as large as 1.5 kΩ, which would reduce power consumption on the board. The output stage can drive 30 meters of twinax cable directly.

Figure 3. High Speed Differential Inputs

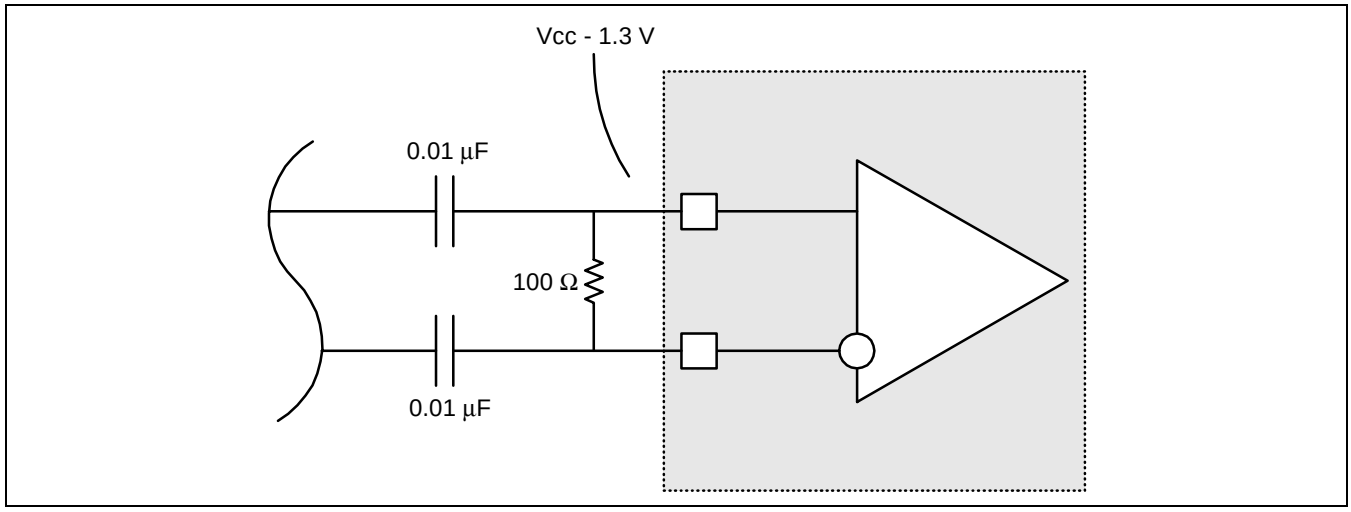


Figure 4. Fiber Optic Transceiver Connection

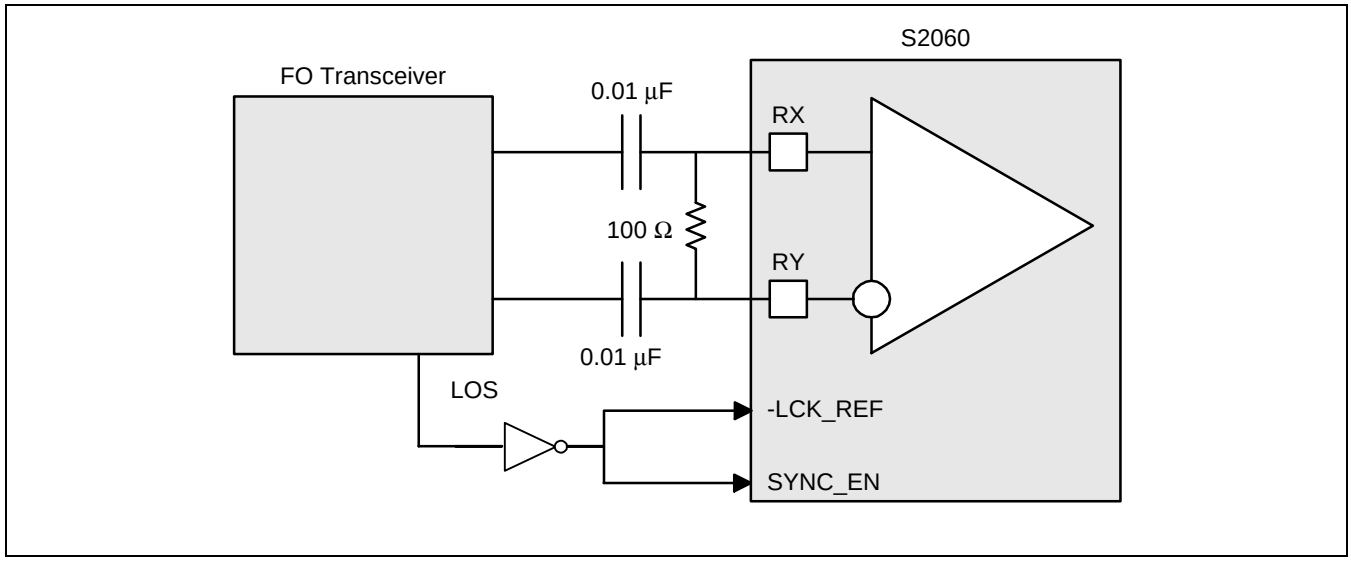
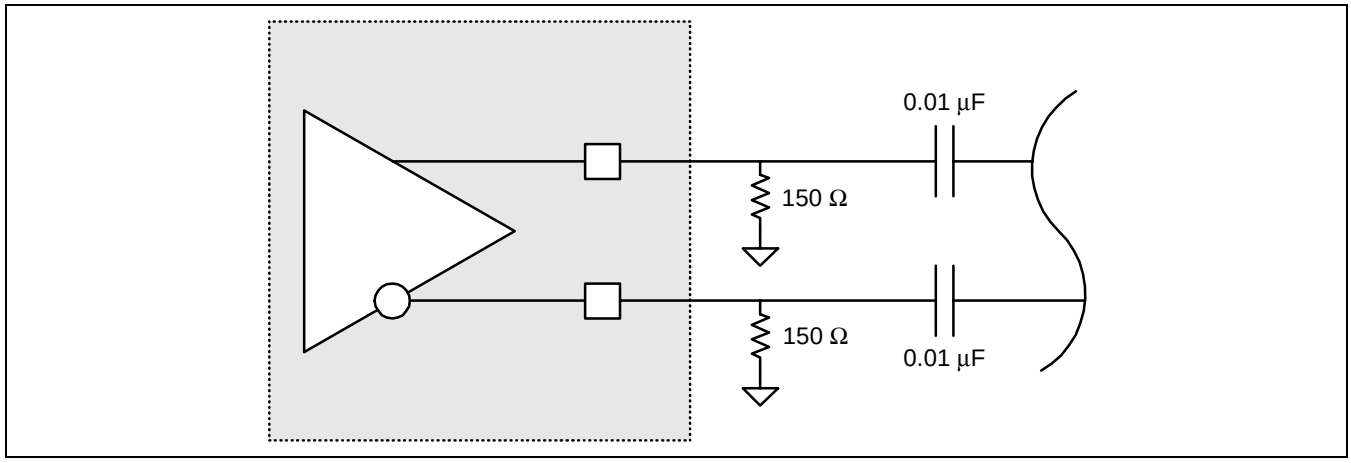


Figure 5. Serial Output Load



Reference Designs

Figure 6 shows a reference design with a 5 V Media Access Controller (MAC). The Transmit Byte Clock (TBC) input to the S2060 will not tolerate signals above the VCC voltage rail, so it may be necessary to reduce the voltage of the TBC output of the MAC. If the output levels are CMOS, set R1 = 180 Ω, R2 = 330 Ω. If the levels out of the MAC are TTL, R1 should be 0 Ω and R2 should be removed. The 43 Ω series resistors on the Transmit (TX) and TBC outputs of the MAC provide 50 Ω termination (43 Ω + ~7 Ω output impedance) for any reflections coming from the S2060 inputs. These resistors should be placed as close to the MAC as possible.

Figure 7 shows the 3.3 V reference design. The difference between the 5.0 V and 3.3 V application is the removal of R1 and R2.

Termination into the Fiber Optic transmitter is shown as 100 Ω line-to-line. Refer to the data sheet or application notes of the chosen FO transmitter for input connection recommendations.

Figure 6. Gigabit Ethernet Application, 5.0 V MAC

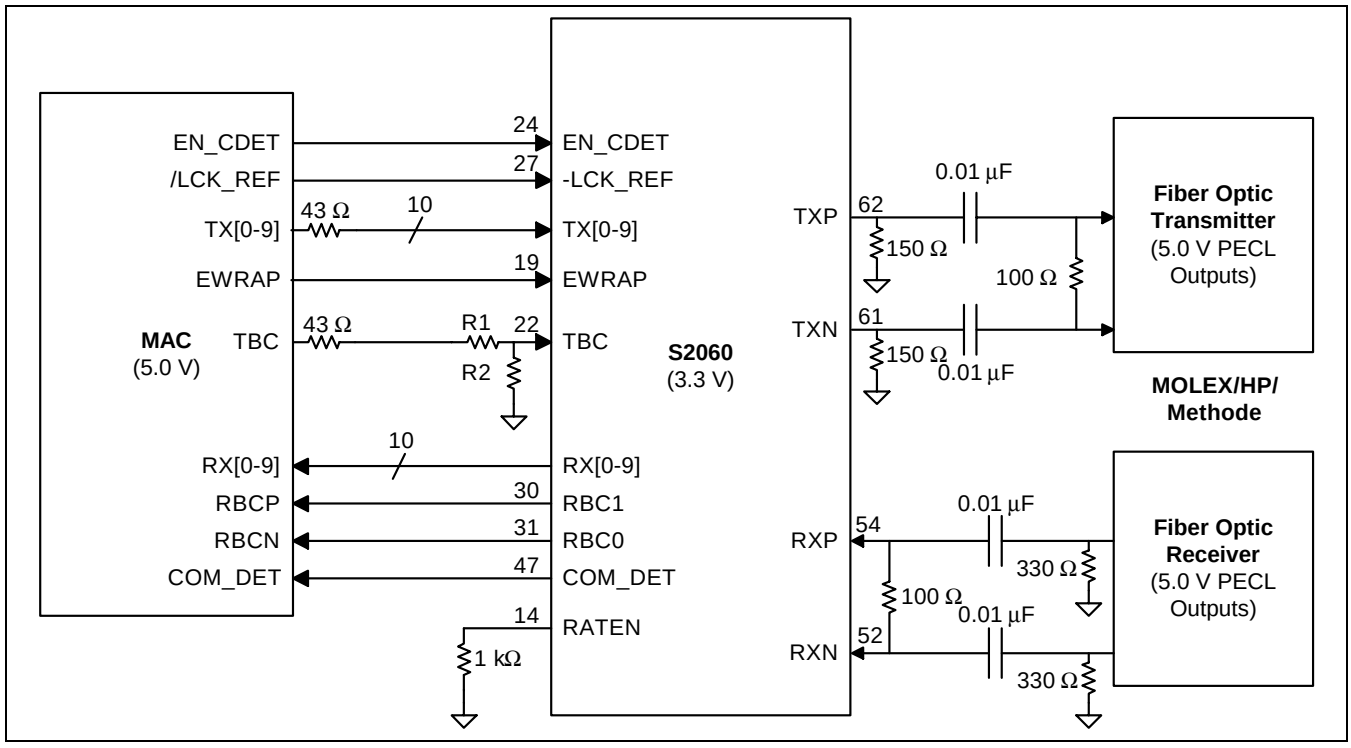
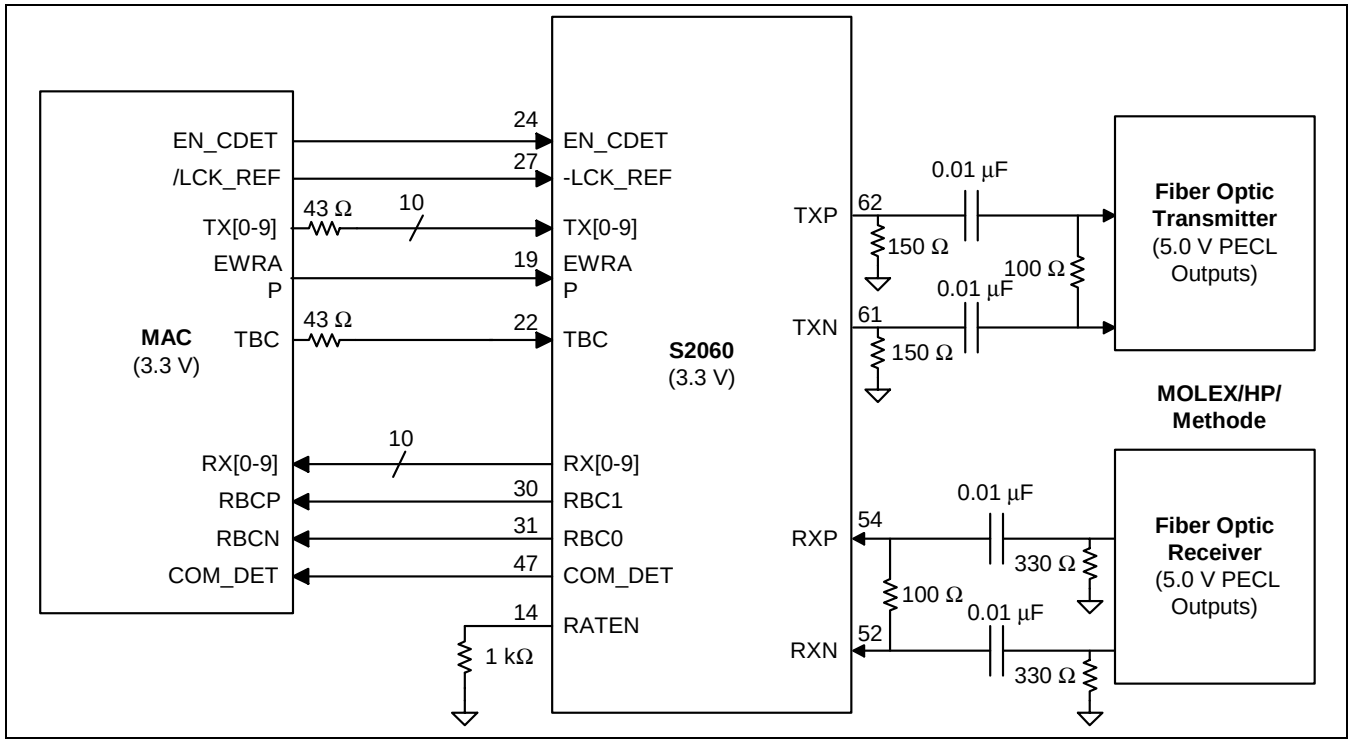


Figure 7. Gigabit Ethernet Application, 3.3 V MAC



S2060 Compatibility with Existing Products

The S2060 is the CMOS equivalent of the S2052. The bulleted items below outline the functional differences between the two parts.

- S2060 typical power dissipation is 660 mW. S2052 dissipates 800 mW.
- S2060 serial input bias voltage is VCC – 1.3 V (standard LVPECL). This complies with both HP and Vitesse. S2052 serial input bias voltage is VCC – 0.65 V.
  With the recommended AC coupled input connection, the bias voltage is irrelevant (see previous section on serial input/output connections) however, designers who wish to set the bias voltage externally should take note of the difference in bias voltage.
- S2060 serial input should not have a pull-up offset resistor.
  S2052 pull-up resistor value is 10 kΩ (for applications where input data goes away).
- When EWRAP is active, TXP/N outputs are static (High). This complies with the S2052. HP holds both pins High. Vitesse holds the P output High and the N output Low.
- S2060 pin 14 is rate selection pin, held Low for normal (full rate) operation. S2052 pin 14 is ground.
- S2060 pin 27 (-LCK_REF) can be either floated or held High to lock to input data (normal operation). S2052 pin 27 (-LCK_REF) must be held high to lock to input data.

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