10 AND 14-OUTPUT LVTTL CLOCK DRIVERS SC3318/68

FEATURES

- **Ten or fourteen clock outputs**
  - Outputs operate at frequencies up to 80 MHz
  - Outputs grouped in two banks of five outputs on SC3318
  - Outputs grouped in a bank of six and a bank of eight outputs on the SC3368
- **All outputs are leading-edge synchronized to within ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 65–75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTL standard**
- **+5V V_{CC} Supply**
- **28 SOIC package**
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

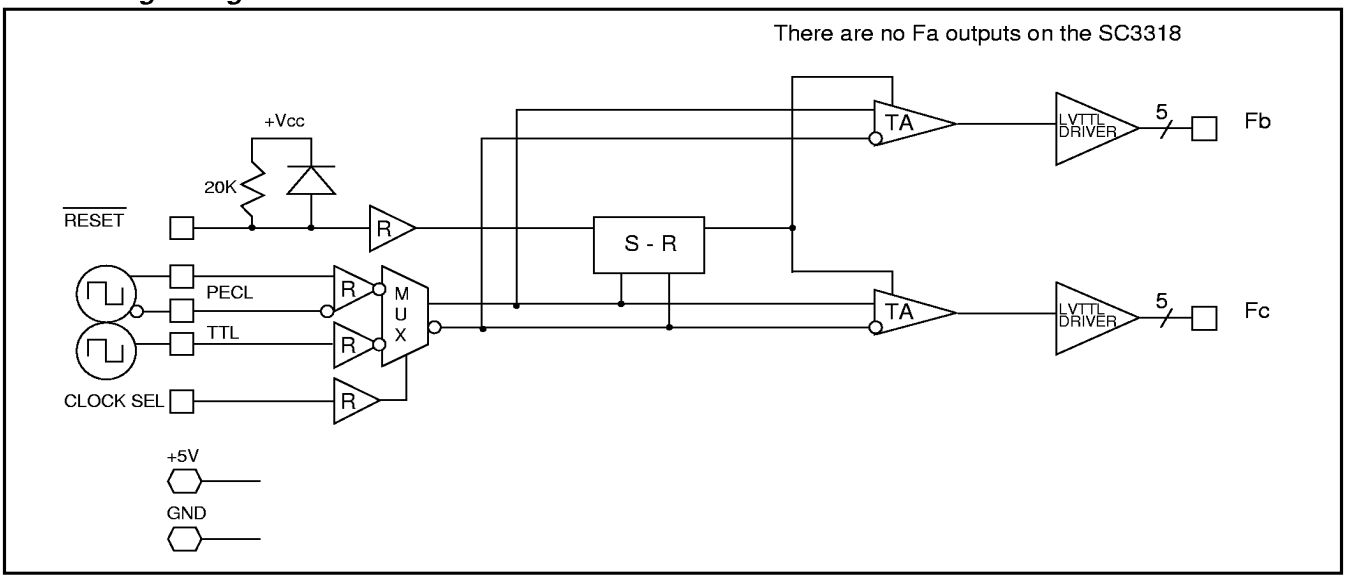
- **Datacom and Telecom networks**
- **Compatible with PowerPC™ processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**
- **Compatible with Intel's Pentium™ and Pentium Pro™ processors**

GENERAL DESCRIPTION

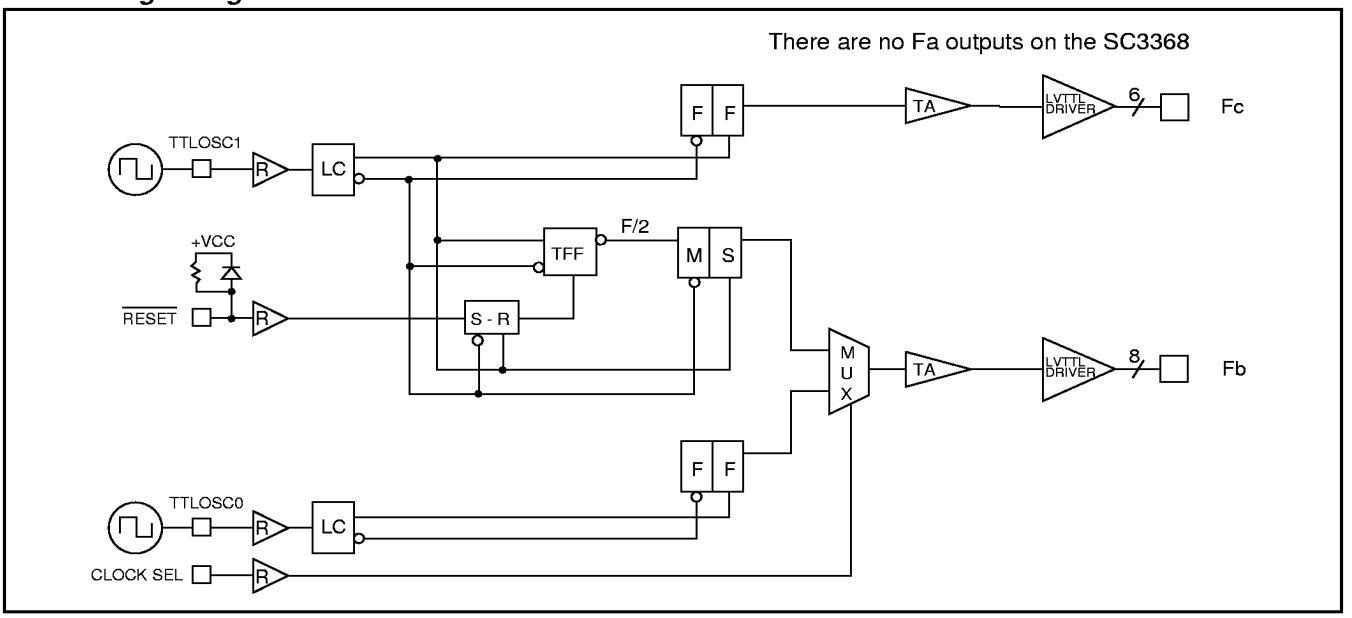
The SC3318 and SC3368 are minimum skew clock drivers with ten or fourteen outputs. They employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground. This reference frequency input is received and distributed to the clock output drivers. All outputs are "clamped" to conform with JEDEC LVTTL levels.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise and distortion.

SC3318 Logic Diagram



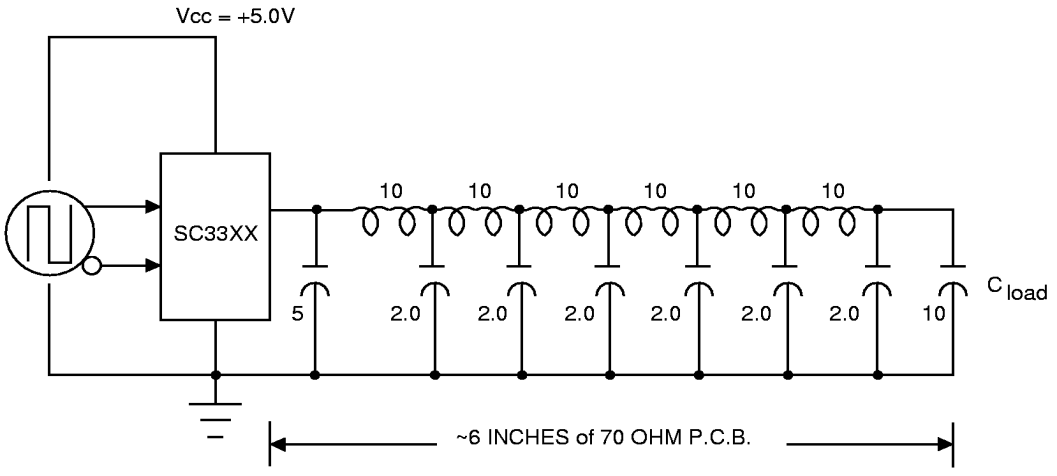
SC3368 Logic Diagram



SC3318/68 Product Selection Guide

	Output Frequency with Respect to Input Frequency				
P/N	**Total Outputs**	**Number of Outputs ÷ 1**	**Number of Outputs ÷ 2**	**Special Features**	**Package**
SC3318	10	10	N/A		28 SOIC
SC3368	14	6	8	Selectable single or dual clock input.	28 SOIC

AC Test/Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

Applied Micro Circuits Corporation
6290 Sequence Dr., San Diego, CA 92121-4358

Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage .....>1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current .....>200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

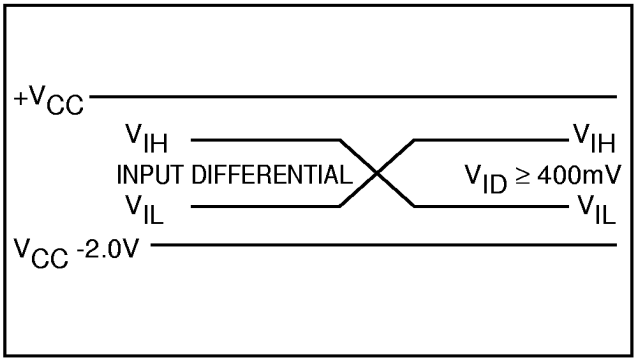
Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference "AC Test/Evaluation Circuit")

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	RESET	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	RESET	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz, C_L = 10pF	2.3	3.65	V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz, C_L = 10pF		0.4V	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-45		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	SC3318, 70°, Typ Pwr=340mW		550	mW
		SC3327, 70˚, Typ Pwr=290mW		475	mW
		SC3367, 70˚, Typ Pwr=250mW		400	mW
		SC3368, 70˚, Typ Pwr=250mW		400	mW

1. Maximum test duration, one second.
2. The SC3318/68 features source series termination of approximately 40 Ohms to assist in matching 65–75 Ohm P.C. board environments.
3. Maximum V_{OH} level is specified at 60˚C and must be derated by 10mV/˚C for T_a > 60˚C.

PECL Differential Input Voltage Range



DC Characteristics

The outputs have been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the output will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -2mA	2.1V	
V_{OL}	I_{OL} = 2mA		0.6V

AC Specifications—Using "AC Test/Evaluation Circuit"

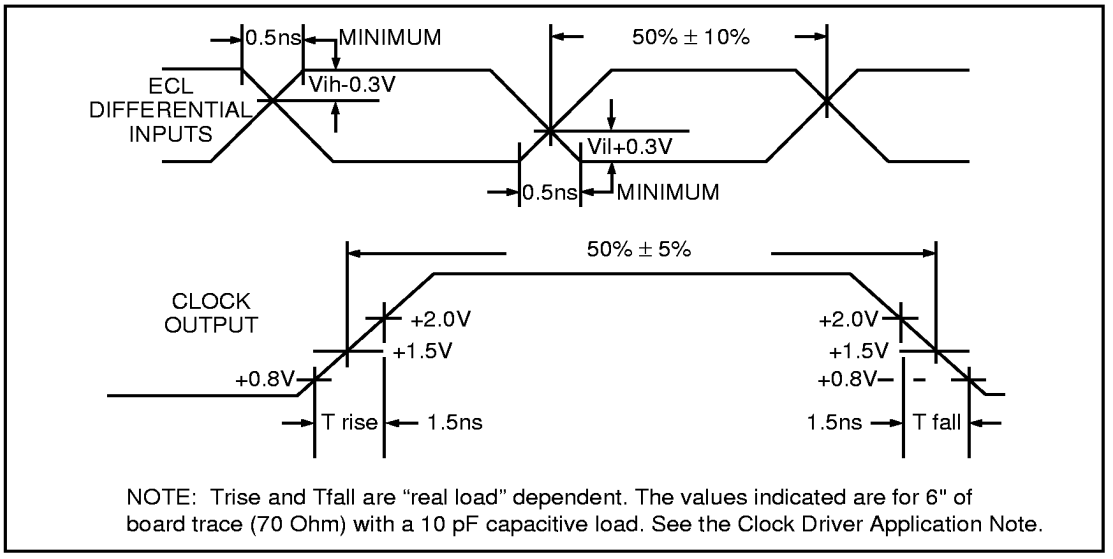
V_{CC} = +5.0V ± 5%, T_a = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3318	SC3368	Units
Maximum Skew Across Fb Outputs	250	500	ps
Maximum Skew Across Fc Outputs	250	250	ps
Maximum Skew Across Fb and Fc Outputs, CLKSEL=0		500	ps
Maximum Skew Across All Outputs Options: Standard –1	— 0.5		ns
Delay of Fb from Fc outputs (CLKSEL = 1) [Tdly or Tcb]	—	Typ. 0.5 Max. 1.0	ns ns
Delay of Fc from Fd outputs [Tdc]	—		ns ns ns
Maximum Output Duty Cycle Asymmetry		Min. 45% Max. 55%	%
Maximum TTL Input Frequency	80	80	MHz
Maximum TTL Output Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	80		MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising and falling edges of all outputs.
2. Output Duty Cycle Asymmetry is defined as the duty cycle deviation from 50%, measured at 1.5V. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "AC Test/Evaluation Circuit." Synchronous outputs may be paralleled for high loads.
5. Parameters guaranteed by design and characterization or tested.

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

Applied Micro Circuits Corporation
6290 Sequence Dr., San Diego, CA 92121-4358

DESCRIPTION OF OPERATION
(Refer to Logic Diagram)

AMCC has developed ten and fourteen-output clock buffer drivers using AMCC's advanced BiCMOS process. These designs have been optimized for minimum skew across all outputs.

The clock source input for these devices may operate between +5V and ground and can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) input levels to AMCC's Clock Drivers. This selection is accomplished by use of the CLKSEL pin (on the SC3318), where logic LOW (or "float") selects TTL and logic HIGH selects PECL. On the SC3368, CLKSEL chooses the source of the clock for the Fb outputs. When CLKSEL is low the TTLOSC0 input drives the Fb outputs and when CLKSEL is high a divide-by-two version of the TTLOSC1 input drives the Fb outputs. This input clock will be fanned out to translation amplifiers and output drivers, refer to the Logic Diagrams. The output duty factor asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs (three falling edge clock inputs for the SC3368). At the expiration of RESET (high) the outputs will resume after four falling edge clock inputs (three falling edge clock inputs for the SC3368), from a high (leading edge) count origin. The reset function is only operational when CLKSEL=1.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 65 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for spice models).

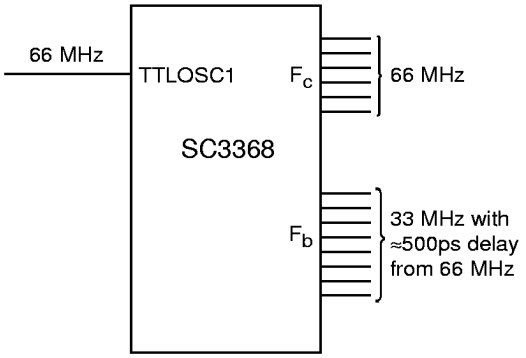
Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the clock drivers will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

SC3368 Application Examples

Example 1.
Low Skew, Single Reference Frequency Mode

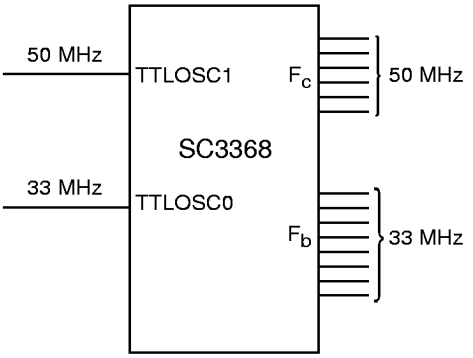
Six outputs at the primary frequency and eight outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈500 ps.



CLKSEL = 1

Example 2.
Dual Reference Frequency Mode, Asynchronous

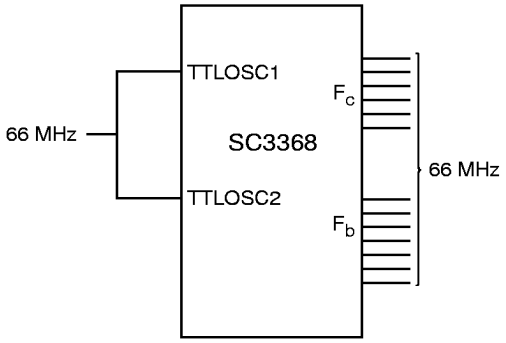
Six outputs at the primary frequency and eight outputs at the secondary frequency.



CLKSEL = 0

Example 3.
Single Reference Frequency Mode, Synchronous

All fourteen outputs will follow the input reference with a maximum skew of 500 ps across all outputs.



CLKSEL = 0

Power Management

The overall goal of managing the power dissipated by the clock driver is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the clock driver is determined by the load that each output drives and the frequency that each output is running. The "Output Power Dissipation" table summarizes these dependencies (see "AC Test/ Evaluation Circuit", for complete load definition).

The output power must be added to the core power (550 mW) of the clock driver to determine the total power being dissipated by the clock driver. This total power is then multiplied by the clock driver's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the clock driver. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the clock driver is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an clock driver with 8 outputs driving 10 pF loads at 66 MHz. Total chip power is calculated as follows:

Core Power (SC3318) = 550 mW

8 outputs, 10 pF, 66 MHz = (8 x 33 mW) = 264 mW
2 outputs, no load, 66 MHz = (2 x 11 mW) = 22 mW

Total Power = 836 mW

The design specifies a 70˚C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7˚C/watt. The clock driver's junction temperature would then be:

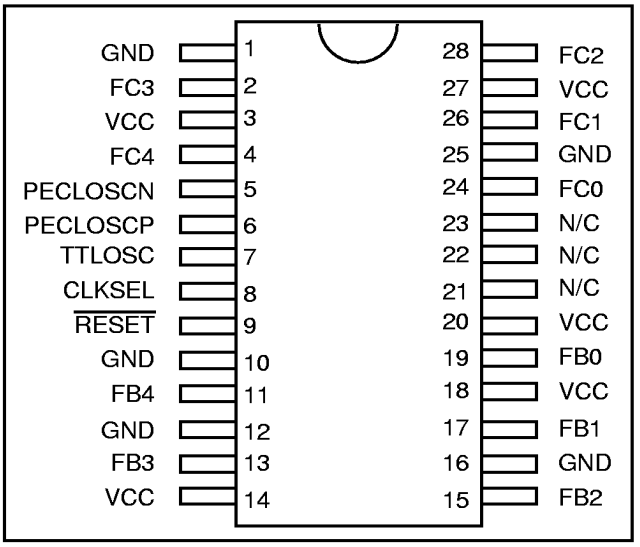
70˚C + (0.836 watts x 57.7˚C/watt) = 118˚C

Note this is below the 140˚C maximum junction temperature.

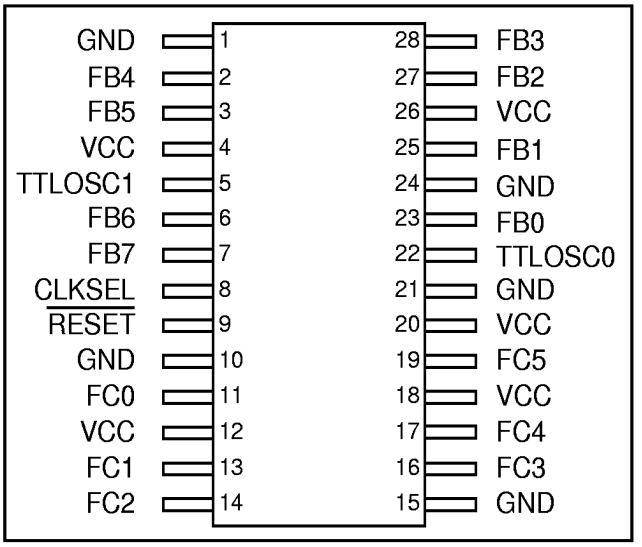
Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

SC3318 Pinout



SC3368 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC33XX **S** **–1** **/TD**

Optional Shipping Configuration
Blank = 25-unit tube
/D = dry pack
/T = tape, reel and dry pack

Skew Option
Blank = standard output-output skew
–1 = 500 ps output-output skew

Package Option
S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC33XXS–1/D
28-pin SOIC package, 500 ps output-output skew, shipped dry packed in the standard tube.

Part Number	Standard	–1
SC3318	N/A	✔
SC3368	✔	N/A

Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121
Phone: (619) 450-9333 • (800) 755-2622 • Fax: (619) 450-9885
http://www.amcc.com

June 25, 1997