

# Low Voltage Precision Adjustable Shunt Regulator

## TLV431, NCV431, SCV431

The TLV431A, B and C series are precision low voltage shunt regulators that are programmable over a wide voltage range of 1.24 V to 16 V. The TLV431A series features a guaranteed reference accuracy of  $\pm 1.0\%$  at 25 °C and  $\pm 2.0\%$  over the entire industrial temperature range of -40 °C to 85 °C. The TLV431B series features higher reference accuracy of  $\pm 0.5\%$  and  $\pm 1.0\%$  respectively. For the TLV431C series, the accuracy is even higher. It is  $\pm 0.2\%$  and  $\pm 1.0\%$  respectively. These devices exhibit a sharp low current turn-on characteristic with a low dynamic impedance of 0.20  $\Omega$  over an operating current range of 100  $\mu$ A to 20 mA. This combination of features makes this series an excellent replacement for zener diodes in numerous applications circuits that require a precise reference voltage. When combined with an optocoupler, the TLV431A/B/C can be used as an error amplifier for controlling the feedback loop in isolated low output voltage (3.0 V to 3.3 V) switching power supplies. These devices are available in economical TO-92-3 and micro size TSOP-5 and SOT-23-3 packages.

### Features

- Programmable Output Voltage Range of 1.24 V to 16 V
- Voltage Reference Tolerance  $\pm 1.0\%$  for A Series,  $\pm 0.5\%$  for B Series and  $\pm 0.2\%$  for C Series
- Sharp Low Current Turn-On Characteristic
- Low Dynamic Output Impedance of 0.20  $\Omega$  from 100  $\mu$ A to 20 mA
- Wide Operating Current Range of 50  $\mu$ A to 20 mA
- Micro Miniature TSOP-5, SOT-23-3 and TO-92-3 Packages
- NCV and SCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free and Halide-Free Devices

### Applications

- Low Output Voltage (3.0 V to 3.3 V) Switching Power Supply Error Amplifier
- Adjustable Voltage or Current Linear and Switching Power Supplies
- Voltage Monitoring
- Current Source and Sink Circuits
- Analog and Digital Circuits Requiring Precision References
- Low Voltage Zener Diode Replacements

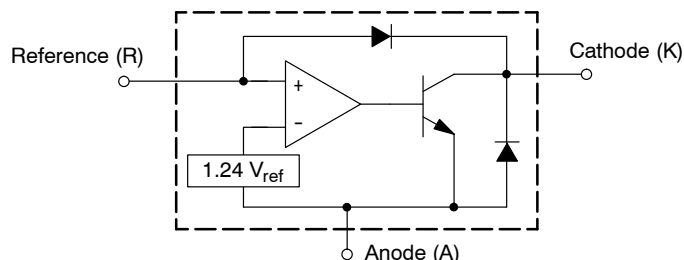
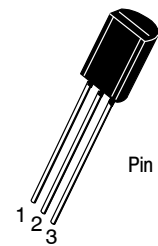
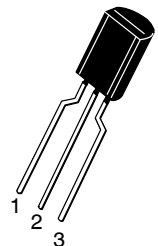


Figure 1. Representative Block Diagram



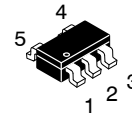
STRAIGHT LEAD  
BULK PACK

TO-92  
LP SUFFIX  
CASE 29-10



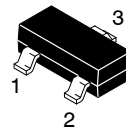
BENT LEAD  
TAPE & REEL  
AMMO PACK

TO-92  
LPRA, LPRE, LPRM,  
LPRP SUFFIX  
CASE 29-10



Pin 1. NC  
2. NC  
3. Cathode  
4. Reference  
5. Anode

TSOP-5  
SN SUFFIX  
CASE 483



Pin 1. Reference  
2. Cathode  
3. Anode

SOT-23  
SN1 SUFFIX  
CASE 318

### ORDERING INFORMATION

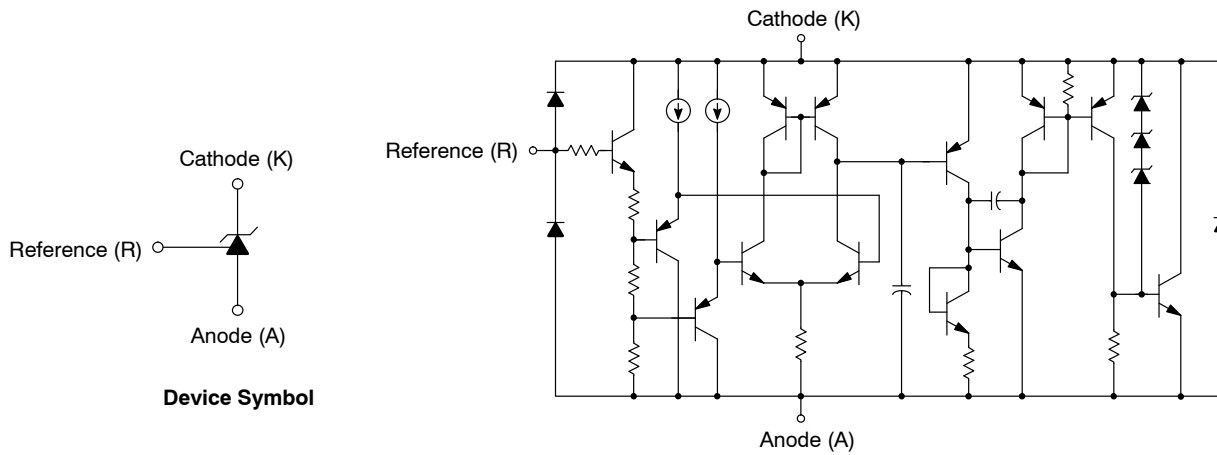
See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 14.

### DEVICE MARKING INFORMATION AND PIN CONNECTIONS

See general marking information in the device marking section on page 13 of this data sheet.

# TLV431, NCV431, SCV431



**Figure 2. Representative Device Symbol and Schematic Diagram**

## MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted)

| Rating                                    | Symbol          | Value                   | Unit                 |
|-------------------------------------------|-----------------|-------------------------|----------------------|
| Cathode to Anode Voltage                  | $V_{KA}$        | 18                      | V                    |
| Cathode Current Range, Continuous         | $I_K$           | -20 to 25               | mA                   |
| Reference Input Current Range, Continuous | $I_{ref}$       | -0.05 to 10             | mA                   |
| Thermal Characteristics                   |                 |                         | $^{\circ}\text{C/W}$ |
| LP Suffix Package, TO-92-3 Package        |                 |                         |                      |
| Thermal Resistance, Junction-to-Ambient   | $R_{\theta JA}$ | 178                     |                      |
| Thermal Resistance, Junction-to-Case      | $R_{\theta JC}$ | 83                      |                      |
| SN Suffix Package, TSOP-5 Package         |                 |                         |                      |
| Thermal Resistance, Junction-to-Ambient   | $R_{\theta JA}$ | 226                     |                      |
| SN1 Suffix Package, SOT-23-3 Package      |                 |                         |                      |
| Thermal Resistance, Junction-to-Ambient   | $R_{\theta JA}$ | 491                     |                      |
| Operating Junction Temperature            | $T_J$           | 150                     | $^{\circ}\text{C}$   |
| Operating Ambient Temperature Range       | $T_A$           | -40 to 85<br>-40 to 125 | $^{\circ}\text{C}$   |
| Storage Temperature Range                 | $T_{stg}$       | -65 to 150              | $^{\circ}\text{C}$   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per JEDEC JESD22-A114F, Machine Model Method 200 V per JEDEC JESD22-A115C, Charged Device Method 1000 V per JEDEC JESD22-C101E. This device contains latch-up protection and exceeds  $\pm 100$  mA per JEDEC standard JESD78.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

## RECOMMENDED OPERATING CONDITIONS

| Condition                | Symbol   | Min       | Max | Unit |
|--------------------------|----------|-----------|-----|------|
| Cathode to Anode Voltage | $V_{KA}$ | $V_{ref}$ | 16  | V    |
| Cathode Current          | $I_K$    | 0.1       | 20  | mA   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# TLV431, NCV431, SCV431

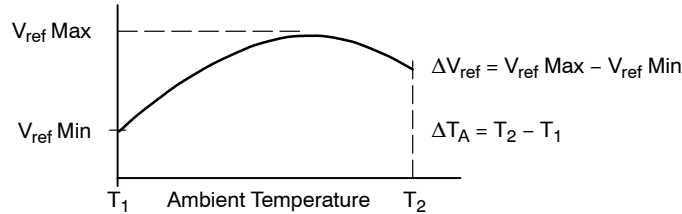
## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)

| Characteristic                                                                                                                                                                                         | Symbol                                 | TLV431A        |               |                | TLV431B        |               |                | Unit           |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|----------------|---------------|----------------|----------------|---------------|----------------|----------------|
|                                                                                                                                                                                                        |                                        | Min            | Typ           | Max            | Min            | Typ           | Max            |                |
| Reference Voltage (Figure 3)<br>(V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = 25 °C)<br>(T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> , Note 1)             | V <sub>ref</sub>                       | 1.228<br>1.215 | 1.240<br>–    | 1.252<br>1.265 | 1.234<br>1.228 | 1.240<br>–    | 1.246<br>1.252 | V              |
| Reference Input Voltage Deviation Over Temperature (Figure 3)<br>(V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> , Notes 1, 2, 3) | ΔV <sub>ref</sub>                      | –              | 7.2           | 20             | –              | 7.2           | 20             | mV             |
| Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4)<br>(V <sub>KA</sub> = V <sub>ref</sub> to 16 V, I <sub>K</sub> = 10 mA)                                                  | $\frac{\Delta V_{ref}}{\Delta V_{KA}}$ | –              | –0.6          | –1.5           | –              | –0.6          | –1.5           | $\frac{mV}{V}$ |
| Reference Terminal Current (Figure 4)<br>(I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open)                                                                                                               | I <sub>ref</sub>                       | –              | 0.15          | 0.3            | –              | 0.15          | 0.3            | μA             |
| Reference Input Current Deviation Over Temperature (Figure 4)<br>(I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open, Notes 1, 2, 3)                                                                        | ΔI <sub>ref</sub>                      | –              | 0.04          | 0.08           | –              | 0.04          | 0.08           | μA             |
| Minimum Cathode Current for Regulation (Figure 3)                                                                                                                                                      | I <sub>K(min)</sub>                    | –              | 30            | 80             | –              | 30            | 80             | μA             |
| Off-State Cathode Current (Figure 5)<br>(V <sub>KA</sub> = 6.0 V, V <sub>ref</sub> = 0)<br>(V <sub>KA</sub> = 16 V, V <sub>ref</sub> = 0)                                                              | I <sub>K(off)</sub>                    | –<br>–         | 0.01<br>0.012 | 0.04<br>0.05   | –<br>–         | 0.01<br>0.012 | 0.04<br>0.05   | μA             |
| Dynamic Impedance (Figure 3)<br>(V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 4)                                                                           | Z <sub>KA</sub>                        | –              | 0.25          | 0.4            | –              | 0.25          | 0.4            | Ω              |

1. Ambient temperature range: T<sub>low</sub> = –40 °C, T<sub>high</sub> = 85 °C.

2. Guaranteed but not tested.

3. The deviation parameters ΔV<sub>ref</sub> and ΔI<sub>ref</sub> are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

$$\alpha V_{ref} \left( \frac{ppm}{^{\circ}C} \right) = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} (T_A = 25^{\circ}C)} \times 10^6 \right)}{\Delta T_A}$$

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV<sub>ref</sub> = 7.2 mV and the slope is positive,

$$V_{ref} @ 25^{\circ}C = 1.241 V$$

$$\Delta T_A = 125^{\circ}C$$

$$\alpha V_{ref} \left( \frac{ppm}{^{\circ}C} \right) = \frac{0.0072 \times 10^6}{1.241 \times 125} = 46 ppm/^{\circ}C$$

4. The dynamic impedance Z<sub>KA</sub> is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left( 1 + \frac{R1}{R2} \right)$$

# TLV431, NCV431, SCV431

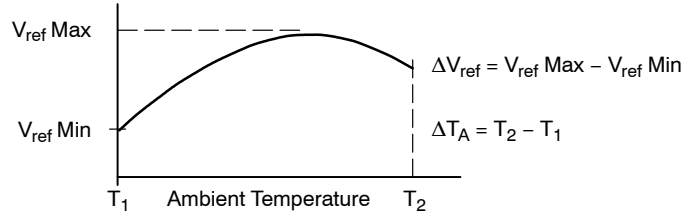
## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)

| Characteristic                                                                                                                                                                                         | Symbol                                 | TLV431C        |               |                | Unit           |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|----------------|---------------|----------------|----------------|
|                                                                                                                                                                                                        |                                        | Min            | Typ           | Max            |                |
| Reference Voltage (Figure 3)<br>(V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = 25 °C)<br>(T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> , Note 5)             | V <sub>ref</sub>                       | 1.237<br>1.228 | 1.240<br>–    | 1.243<br>1.252 | V              |
| Reference Input Voltage Deviation Over Temperature (Figure 3)<br>(V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 10 mA, T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub> , Notes 5, 6, 7) | ΔV <sub>ref</sub>                      | –              | 7.2           | 20             | mV             |
| Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4)<br>(V <sub>KA</sub> = V <sub>ref</sub> to 16 V, I <sub>K</sub> = 10 mA)                                                  | $\frac{\Delta V_{ref}}{\Delta V_{KA}}$ | –              | –0.6          | –1.5           | $\frac{mV}{V}$ |
| Reference Terminal Current (Figure 4)<br>(I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open)                                                                                                               | I <sub>ref</sub>                       | –              | 0.15          | 0.3            | μA             |
| Reference Input Current Deviation Over Temperature (Figure 4)<br>(I <sub>K</sub> = 10 mA, R1 = 10 kΩ, R2 = open, Notes 5, 6, 7)                                                                        | ΔI <sub>ref</sub>                      | –              | 0.04          | 0.08           | μA             |
| Minimum Cathode Current for Regulation (Figure 3)                                                                                                                                                      | I <sub>K(min)</sub>                    | –              | 30            | 80             | μA             |
| Off-State Cathode Current (Figure 5)<br>(V <sub>KA</sub> = 6.0 V, V <sub>ref</sub> = 0)<br>(V <sub>KA</sub> = 16 V, V <sub>ref</sub> = 0)                                                              | I <sub>K(off)</sub>                    | –<br>–         | 0.01<br>0.012 | 0.04<br>0.05   | μA             |
| Dynamic Impedance (Figure 3)<br>(V <sub>KA</sub> = V <sub>ref</sub> , I <sub>K</sub> = 0.1 mA to 20 mA, f ≤ 1.0 kHz, Note 8)                                                                           | Z <sub>KA</sub>                        | –              | 0.25          | 0.4            | Ω              |

5. Ambient temperature range: T<sub>low</sub> = –40 °C, T<sub>high</sub> = 85 °C.

6. Guaranteed but not tested.

7. The deviation parameters ΔV<sub>ref</sub> and ΔI<sub>ref</sub> are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage, αV<sub>ref</sub> is defined as:

$$\alpha V_{ref} \left( \frac{ppm}{^{\circ}C} \right) = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} (T_A = 25^{\circ}C)} \times 10^6 \right)}{\Delta T_A}$$

αV<sub>ref</sub> can be positive or negative depending on whether V<sub>ref</sub> Min or V<sub>ref</sub> Max occurs at the lower ambient temperature, refer to Figure 8.

Example: ΔV<sub>ref</sub> = 7.2 mV and the slope is positive,

$$V_{ref} @ 25^{\circ}C = 1.241 V$$

$$\Delta T_A = 125^{\circ}C$$

$$\alpha V_{ref} \left( \frac{ppm}{^{\circ}C} \right) = \frac{0.0072 \times 10^6}{1.241 \times 125} = 46 ppm/^{\circ}C$$

8. The dynamic impedance Z<sub>KA</sub> is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors, R1 and R2, (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left( 1 + \frac{R1}{R2} \right)$$

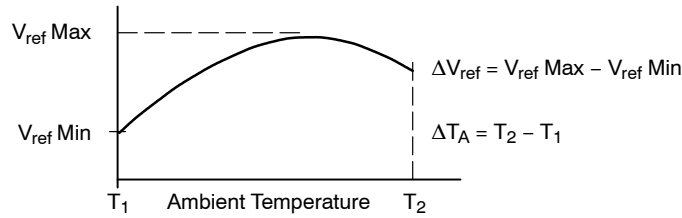
# TLV431, NCV431, SCV431

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted. NCV prefix indicates TSOP package device. SCV prefix indicates SOT-23 package device.)

| Characteristic                                                                                                                                                                                                                                                                                                                                       | Symbol                                 | NCV431A, SCV431A        |                 |                         | Unit                         |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|-------------------------|-----------------|-------------------------|------------------------------|
|                                                                                                                                                                                                                                                                                                                                                      |                                        | Min                     | Typ             | Max                     |                              |
| Reference Voltage (Figure 3)<br>( $V_{KA} = V_{ref}$ , $I_K = 10\text{ mA}$ , $T_A = 25^\circ\text{C}$ )<br>( $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ )<br>( $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ )                                                                                                                              | $V_{ref}$                              | 1.228<br>1.215<br>1.211 | 1.240<br>–<br>– | 1.252<br>1.265<br>1.265 | V                            |
| Reference Input Voltage Deviation Over Temperature (Figure 3)<br>( $V_{KA} = V_{ref}$ , $I_K = 10\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , Notes 9, 10)<br>( $V_{KA} = V_{ref}$ , $I_K = 10\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ , Notes 9, 10)                                                       | $\Delta V_{ref}$                       | –<br>–                  | 7.2<br>7.2      | 20<br>24                | mV                           |
| Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4)<br>( $V_{KA} = V_{ref}$ to 16 V, $I_K = 10\text{ mA}$ )                                                                                                                                                                                                                | $\frac{\Delta V_{ref}}{\Delta V_{KA}}$ | –                       | –0.6            | –1.5                    | $\frac{\text{mV}}{\text{V}}$ |
| Reference Terminal Current (Figure 4)<br>( $I_K = 10\text{ mA}$ , $R1 = 10\text{ k}\Omega$ , $R2 = \text{open}$ )                                                                                                                                                                                                                                    | $I_{ref}$                              | –                       | 0.15            | 0.3                     | $\mu\text{A}$                |
| Reference Input Current Deviation Over Temperature (Figure 4)<br>( $I_K = 10\text{ mA}$ , $R1 = 10\text{ k}\Omega$ , $R2 = \text{open}$ , $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , Notes 9, 10)<br>( $I_K = 10\text{ mA}$ , $R1 = 10\text{ k}\Omega$ , $R2 = \text{open}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ , Notes 9, 10) | $\Delta I_{ref}$                       | –<br>–                  | 0.04<br>–       | 0.08<br>0.10            | $\mu\text{A}$                |
| Minimum Cathode Current for Regulation (Figure 3)                                                                                                                                                                                                                                                                                                    | $I_{K(\text{min})}$                    | –                       | 30              | 80                      | $\mu\text{A}$                |
| Off-State Cathode Current (Figure 5)<br>( $V_{KA} = 6.0\text{ V}$ , $V_{ref} = 0$ )<br>( $V_{KA} = 16\text{ V}$ , $V_{ref} = 0$ )                                                                                                                                                                                                                    | $I_{K(\text{off})}$                    | –<br>–                  | 0.01<br>0.012   | 0.04<br>0.05            | $\mu\text{A}$                |
| Dynamic Impedance (Figure 3)<br>( $V_{KA} = V_{ref}$ , $I_K = 0.1\text{ mA}$ to $20\text{ mA}$ , $f \leq 1.0\text{ kHz}$ , Note 11)                                                                                                                                                                                                                  | $ Z_{KA} $                             | –                       | 0.25            | 0.4                     | $\Omega$                     |

9. Guaranteed but not tested.

10. The deviation parameters  $\Delta V_{ref}$  and  $\Delta I_{ref}$  are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage,  $\alpha V_{ref}$  is defined as:

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} (T_A = 25^\circ\text{C})} \times 10^6 \right)}{\Delta T_A}$$

$\alpha V_{ref}$  can be positive or negative depending on whether  $V_{ref} \text{ Min}$  or  $V_{ref} \text{ Max}$  occurs at the lower ambient temperature, refer to Figure 8.

Example:  $\Delta V_{ref} = 7.2\text{ mV}$  and the slope is positive,

$$V_{ref} @ 25^\circ\text{C} = 1.241\text{ V}$$

$$\Delta T_A = 125^\circ\text{C}$$

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{0.0072 \times 10^6}{1.241 \times 125} = 46 \text{ ppm}/^\circ\text{C}$$

11. The dynamic impedance  $Z_{KA}$  is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operating with two external resistors,  $R1$  and  $R2$ , (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left( 1 + \frac{R1}{R2} \right)$$

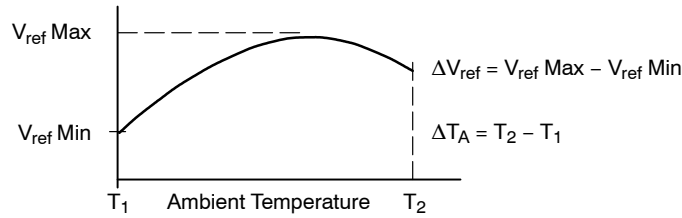
# TLV431, NCV431, SCV431

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted. NCV prefix indicates TSOP package device. SCV prefix indicates SOT-23 package device.)

| Characteristic                                                                                                                                                                                                                                                                                                                                         | Symbol                                 | NCV431B, SCV431B        |                 |                         | Unit                         |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|-------------------------|-----------------|-------------------------|------------------------------|
|                                                                                                                                                                                                                                                                                                                                                        |                                        | Min                     | Typ             | Max                     |                              |
| Reference Voltage (Figure 3)<br>( $V_{KA} = V_{ref}$ , $I_K = 10\text{ mA}$ , $T_A = 25^\circ\text{C}$ )<br>( $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ )<br>( $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ )                                                                                                                                | $V_{ref}$                              | 1.234<br>1.228<br>1.224 | 1.240<br>–<br>– | 1.246<br>1.252<br>1.252 | V                            |
| Reference Input Voltage Deviation Over Temperature (Figure 3)<br>( $V_{KA} = V_{ref}$ , $I_K = 10\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , Notes 9, 10)<br>( $V_{KA} = V_{ref}$ , $I_K = 10\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ , Notes 9, 10)                                                         | $\Delta V_{ref}$                       | –<br>–                  | 7.2<br>7.2      | 20<br>24                | mV                           |
| Ration of Reference Input Voltage Change to Cathode Voltage Change (Figure 4)<br>( $V_{KA} = V_{ref}$ to $16\text{ V}$ , $I_K = 10\text{ mA}$ )                                                                                                                                                                                                        | $\frac{\Delta V_{ref}}{\Delta V_{KA}}$ | –                       | –0.6            | –1.5                    | $\frac{\text{mV}}{\text{V}}$ |
| Reference Terminal Current (Figure 4)<br>( $I_K = 10\text{ mA}$ , $R1 = 10\text{ k}\Omega$ , $R2 = \text{open}$ )                                                                                                                                                                                                                                      | $I_{ref}$                              | –                       | 0.15            | 0.3                     | $\mu\text{A}$                |
| Reference Input Current Deviation Over Temperature (Figure 4)<br>( $I_K = 10\text{ mA}$ , $R1 = 10\text{ k}\Omega$ , $R2 = \text{open}$ , $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , Notes 12, 13)<br>( $I_K = 10\text{ mA}$ , $R1 = 10\text{ k}\Omega$ , $R2 = \text{open}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ , Notes 12, 13) | $\Delta I_{ref}$                       | –<br>–                  | 0.04<br>–       | 0.08<br>0.10            | $\mu\text{A}$                |
| Minimum Cathode Current for Regulation (Figure 3)                                                                                                                                                                                                                                                                                                      | $I_{K(\min)}$                          | –                       | 30              | 80                      | $\mu\text{A}$                |
| Off-State Cathode Current (Figure 5)<br>( $V_{KA} = 6.0\text{ V}$ , $V_{ref} = 0$ )<br>( $V_{KA} = 16\text{ V}$ , $V_{ref} = 0$ )                                                                                                                                                                                                                      | $I_{K(\text{off})}$                    | –<br>–                  | 0.01<br>0.012   | 0.04<br>0.05            | $\mu\text{A}$                |
| Dynamic Impedance (Figure 3)<br>( $V_{KA} = V_{ref}$ , $I_K = 0.1\text{ mA}$ to $20\text{ mA}$ , $f \leq 1.0\text{ kHz}$ , Note 14)                                                                                                                                                                                                                    | $ Z_{KA} $                             | –                       | 0.25            | 0.4                     | $\Omega$                     |

12. Guaranteed but not tested.

13. The deviation parameters  $\Delta V_{ref}$  and  $\Delta I_{ref}$  are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.



The average temperature coefficient of the reference input voltage,  $\alpha V_{ref}$  is defined as:

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{\left( \frac{\Delta V_{ref}}{V_{ref} (T_A = 25^\circ\text{C})} \times 10^6 \right)}{\Delta T_A}$$

$\alpha V_{ref}$  can be positive or negative depending on whether  $V_{ref} \text{ Min}$  or  $V_{ref} \text{ Max}$  occurs at the lower ambient temperature, refer to Figure 8.

Example:  $\Delta V_{ref} = 7.2\text{ mV}$  and the slope is positive,

$V_{ref} @ 25^\circ\text{C} = 1.241\text{ V}$

$\Delta T_A = 125^\circ\text{C}$

$$\alpha V_{ref} \left( \frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{0.0072 \times 10^6}{1.241 \times 125} = 46 \text{ ppm}/^\circ\text{C}$$

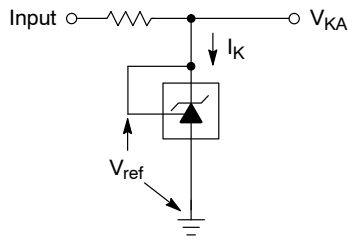
14. The dynamic impedance  $Z_{KA}$  is defined as:

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

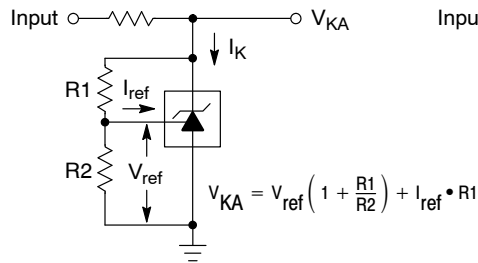
When the device is operating with two external resistors,  $R1$  and  $R2$ , (refer to Figure 4) the total dynamic impedance of the circuit is given by:

$$|Z_{KA}'| = |Z_{KA}| \times \left( 1 + \frac{R1}{R2} \right)$$

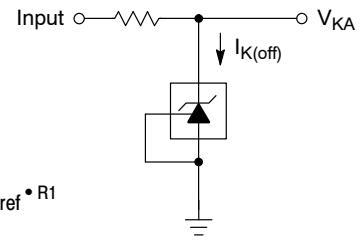
# TLV431, NCV431, SCV431



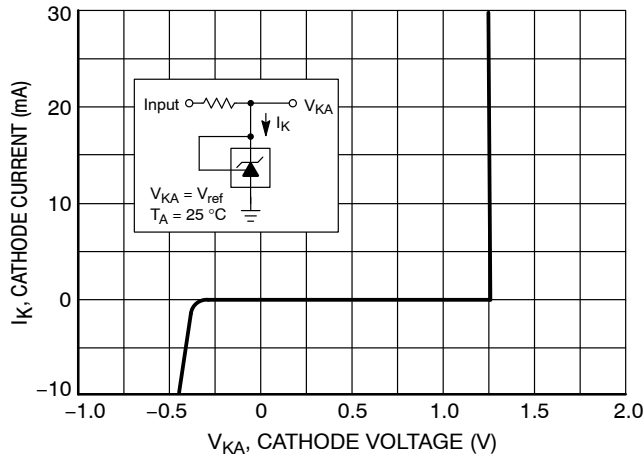
**Figure 3. Test Circuit for  $V_{KA} = V_{ref}$**



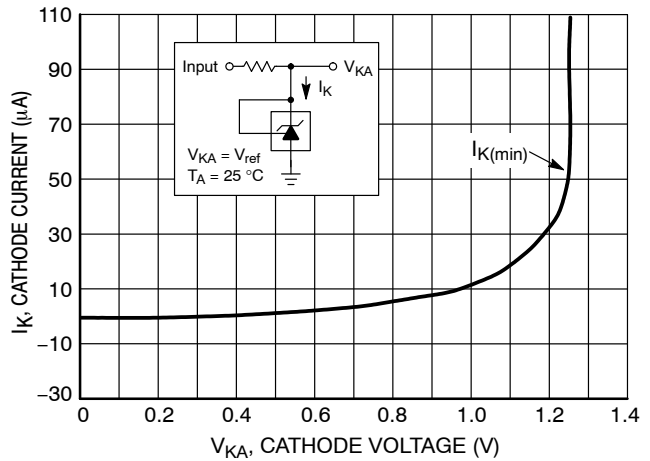
**Figure 4. Test Circuit for  $V_{KA} > V_{ref}$**



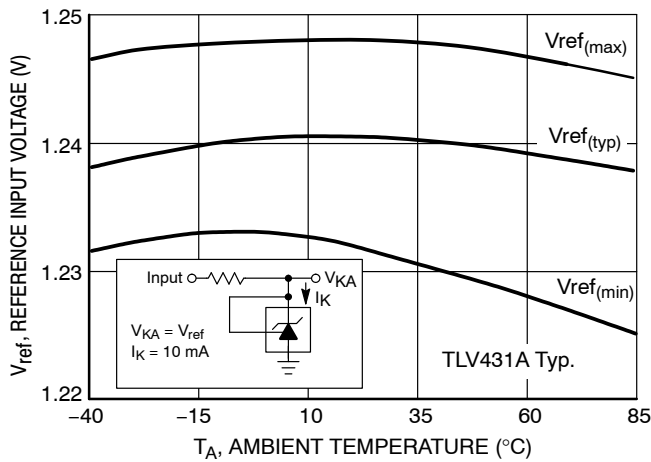
**Figure 5. Test Circuit for  $I_{K(off)}$**



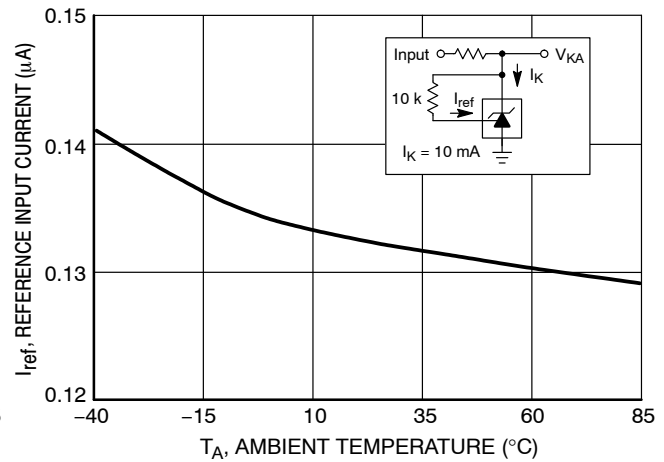
**Figure 6. Cathode Current vs. Cathode Voltage**



**Figure 7. Cathode Current vs. Cathode Voltage**



**Figure 8. Reference Input Voltage versus Ambient Temperature**



**Figure 9. Reference Input Current versus Ambient Temperature**

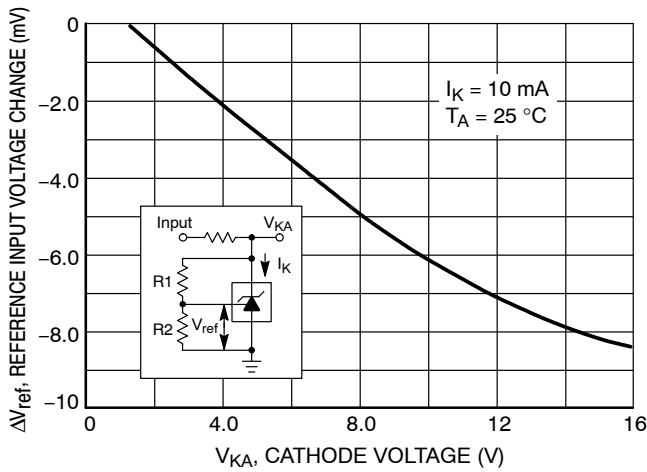


Figure 10. Reference Input Voltage Change versus Cathode Voltage

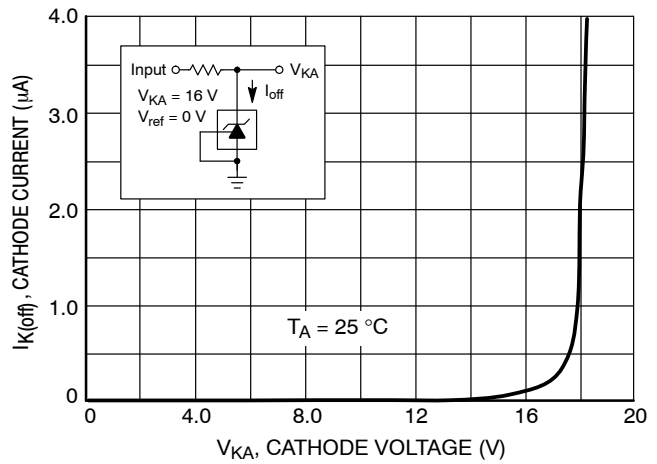


Figure 11. Off-State Cathode Current versus Cathode Voltage

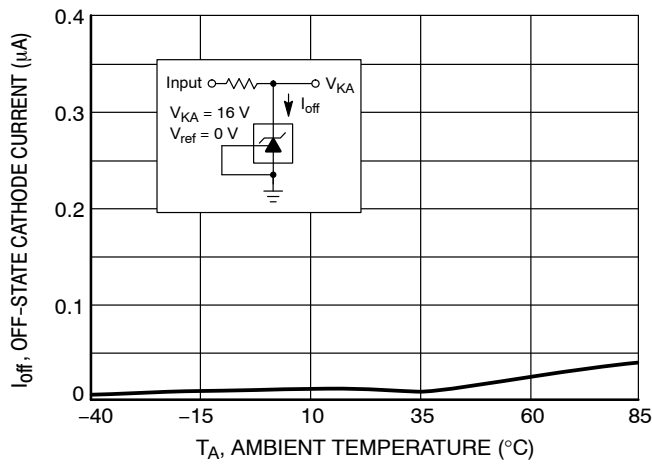


Figure 12. Off-State Cathode Current versus Ambient Temperature

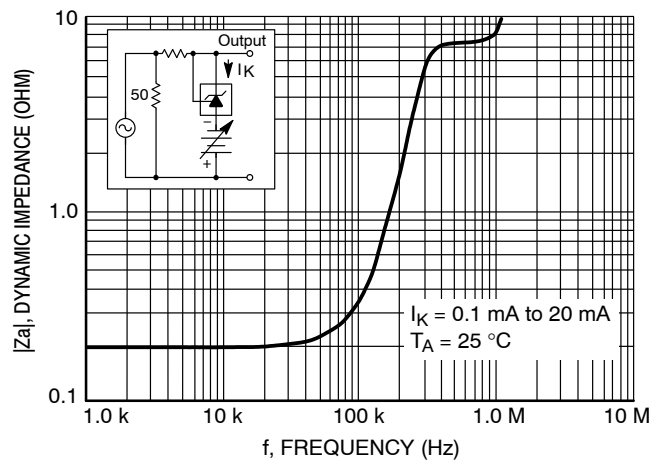


Figure 13. Dynamic Impedance versus Frequency

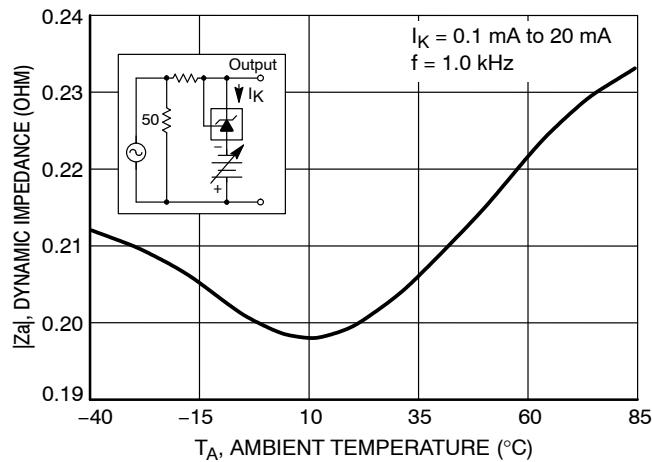


Figure 14. Dynamic Impedance versus Ambient Temperature

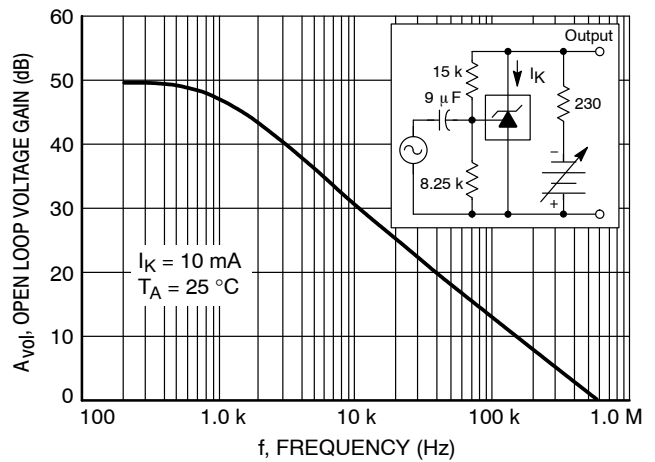


Figure 15. Open-Loop Voltage Gain versus Frequency

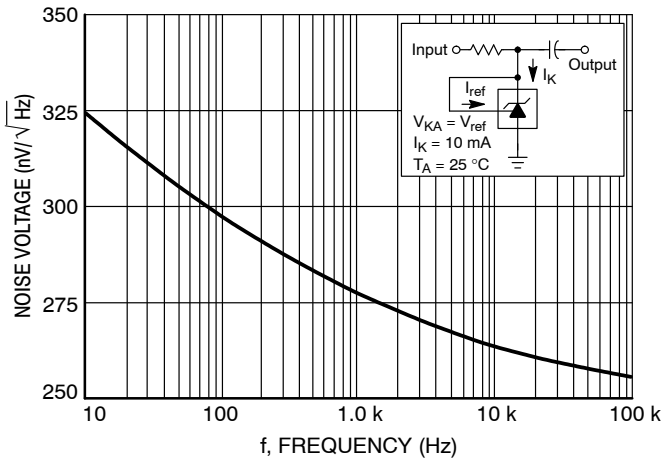


Figure 16. Spectral Noise Density

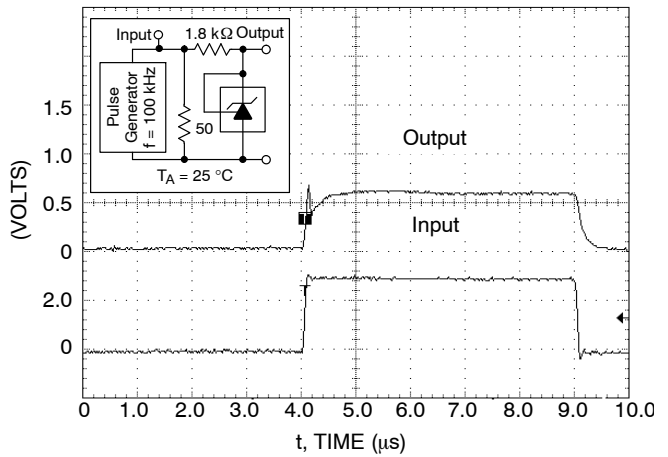


Figure 17. Pulse Response

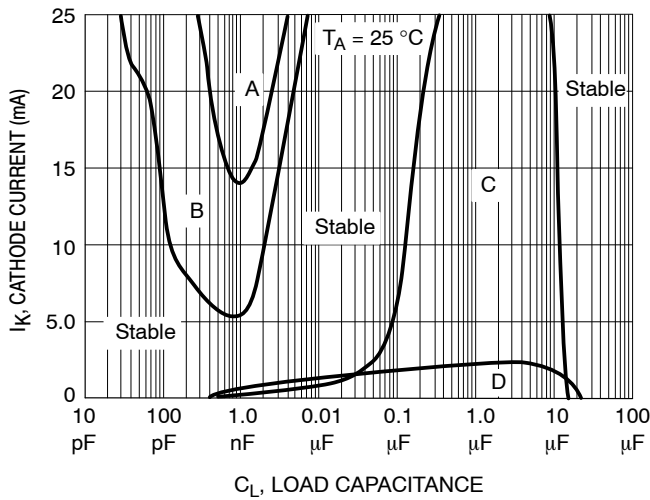
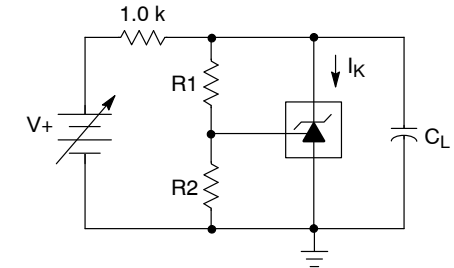


Figure 18. Stability Boundary Conditions



| Unstable Regions | V <sub>KA</sub> (V) | R1 (kΩ) | R2 (kΩ) |
|------------------|---------------------|---------|---------|
| A, C             | V <sub>ref</sub>    | 0       | ∞       |
| B, D             | 5.0                 | 30.4    | 10      |

Figure 19. Test Circuit for Figure 18

## STABILITY

Figures 18 and 19 show the stability boundaries and circuit configurations for the worst case conditions with the load capacitance mounted as close as possible to the device. The required load capacitance for stable operation can vary depending on the operating temperature and capacitor

equivalent series resistance (ESR). Ceramic or tantalum surface mount capacitors are recommended for both temperature and ESR. The application circuit stability should be verified over the anticipated operating current and temperature ranges.

TYPICAL APPLICATIONS

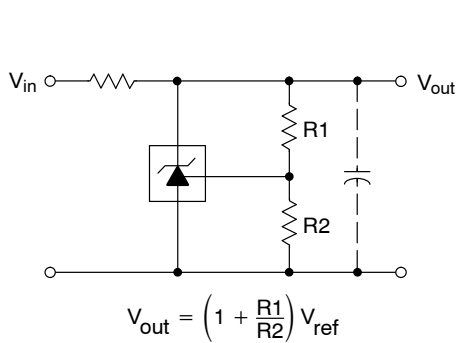


Figure 20. Shunt Regulator

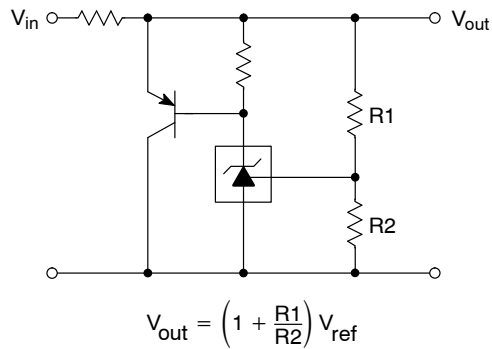


Figure 21. High Current Shunt Regulator

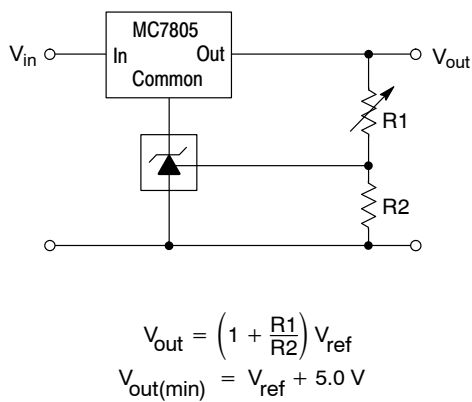


Figure 22. Output Control for a Three Terminal Fixed Regulator

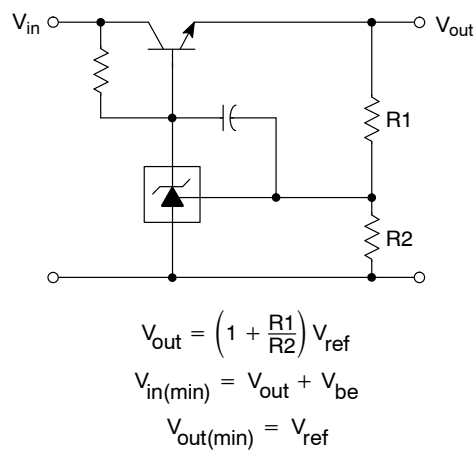


Figure 23. Series Pass Regulator

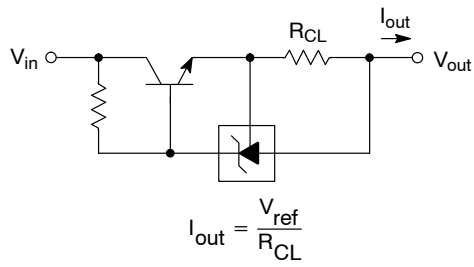


Figure 24. Constant Current Source

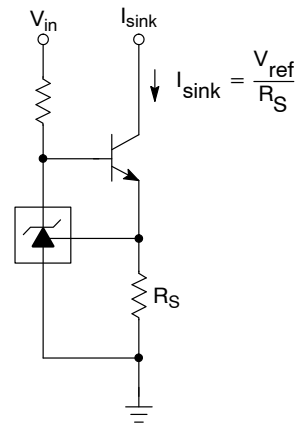


Figure 25. Constant Current Sink

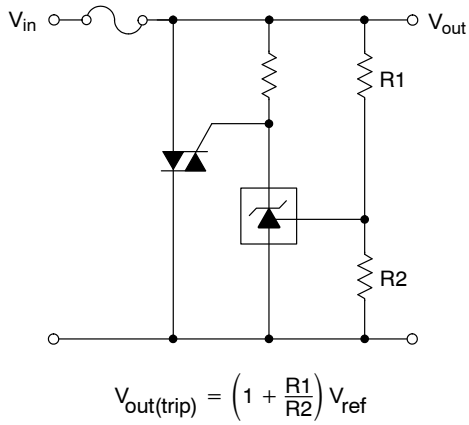


Figure 26. TRIAC Crowbar

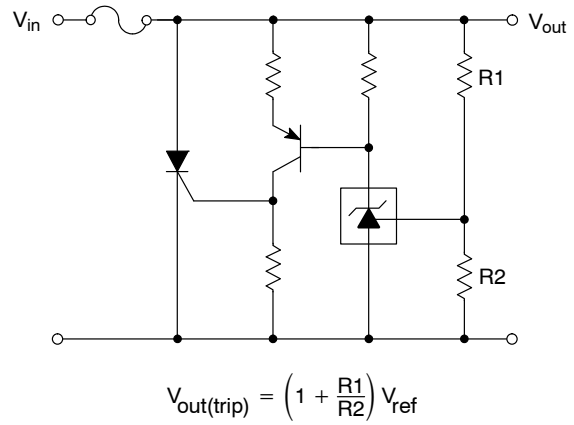
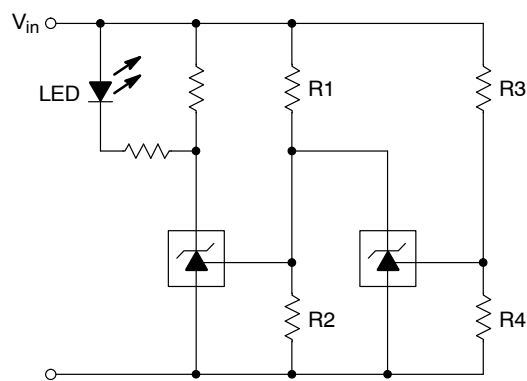


Figure 27. SCR Crowbar

## TLV431, NCV431, SCV431

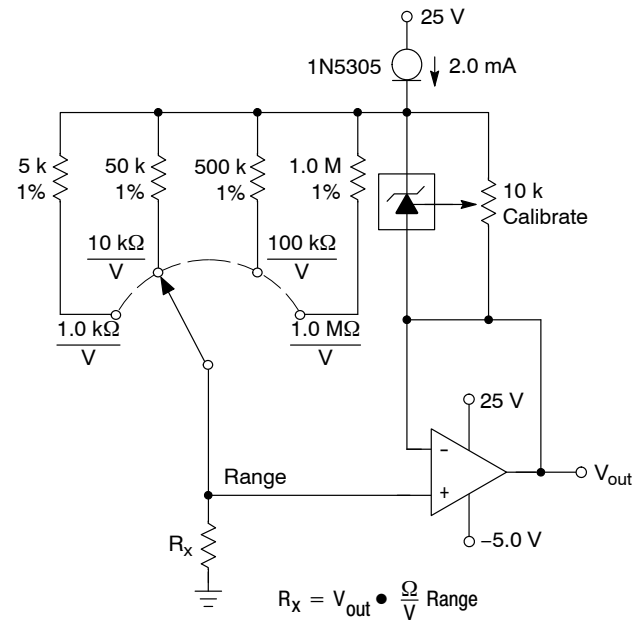


L.E.D. indicator is 'ON' when  $V_{in}$  is between the upper and lower limits,

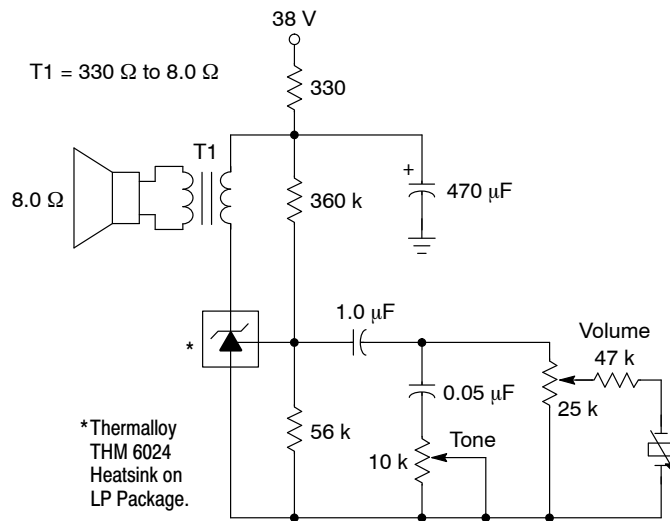
$$\text{Lower limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$\text{Upper limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

**Figure 28. Voltage Monitor**

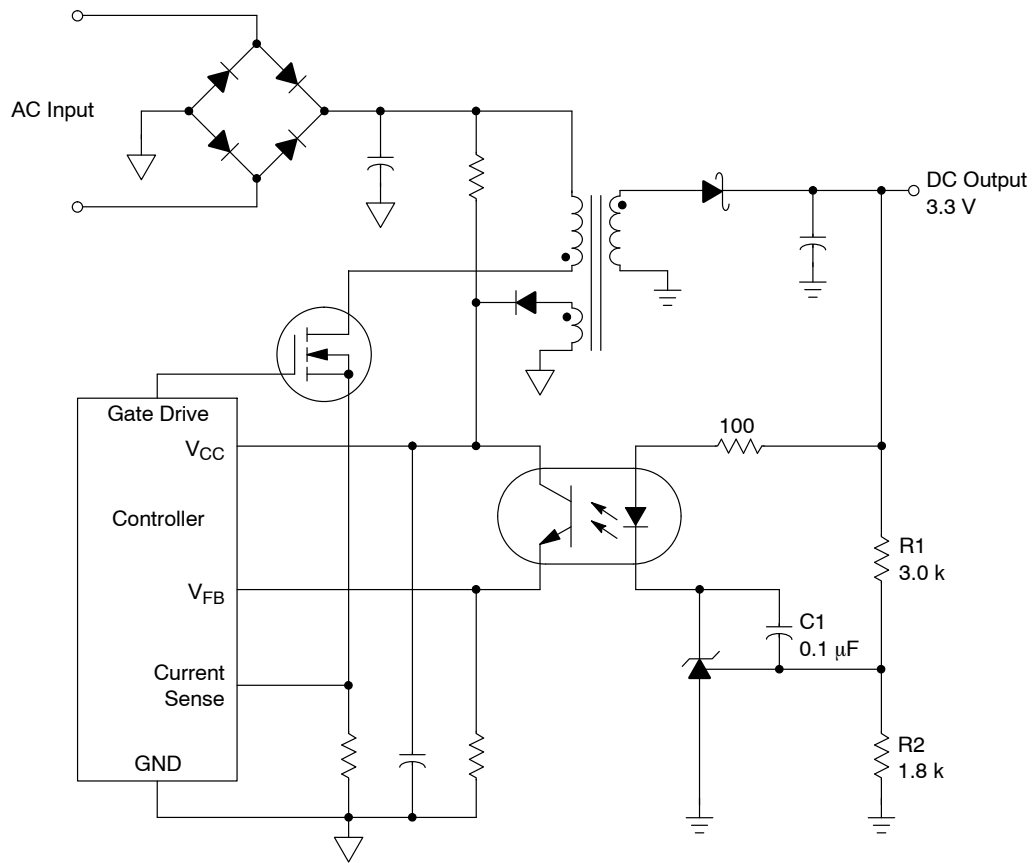


**Figure 29. Linear Ohmmeter**



**Figure 30. Simple 400 mW Phono Amplifier**

## TLV431, NCV431, SCV431

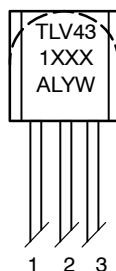


**Figure 31. Isolated Output Line Powered Switching Power Supply**

The above circuit shows the TLV431A/B/C as a compensated amplifier controlling the feedback loop of an isolated output line powered switching regulator. The output voltage is programmed to 3.3 V by the resistors values selected for R1 and R2. The minimum output voltage that can be programmed with this circuit is 2.64 V, and is limited by the sum of the reference voltage (1.24 V) and the forward drop of the optocoupler light emitting diode (1.4 V). Capacitor C1 provides loop compensation.

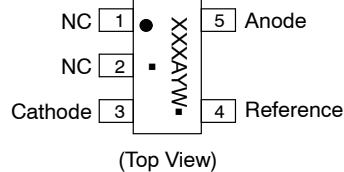
## PIN CONNECTIONS AND DEVICE MARKING

### TO-92



1. Reference
2. Anode
3. Cathode

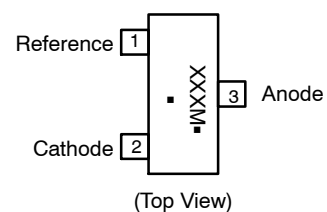
### TSOP-5



(Top View)

XXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 L = Wafer Lot  
 W = Work Week  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

### SOT-23-3



(Top View)

XXX = Specific Device Code  
 M = Date Code  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

# TLV431, NCV431, SCV431

## ORDERING INFORMATION

| Device         | Device Code | Package                            | Shipping†          |
|----------------|-------------|------------------------------------|--------------------|
| TLV431ALPRAG   | ALP         | TO-92-3<br>(Pb-Free)               | 2000 / Tape & Reel |
| TLV431ASNT1G   | RAA         | TSOP-5<br>(Pb-Free, Halide-Free)   | 3000 / Tape & Reel |
| TLV431ASN1T1G  | RAF         | SOT-23-3<br>(Pb-Free, Halide-Free) | 3000 / Tape & Reel |
| TLV431BSNT1G   | RAH         | TSOP-5<br>(Pb-Free, Halide-Free)   | 3000 / Tape & Reel |
| TLV431BSN1T1G  | RAG         | SOT-23-3<br>(Pb-Free, Halide-Free) | 3000 / Tape & Reel |
| TLV431CSN1T1G  | AAN         | SOT-23-3<br>(Pb-Free, Halide-Free) | 3000 / Tape & Reel |
| SCV431ASN1T1G* | RAE         | SOT-23-3<br>(Pb-Free, Halide-Free) | 3000 / Tape & Reel |
| SCV431BSN1T1G* | RAC         | SOT-23-3<br>(Pb-Free, Halide-Free) | 3000 / Tape & Reel |
| NCV431ASNT1G*  | ACH         | TSOP-5<br>(Pb-Free, Halide-Free)   | 3000 / Tape & Reel |
| NCV431BSNT1G*  | AD6         | TSOP-5<br>(Pb-Free, Halide-Free)   | 3000 / Tape & Reel |

## DISCONTINUED (Note 15)

|              |     |                      |                    |
|--------------|-----|----------------------|--------------------|
| TLV431ALPG   | ALP | TO-92-3<br>(Pb-Free) | 6000 / Box         |
| TLV431ALPREG | ALP | TO-92-3<br>(Pb-Free) | 2000 / Tape & Reel |
| TLV431ALPRMG | ALP | TO-92-3<br>(Pb-Free) | 2000 / Ammo Pack   |
| TLV431ALPRPG | ALP | TO-92-3<br>(Pb-Free) | 2000 / Ammo Pack   |
| TLV431BLPG   | BLP | TO-92-3<br>(Pb-Free) | 6000 / Box         |
| TLV431BLPRAG | BLP | TO-92-3<br>(Pb-Free) | 2000 / Tape & Reel |
| TLV431BLPREG | BLP | TO-92-3<br>(Pb-Free) | 2000 / Tape & Reel |
| TLV431BLPRMG | BLP | TO-92-3<br>(Pb-Free) | 2000 / Ammo Pack   |
| TLV431BLPRPG | BLP | TO-92-3<br>(Pb-Free) | 2000 / Ammo Pack   |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*SCV, NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

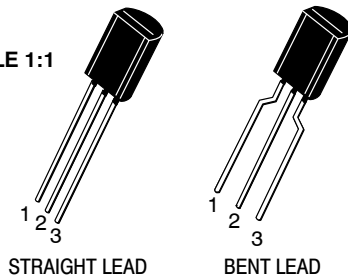
15. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

## TLV431, NCV431, SCV431

### REVISION HISTORY

| Revision | Description of Changes                                                                                                                                                                                                                                              | Date     |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| 28       | <ul style="list-style-type: none"><li>• Rebranded the Data Sheet to <b>onsemi</b> format.</li><li>• TLV431ALPG, TLV431ALPREG, TLV431ALPRMG, TLV431ALPRPG, TLV431BLPG, TLV431BLPRAG, TLV431BLPREG, TLV431BLPRMG, TLV431BLPRPG OPNs Marked as Discontinued.</li></ul> | 6/5/2025 |

SCALE 1:1



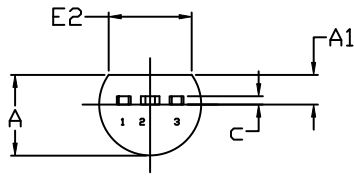
STRAIGHT LEAD

BENT LEAD

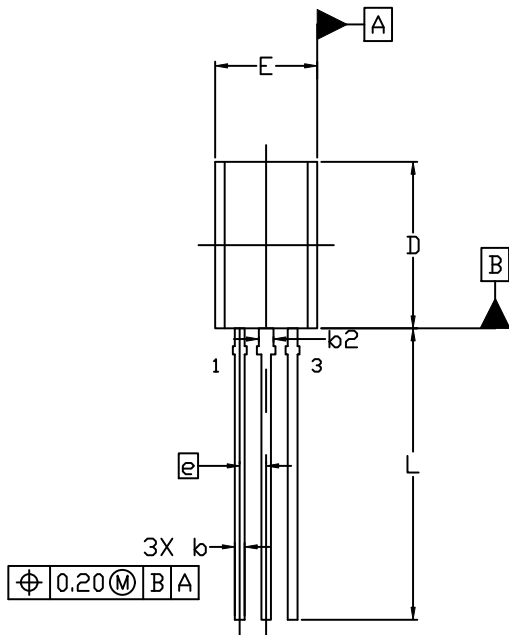
**TO-92 (TO-226) 1 WATT**  
**CASE 29-10**  
**ISSUE D**

DATE 05 MAR 2021

## STRAIGHT LEAD



END VIEW



TOP VIEW

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

| DIM | MILLIMETERS |       |       |
|-----|-------------|-------|-------|
|     | MIN.        | NOM.  | MAX.  |
| A   | 3.75        | 3.90  | 4.05  |
| A1  | 1.28        | 1.43  | 1.58  |
| b   | 0.38        | 0.465 | 0.55  |
| b2  | 0.62        | 0.70  | 0.78  |
| c   | 0.35        | 0.40  | 0.45  |
| D   | 7.85        | 8.00  | 8.15  |
| E   | 4.75        | 4.90  | 5.05  |
| E2  | 3.90        | ---   | ---   |
| e   | 1.27 BSC    |       |       |
| L   | 13.80       | 14.00 | 14.20 |

## STYLES AND MARKING ON PAGE 3

|                         |                              |                                                                                                                                                                                  |
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**TO-92 (TO-226) 1 WATT**  
CASE 29-10  
ISSUE D

DATE 05 MAR 2021

**FORMED LEAD**



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

| DIM | MILLIMETERS |       |       |
|-----|-------------|-------|-------|
|     | MIN.        | NOM.  | MAX.  |
| A   | 3.75        | 3.90  | 4.05  |
| A1  | 1.28        | 1.43  | 1.58  |
| b   | 0.38        | 0.465 | 0.55  |
| b2  | 0.62        | 0.70  | 0.78  |
| c   | 0.35        | 0.40  | 0.45  |
| D   | 7.85        | 8.00  | 8.15  |
| E   | 4.75        | 4.90  | 5.05  |
| E2  | 3.90        | ---   | ---   |
| e   | 2.50 BSC    |       |       |
| L   | 13.80       | 14.00 | 14.20 |
| L2  | 13.20       | 13.60 | 14.00 |
| L3  | 3.00 REF    |       |       |

**STYLES AND MARKING ON PAGE 3**

|                         |                              |                                                                                                                                                                                     |
|-------------------------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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**TO-92 (TO-226) 1 WATT**  
**CASE 29-10**  
**ISSUE D**

DATE 05 MAR 2021

|                                                                 |                                                                      |                                                              |                                                                 |                                                             |
|-----------------------------------------------------------------|----------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------------------------------------------|-------------------------------------------------------------|
| STYLE 1:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR           | STYLE 2:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR                | STYLE 3:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE           | STYLE 4:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE            | STYLE 5:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE            |
| STYLE 6:<br>PIN 1. GATE<br>2. SOURCE & SUBSTRATE<br>3. DRAIN    | STYLE 7:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE                     | STYLE 8:<br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE & SUBSTRATE | STYLE 9:<br>PIN 1. BASE 1<br>2. EMITTER<br>3. BASE 2            | STYLE 10:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          |
| STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE & ANODE<br>3. CATHODE   | STYLE 12:<br>PIN 1. MAIN TERMINAL 1<br>2. GATE<br>3. MAIN TERMINAL 2 | STYLE 13:<br>PIN 1. ANODE 1<br>2. GATE<br>3. CATHODE 2       | STYLE 14:<br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. BASE          | STYLE 15:<br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2     |
| STYLE 16:<br>PIN 1. ANODE<br>2. GATE<br>3. CATHODE              | STYLE 17:<br>PIN 1. COLLECTOR<br>2. BASE<br>3. EMITTER               | STYLE 18:<br>PIN 1. ANODE<br>2. CATHODE<br>3. NOT CONNECTED  | STYLE 19:<br>PIN 1. GATE<br>2. ANODE<br>3. CATHODE              | STYLE 20:<br>PIN 1. NOT CONNECTED<br>2. CATHODE<br>3. ANODE |
| STYLE 21:<br>PIN 1. COLLECTOR<br>2. EMITTER<br>3. BASE          | STYLE 22:<br>PIN 1. SOURCE<br>2. GATE<br>3. DRAIN                    | STYLE 23:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN            | STYLE 24:<br>PIN 1. EMITTER<br>2. COLLECTOR/ANODE<br>3. CATHODE | STYLE 25:<br>PIN 1. MT 1<br>2. GATE<br>3. MT 2              |
| STYLE 26:<br>PIN 1. V <sub>CC</sub><br>2. GROUND 2<br>3. OUTPUT | STYLE 27:<br>PIN 1. MT<br>2. SUBSTRATE<br>3. MT                      | STYLE 28:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE           | STYLE 29:<br>PIN 1. NOT CONNECTED<br>2. ANODE<br>3. CATHODE     | STYLE 30:<br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE           |
| STYLE 31:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE               | STYLE 32:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER               | STYLE 33:<br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT          | STYLE 34:<br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC              | STYLE 35:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER      |

**GENERIC  
MARKING DIAGRAM\***



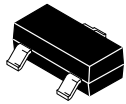
XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

|                         |                              |                                                                                                                                                                                     |
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| <b>DESCRIPTION:</b>     | <b>TO-92 (TO-226) 1 WATT</b> | <b>PAGE 3 OF 3</b>                                                                                                                                                                  |

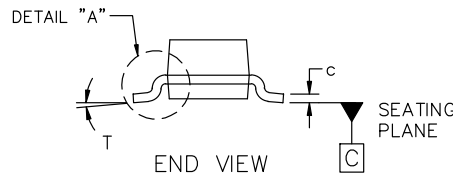
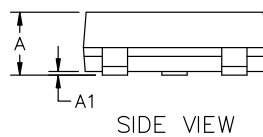
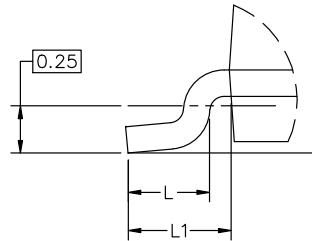
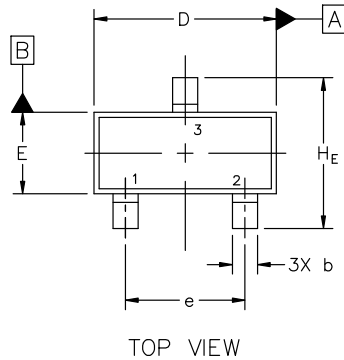
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SCALE 4:1

**SOT-23 (TO-236) 2.90x1.30x1.00 1.90P**  
**CASE 318**  
**ISSUE AU**

DATE 14 AUG 2024

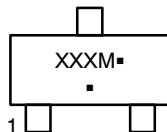


| MILLIMETERS |      |      |      |
|-------------|------|------|------|
| DIM         | MIN  | NOM  | MAX  |
| A           | 0.89 | 1.00 | 1.11 |
| A1          | 0.01 | 0.06 | 0.10 |
| b           | 0.37 | 0.44 | 0.50 |
| c           | 0.08 | 0.14 | 0.20 |
| D           | 2.80 | 2.90 | 3.04 |
| E           | 1.20 | 1.30 | 1.40 |
| e           | 1.78 | 1.90 | 2.04 |
| L           | 0.30 | 0.43 | 0.55 |
| L1          | 0.35 | 0.54 | 0.69 |
| HE          | 2.10 | 2.40 | 2.64 |
| T           | 0°   | ---  | 10°  |

NOTES:

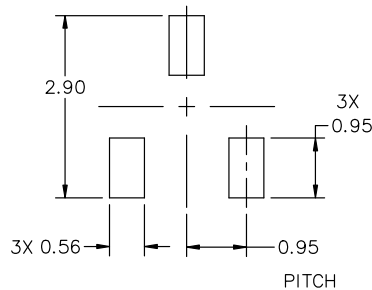
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

**GENERIC MARKING DIAGRAM\***



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

**STYLES ON PAGE 2**

|                         |                                             |                                                                                                                                                                                     |
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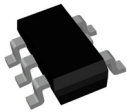
**SOT-23 (TO-236) 2.90x1.30x1.00 1.90P**  
**CASE 318**  
**ISSUE AU**

DATE 14 AUG 2024

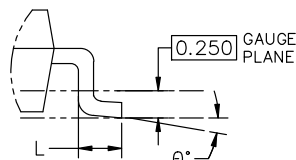
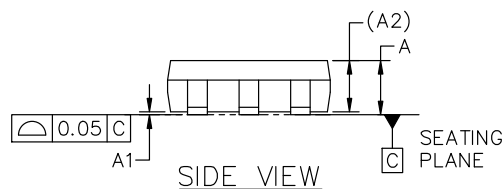
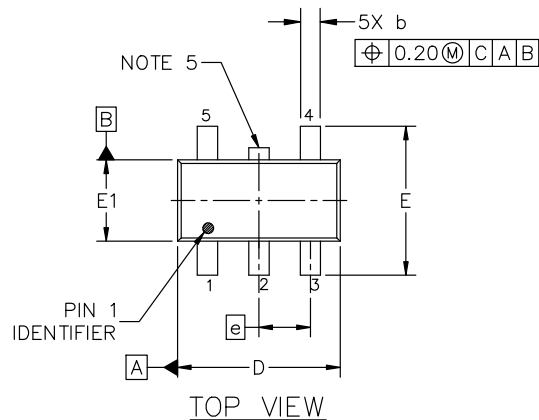
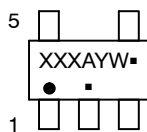
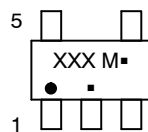
|                                                         |                                                       |                                                             |                                                             |                                                             |                                                             |
|---------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------|
| STYLE 1 THRU 5:<br>CANCELLED                            | STYLE 6:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR | STYLE 7:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR       | STYLE 8:<br>PIN 1. ANODE<br>2. NO CONNECTION<br>3. CATHODE  |                                                             |                                                             |
| STYLE 9:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE      | STYLE 10:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE     | STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE-ANODE | STYLE 12:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE       | STYLE 13:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE           | STYLE 14:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          |
| STYLE 15:<br>PIN 1. GATE<br>2. CATHODE<br>3. ANODE      | STYLE 16:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE | STYLE 17:<br>PIN 1. NO CONNECTION<br>2. ANODE<br>3. CATHODE | STYLE 18:<br>PIN 1. NO CONNECTION<br>2. CATHODE<br>3. ANODE | STYLE 19:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE-ANODE | STYLE 20:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE          |
| STYLE 21:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN       | STYLE 22:<br>PIN 1. RETURN<br>2. OUTPUT<br>3. INPUT   | STYLE 23:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE         | STYLE 24:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE           | STYLE 25:<br>PIN 1. ANODE<br>2. CATHODE<br>3. GATE          | STYLE 26:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION |
| STYLE 27:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE | STYLE 28:<br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE     |                                                             |                                                             |                                                             |                                                             |

|                  |                                      |                                                                                                                                                                                     |
|------------------|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| DESCRIPTION:     | SOT-23 (TO-236) 2.90x1.30x1.00 1.90P | PAGE 2 OF 2                                                                                                                                                                         |

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**TSOP-5 3.00x1.50x0.95, 0.95P**  
**CASE 483**  
**ISSUE P**

DATE 01 APR 2024


**GENERIC**  
**MARKING DIAGRAM\***

**Analog**

**Discrete/Logic**

XXX = Specific Device Code    XXX = Specific Device Code  
A = Assembly Location    M = Date Code  
Y = Year    ■ = Pb-Free Package  
W = Work Week  
■ = Pb-Free Package

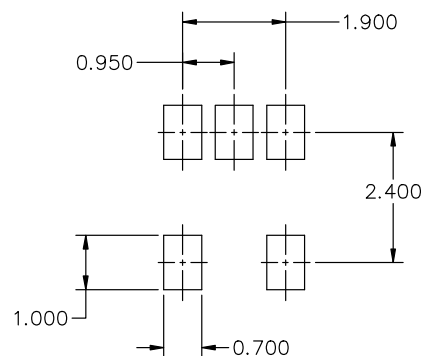
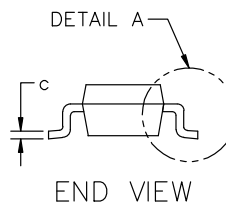
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

## NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

| DIM | MILLIMETERS |       |       |
|-----|-------------|-------|-------|
|     | MIN.        | NOM.  | MAX.  |
| A   | 0.900       | 1.000 | 1.100 |
| A1  | 0.010       | 0.055 | 0.100 |
| A2  | 0.950 REF.  |       |       |
| b   | 0.250       | 0.375 | 0.500 |
| c   | 0.100       | 0.180 | 0.260 |
| D   | 2.850       | 3.000 | 3.150 |
| E   | 2.500       | 2.750 | 3.000 |
| E1  | 1.350       | 1.500 | 1.650 |
| e   | 0.950 BSC   |       |       |
| L   | 0.200       | 0.400 | 0.600 |
| θ   | 0°          | 5°    | 10°   |


**RECOMMENDED MOUNTING FOOTPRINT\***

\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

|                         |                                     |                                                                                                                                                                                  |
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| <b>DESCRIPTION:</b>     | <b>TSOP-5 3.00x1.50x0.95, 0.95P</b> | <b>PAGE 1 OF 1</b>                                                                                                                                                               |

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