

Vishay Siliconix

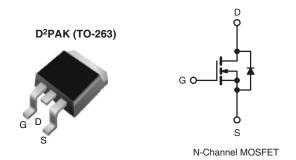
RoHS

COMPLIANT HALOGEN

FREE

Power MOSFET

| PRODUCT SUMMARY | | | | | |
|----------------------------|------------------------|------------------------------|--|--|--|
| V _{DS} (V) | 100 | 100 | | | |
| $R_{DS(on)}(\Omega)$ | V _{GS} = 10 V | V _{GS} = 10 V 0.077 | | | |
| Q _g (Max.) (nC) | 72 | 72 | | | |
| Q _{gs} (nC) | 11 | 11 | | | |
| Q _{gd} (nC) | 32 | 32 | | | |
| Configuration | Sing | Single | | | |



FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- · Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- 175 °C Operating Temperature
- Fast Switching
- · Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

| ORDERING INFORMATION | | | | | |
|---------------------------------|-----------------------------|-----------------------------|-----------------------------|--|--|
| Package | D ² PAK (TO-263) | D ² PAK (TO-263) | D ² PAK (TO-263) | | |
| Lead (Pb)-free and Halogen-free | SiHF540S-GE3 | SiHF540STRL-GE3a | SiHF540STRR-GE3a | | |
| Load (Dh) froe | IRF540SPbF | IRF540STRLPbFa | IRF540STRRPbFa | | |
| Lead (Pb)-free | SiHF540S-E3 | SiHF540STL-E3 ^a | SiHF540STR-E3 ^a | | |

Note

a. See device orientation.

| ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted | | | | | | |
|--|-------------------------|---|-----------------------------------|------------------|---------------------------------------|--|
| PARAMETER | | | SYMBOL | LIMIT | UNIT | |
| Drain-Source Voltage | | | V _{DS} | 100 | V | |
| Gate-Source Voltage | | | V_{GS} | ± 20 | \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ | |
| Continuous Drain Current | V _{GS} at 10 V | T _C = 25 °C T _C = 100 °C | I _D | 28 | | |
| Continuous Drain Current | V _{GS} at 10 V | T _C = 100 °C | | 20 | Α | |
| Pulsed Drain Current ^a | | | I _{DM} | 110 | | |
| Linear Derating Factor | | | | 1.0 | W/°C | |
| Linear Derating Factor (PCB Mount) ^e | | | | 0.025 |] | |
| Single Pulse Avalanche Energy ^b | | | E _{AS} | 230 | mJ | |
| Avalanche Current ^a | | | I _{AR} | 28 | Α | |
| Repetitive Avalanche Energy ^a | | | E _{AR} | 15 | mJ | |
| Maximum Power Dissipation $T_C = 25 ^{\circ}\text{C}$ | | | P _D | 150 | W | |
| Maximum Power Dissipation (PCB Mount) ^e T _A = 25 °C | | | | 3.7 | 1 ^{vv} | |
| Peak Diode Recovery dV/dt ^c | | | dV/dt | 5.5 | V/ns | |
| Operating Junction and Storage Temperature Range | | | T _J , T _{stg} | - 55 to + 175 | °C | |
| Soldering Recommendations (Peak Temperature) for 10 s | | | - | 300 ^d | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. V_{DD} = 25 V, starting T_J = 25 °C, L = 440 μ H, R_g = 25 Ω , I_{AS} = 28 A (see fig. 12).
- c. $I_{SD} \le 28 \text{ A}$, $dI/dt \le 170 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_{J} \le 175 \,^{\circ}\text{C}$.
- d. 1.6 mm from case.
- e. When mounted on 1" square PCB (FR-4 or G-10 material).

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply

IRF540S, SiHF540S

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| THERMAL RESISTANCE RATINGS | | | | | |
|--|-------------------|------|------|------|--|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT | |
| Maximum Junction-to-Ambient | R _{thJA} | - | 62 | | |
| Maximum Junction-to-Ambient (PCB Mount) ^a | R _{thJA} | - | 40 | °C/W | |
| Maximum Junction-to-Case (Drain) | R _{thJC} | - | 1.0 | | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|-----------------------|---|---|------|------|------------------|------|
| Static | | | | • | | | · |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} | = 0, I _D = 250 μA | 100 | - | - | V |
| V _{DS} Temperature Coefficient | $\Delta V_{DS}/T_{J}$ | Reference | e to 25 °C, I _D = 1 mA | - | 0.13 | - | V/°C |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = | - V _{GS} , I _D = 250 μA | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I _{GSS} | , | V _{GS} = ± 20 V | - | - | ± 100 | nA |
| Zara Cata Valtaga Drain Current | | V _{DS} = | = 100 V, V _{GS} = 0 V | - | - | 25 | |
| Zero Gate Voltage Drain Current | I _{DSS} | $V_{DS} = 80 \text{ V}$ | $V_{GS} = 0 \text{ V}, T_{J} = 150 ^{\circ}\text{C}$ | - | - | 250 | μA |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 17 A ^b | - | - | 0.077 | Ω |
| Forward Transconductance | 9 _{fs} | V _{DS} : | = 50 V, I _D = 17 A ^b | 8.7 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | | $V_{GS} = 0 V$, | - | 1700 | - | |
| Output Capacitance | C_{oss} | | $V_{DS} = 25 V$, | - | 560 | - | pF |
| Reverse Transfer Capacitance | C_{rss} | f = 1. | 0 MHz, see fig. 5 | - | 120 | - | |
| Total Gate Charge | Q_g | | | - | - | 72 | |
| Gate-Source Charge | Q_gs | $V_{GS} = 10 \text{ V}$ | $V_{GS} = 10 \text{ V}$ $I_D = 17 \text{ A}, V_{DS} = 80 \text{ V},$ see fig. 6 and 13 ^b | | - | 11 | nC |
| Gate-Drain Charge | Q_gd | | | - | - | 32 | |
| Turn-On Delay Time | $t_{d(on)}$ | V_{DD} = 50 V, I_{D} = 17 A, R_{g} = 9.1 Ω, R_{D} = 2.9 Ω, see fig. 10 ^b | | - | 11 | - | |
| Rise Time | t _r | | | - | 44 | - | ns |
| Turn-Off Delay Time | t _{d(off)} | | | - | 53 | - | |
| Fall Time | t _f | | | - | 43 | - | |
| Internal Drain Inductance | L _D | 6 mm (0.25") t | Between lead, 6 mm (0.25") from | | 4.5 | - | ъЦ |
| Internal Source Inductance | L _S | package and center of die contact | | _ | 7.5 | - | - nH |
| Drain-Source Body Diode Characteristic | s | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode | | - | - | 28 | А |
| Pulsed Diode Forward Current ^a | I _{SM} | | | - | - | 110 | |
| Body Diode Voltage | V_{SD} | $T_J = 25 ^{\circ}\text{C}, I_S = 28 \text{A}, V_{GS} = 0 \text{V}^{\text{b}}$ | | - | - | 2.5 | V |
| Body Diode Reverse Recovery Time | t _{rr} | $T_J = 25 \text{ °C}, I_F = 17 \text{ A}, dI/dt = 100 \text{ A/}\mu\text{s}^b$ | | - | 180 | 360 | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | | - | 1.3 | 2.8 | μC |
| Forward Turn-On Time | t _{on} | Intrinsic tu | gible (turn-on is dominated by L_S and L_D) | | | L _D) | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

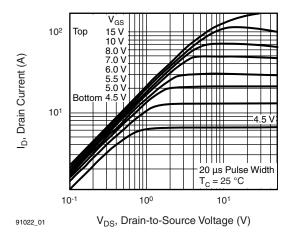


Fig. 1 - Typical Output Characteristics, $T_C = 25$ °C

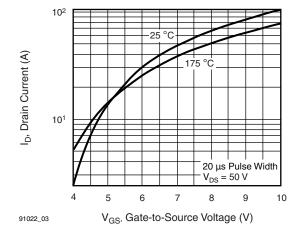


Fig. 3 - Typical Transfer Characteristics

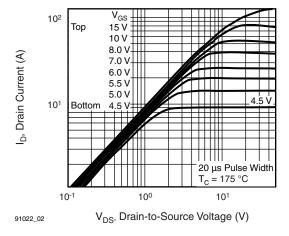


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

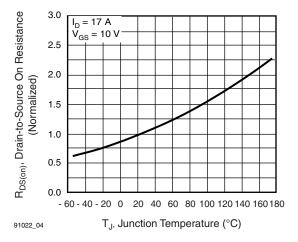


Fig. 4 - Normalized On-Resistance vs. Temperature

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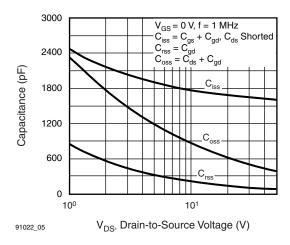


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

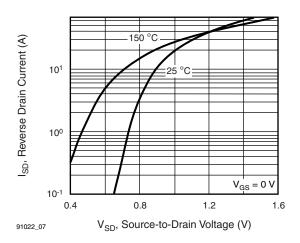


Fig. 7 - Typical Source-Drain Diode Forward Voltage

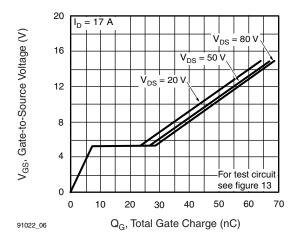


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

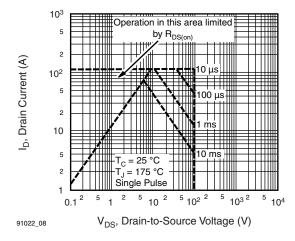


Fig. 8 - Maximum Safe Operating Area





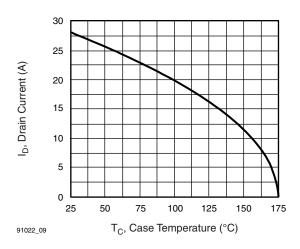


Fig. 9 - Maximum Drain Current vs. Case Temperature

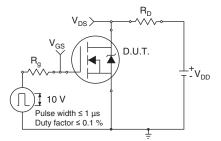


Fig. 10a - Switching Time Test Circuit

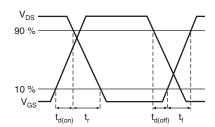


Fig. 10b - Switching Time Waveforms

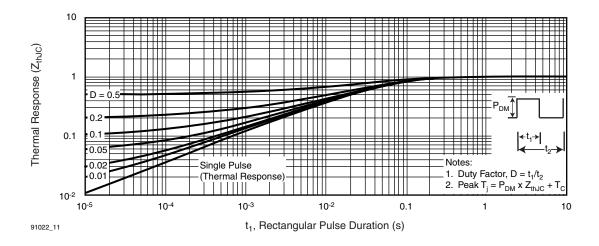


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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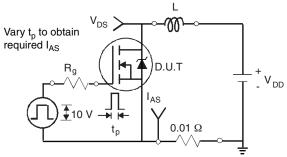


Fig. 12a - Unclamped Inductive Test Circuit

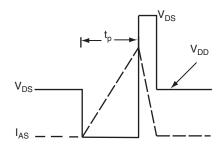


Fig. 12b - Unclamped Inductive Waveforms

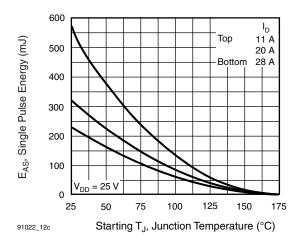


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

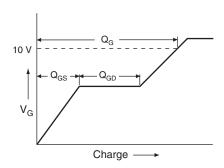


Fig. 13a - Basic Gate Charge Waveform

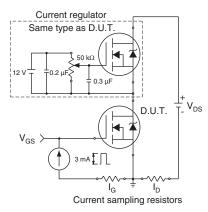
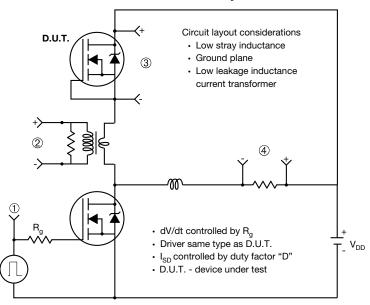


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



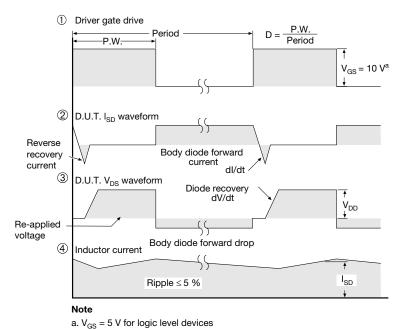


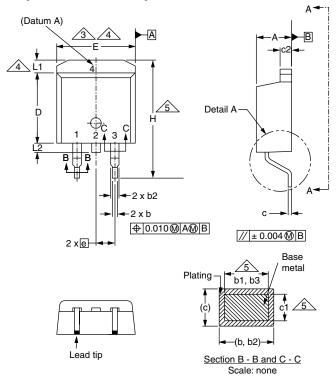
Fig. 14 - For N-Channel

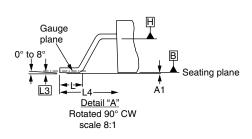
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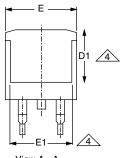




TO-263AB (HIGH VOLTAGE)







View A - A

| | MILLIN | METERS | INC | HES |
|------|--------|--------|-------|-------|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| Α | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| С | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| | MILLIMETERS | | INC | HES |
|------|-------------|-------|-----------|-------|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| Е | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | i |
| е | 2.54 BSC | | 0.100 BSC | |
| Н | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | ı | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 | BSC |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |
| | | | | |

ECN: S-82110-Rev. A, 15-Sep-08

DWG: 5970

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.
- 7. Outline conforms to JEDEC outline to TO-263AB.

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