PRELIMINARY

4-BIT SINGLE CHIP MICRO CONTROLLER

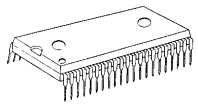
■ GENERAL DESCRIPTION

The **NJU3505** is the C-MOS 4-bit Single Chip Micro Controller consisting of the 4-bit CPU Core, Input / Output Selectable I/O ports, Program ROM, Data RAM, Dual Timer/Counter, 8-bit Serial Interface, 8-bit A/D Converter, and Oscillator Circuit (CR or Ceramic or X'tal). It realizes the control for home appliances or toys by only few external components.

The **NJU3505** is suitable for battery operated appliances because of low operating current, wide operating voltage range, and STANDBY function (HALT mode).

■ PACKAGE OUTLINE

NJU3505FA1



NJU3505L

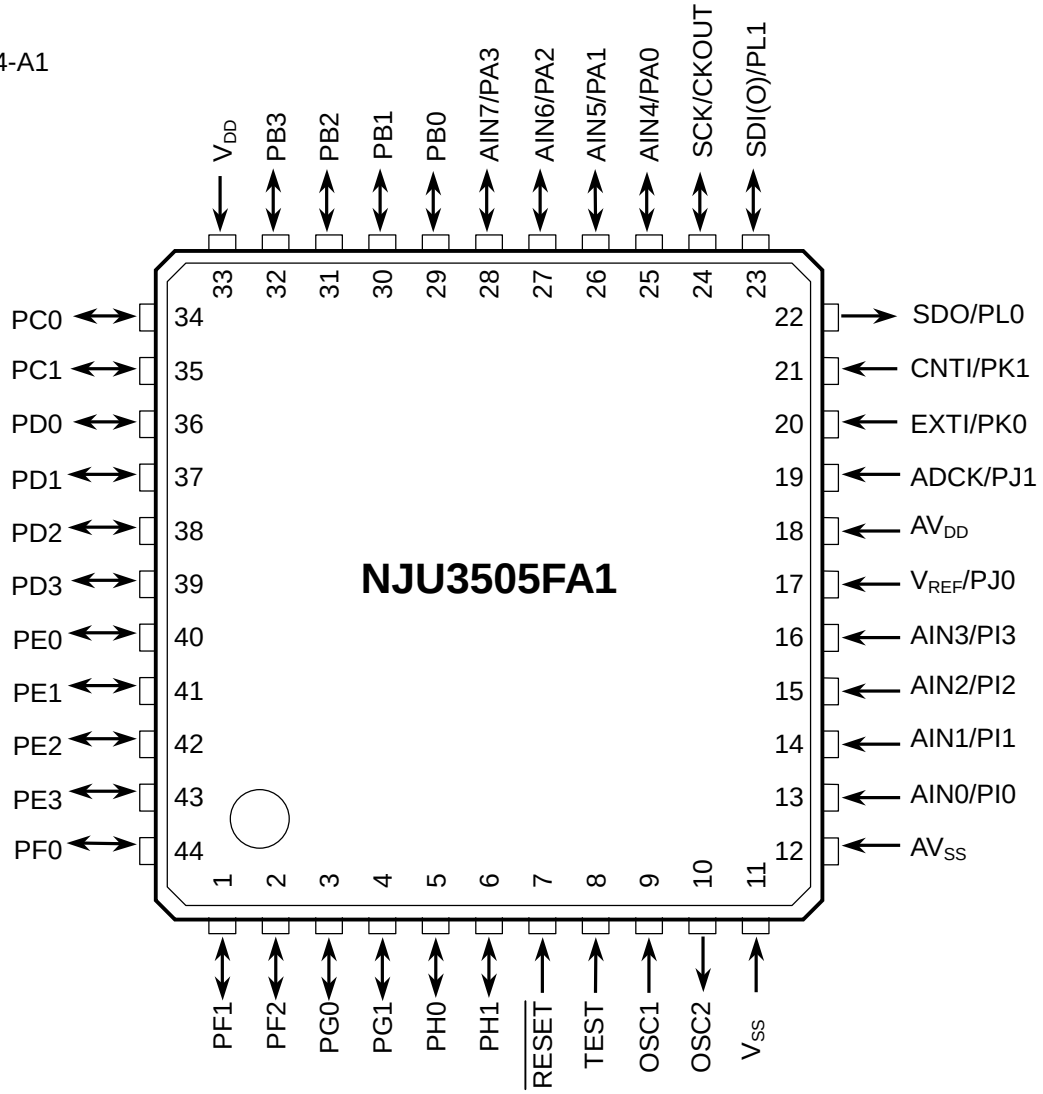
■ FEATURES

- Internal Program ROM 8,192 X 8 bits
- Internal Data RAM 256 X 4 bits
- Input / Output Port 35 lines(MAX) / NJU3505FA1
  33 lines(MAX) / NJU3505L
  17 lines·····Input / Output direction of each bit is selected by the mask option.
  4 lines·····Input / Output direction of the 4-bit lines' group can be changed by the program.
  Additional functions by the mask option.
  External Interrupt Terminal : EXTI/PK0
  External Clock Input Terminal for Timer2 : CNTI/PK1
  Serial Interface Terminals : SDO/PL0, SDI(O)/PL1
  A/D Converter Interface Terminals : AIN0–3/PI0–3,V_{REF}/PJ0,ADCK/PJ1
- High Output-Current terminal (10 lines)
  N-Channel FET Open Drain Type (I_{OL}) 15mA at V_{DD}=5V (PA0–PA3, PB0–PB3, PC0, PC1)
- Instruction Set 59 instructions
- Subroutine Nesting 8 levels
- Pulse Edge Detector
  The rising or falling edge of a pulse is selected by the mask option.
- Instruction Executing Time $6/f_{OSC}$ sec (1.5µsec at 4MHz)
- Operating Frequency Range 30kHz – 4MHz
- Internal Oscillator
  CR, or Ceramic, or X'tal oscillation and External clock input
- STANDBY function (HALT mode)
- Wide operating voltage range 2.4V – 5.5V
- 8-bit Serial Input / Output port
- Timer/Counter
  (Timer1 : 8-bit re-load type timer, Timer2 : 12-bit re-load type timer event counter)
  (Count clock : Timer1's clock is an internal one. Timer2's clock is an internal or external one.)
- 8-bit A/D converter (Multiplexed 8-channel input)
- Interrupt factor 4 (external, timer1, timer2, serial Input / Output)
- C-MOS technology
- Package outline QFP44-A1 / SDIP42

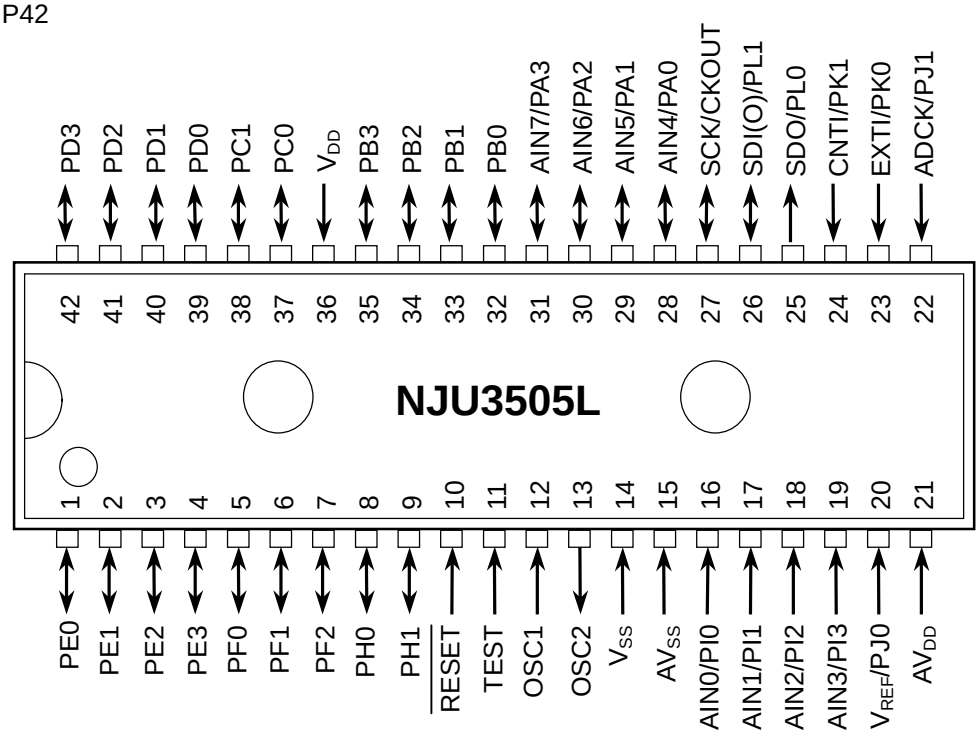
11/May/2001

■ PIN CONFIGURATION

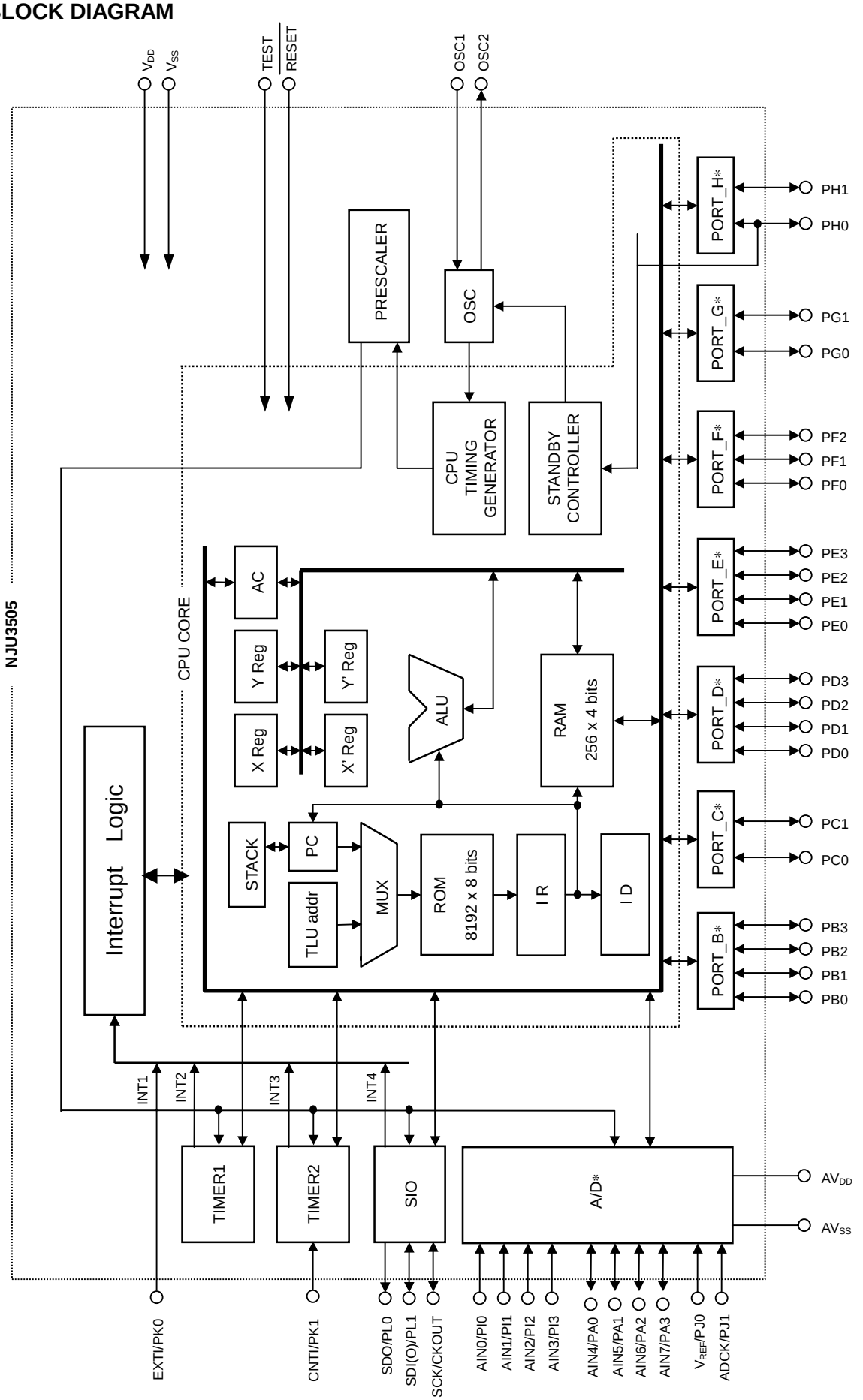
QFP44-A1



SDIP42



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No. NJU 3505F	No. NJU 3505L	SYMBOL	INPUT/OUTPUT	F U N C T I O N S
44 1 2	5 6 7	PF0 PF1 PF2	INPUT/OUTPUT INPUT/OUTPUT INPUT/OUTPUT	3-bit Input / Output PORTF. Selects a terminal circuit for each port from the following by the mask option. •C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance (ISP) •C-MOS Schmitt Trigger Input Terminal (IS) •C-MOS Output Terminal (OC)
3 4	X X	PG0 PG1	INPUT/OUTPUT INPUT/OUTPUT	2-bit Input / Output PORTG. Selects a terminal circuit for each port from the following by the mask option. •C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance (ISP) •C-MOS Schmitt Trigger Input Terminal (IS) •C-MOS Output Terminal (OC)
5 6	8 9	PH0 PH1	INPUT/OUTPUT INPUT/OUTPUT	2-bit Input / Output PORTH. Selects a terminal circuit for each port from the following by the mask option. •C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance (ISP) •C-MOS Schmitt Trigger Input Terminal (IS) •C-MOS Output Terminal (OC) When the ports are selected as the input terminal, PH0 operates also as RESTART signal input terminal to return from STANDBY mode, and PH1 operates also as the Edge Detector Terminal.
7	10	$\overline{\text{RESET}}$	INPUT	RESET Terminal. When the low level input-signal, the system is initialized.
8	11	TEST	INPUT	Maker Testing Terminal with Pull-down Resistance The terminal is recommended to connect to GND.
9 10	12 13	OSC1 OSC2	INPUT OUTPUT	Internal Oscillator Terminals. Connects a device selected from the ceramic or the crystal resonator, or the resistor, to these terminals for the internal oscillator. In the external clock operation, OSC1 is the external clock input terminal and OSC2 is normally open terminal.
11	14	V_{SS}	–	Power Source (0V)
12	15	AV_{SS}	–	Analog Block Power Source (0V) Connects to V_{SS} terminal when A/D converter is not used.

Note) INPUT/OUTPUT : Input or Output is selected by the mask option.
INOUT : Input or Output is changed by the program.
X : No terminals in the **NJU3505L**(SDIP package).

■ TERMINAL DESCRIPTION 2

No. NJU 3505F	No. NJU 3505L	SYMBOL	INPUT/OUTPUT	F U N C T I O N
13 14 15 16	16 17 18 19	AIN0 / PI0 AIN1 / PI1 AIN2 / PI2 AIN3 / PI3	INPUT INPUT INPUT INPUT	4-bit Input PORTI. Selects a function of either of 1) or 2) for PORTI by the mask option. 1) 4-bit Analog Input to A/D Converter. (AD) 2) 4-bit Input Terminals as PORTI. Selects a terminal circuit for each port from the following by the mask option. •C-MOS Input Terminal with Pull-up Resistance (ICP) •C-MOS Input Terminal (IC)
18	21	AV_{DD}	–	Analog Block Power source Connect to V_{DD} terminal when A/D converter is not used.
17 19	20 22	V_{REF} / PJ0 ADCK / PJ1	INPUT INPUT	2-bit Input PORTJ. Selects a function of either of 1) or 2) for PORTJ by the mask option. 1) Input terminal for A/D Converter. Reference Voltage Input Terminal : V_{REF} (AD) External Clock Input Terminal : ADCK (AD) 2) 2-bit Input Terminals as PORTJ. Selects a terminal circuit for each port from follows by the mask option. •C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance (ISP) •C-MOS Schmitt Trigger Input Terminal (IS)
20 21	23 24	EXTI / PK0 CNTI / PK1	INPUT INPUT	2-bit Input PORTK. Selects a function of either of 1) or 2) for PORTK by the mask option. 1) External Interrupt Input Terminal with Pull up resistance :EXTI (IIP / II) External Clock Input Terminal with Pull up resistance for Timer2 :CNTI (IIP,II) 2) 2-bit Input Terminals as PORTK. Selects a terminal circuit for each port from the following by the mask option. •C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance (ISP) •C-MOS Schmitt Trigger Input Terminal (IS)
22 23	25 26	SDO / PL0 SDI(O) / PL1	SDO :OUTPUT PL0 :OUTPUT SDI(O) :INOUT PL1 : INPUT/OUTPUT	2-bit Input / Output PORTL. Selects a function of either of 1) or 2) for PORTL by the mask option. 1) Serial Interface Function Serial Data Output Terminal : SDO (SO) Serial Data Input-Output Terminal with Pull-up Resistance : SDI(O) (SDP,SD) 2) 2-bit Input / Output Terminals as PORTL. Selects a terminal circuit for each port from the following by the mask option. •C-MOS Input Terminal with Pull-up Resistance (ICP) : PL1 •C-MOS Input Terminal (IC) : PL1 •C-MOS Output Terminal (OC) : PL0,PL1

Note) INPUT/OUTPUT : Input or Output is selected by the mask option.
INOUT : Input or Output is changed by the program.

■ TERMINAL DESCRIPTION 3

No. NJU 3505F	No. NJU 3505L	SYMBOL	INPUT/OUTPUT	F U N C T I O N
24	27	SCK / CKOUT	SCK :INOUT CKOUT : OUTPUT	Selects a function of either of 1) or 2) by the mask option. 1) Serial Clock Input or Output Terminal with Pull-up Resistance. (SCP, SC) 2) Clock Divided by Prescaler Output Terminal. Selects the dividing times of the clock in the prescaler by the mask option.
25 26 27 28	28 29 30 31	AIN4/PA0 AIN5/PA1 AIN6/PA2 AIN7/PA3	PA0: INOUT AIN4: INPUT PA1: INOUT AIN5: INPUT PA2: INOUT AIN6: INPUT PA3: INOUT AIN7: INPUT	4-bit Programmable Input / Output PORTA. Selects a function of either of 1) or 2) for PORTA by the mask option. 1) 4-bit Analog Input to A/D Converter. (AD) 2) 4-bit Input / Output Terminals as PORTA. These 4-bit terminals direction can be changed by the program as 4-Input or 4-Output. Use of Pull-up resistance for a terminal is in accordance with the mask option. •as Input : C-MOS Input Terminals (IOP) •as Output: Nch-FET Open-Drain Output Terminals (IO)
29 30 31 32	32 33 34 35	PB0 PB1 PB2 PB3	INOUT	4-bit Programmable Input / Output PORTB. These 4-bit terminals direction can be changed by the program as 4-Input or 4-Output. Use of Pull-up resistance for a terminal is in accordance with the mask option. •as Input : C-MOS Input Terminals (IOP) •as Output: Nch-FET Open-Drain Output Terminals (IO)
33	36	V_{DD}	–	Power Source (2.4V – 5.5V)
34 35	37 38	PC0 PC1	INPUT/OUTPUT	2-bit Input / Output PORTC. Selects a terminal circuit for each port from the following by the mask option. •C-MOS Input Terminal with Pull-up Resistance (ICP) •C-MOS Input Terminal (IC) •Nch-FET Open-Drain Output Terminal with Pull-up Resistance (ONP) •Nch-FET Open-Drain Output Terminal (ON)
36 37 38 39	39 40 41 42	PD0 PD1 PD2 PD3	INPUT/OUTPUT	4-bit Input / Output PORTD. Selects a terminal circuit for each port from the following by the mask option. •C-MOS Input Terminal with Pull-up Resistance (ICP) •C-MOS Input Terminal (IC) •C-MOS Output Terminal (OC)
40 41 42 43	1 2 3 4	PE0 PE1 PE2 PE3	INPUT/OUTPUT	4-bit Input / Output PORTE. Selects a terminal circuit for each port from the following by the mask option. •C-MOS Input Terminal with Pull-up Resistance (ICP) •C-MOS Input Terminal (IC) •C-MOS Output Terminal (OC)

Note)INPUT/OUTPUT : Input or Output is selected by the mask option.
INOUT : Input or Output is changed by the program.
"AD, IC, ICP, II, IIP, IO, IOP, IS, ISP, OC, ON, ONP, SC, SCP, SD, SDP, SO" are symbols using on MASK OPTION GENERATOR(MOG).

■ INTERNAL SYSTEM DESCRIPTION

The **NJU3505** is a C-MOS 4-Bit Single Chip Micro Controller consisted of Original CPU Core, Selectable Input-Output(I/O) Ports(MAX. 35 lines), Program ROM(8,192 bytes), Data RAM(256 nibbles), 8-Bit A/D Converter, 8-bit Serial Interface, Dual Timer/Counter(8-bit and 12-bit), Interrupt Control Circuit and Oscillator Circuit.

The CPU block in the **NJU3505** is consisted of ALU(Arithmetic Logic Unit) executing the binary adding, subtracting or logical calculating, AC(Accumulator), four Registers, STACK allowing the 8-level subroutine-nesting or Interrupt operation, Program Counter indicating 8192 addresses sequentially, and Timing generator.

The **NJU3505** can be applied to the various markets because of the rich and efficient instruction set(59 instructions), wide operating voltage range(2.4V to 5.5V), low operating current, and STANDBY function reducing the power supply current.

(1) INTERNAL REGISTER

- Accumulator(AC)

  Accumulator(AC) is structured by the 4-bit register. It holds a data or a result of calculation, and executes the shift-operation (ROTATE) or the data transference between the other registers and Data Memory (RAM).

  The accumulator condition is unknown on the “RESET” operation.

- X-register(X-reg)

  X-register(X-reg) operates as the 4-bit register. X-reg operates also as the RAM address pointer with Y-register.

  The X-reg condition is unknown on the “RESET” operation.

- Y-register(Y-reg)

  Y-register(Y-reg) operates as the 4-bit register or the RAM address pointer with X-reg.

  The Y-reg condition is unknown on the “RESET” operation.

- X'-register(X'-reg)

  X'-register(X’-reg) operates as the 4-bit register or a part of Program Memory(ROM) address pointer for looking data in the ROM(TRM instruction) up function.

  The X’-reg condition is unknown on the “RESET” operation.

- Y'-register(Y'-reg)

  Y'-register(Y’-reg) operates as the 4-bit register or the peripheral register number(PHYn) pointer.

  The Y’-reg condition is unknown on the “RESET” operation.

(2) INTERNAL FLAG

- RPC flag(RPC)

  RPC flag(RPC) changes the instruction table. Several instructions perform either of the dual tasks in accordance with the RPC flag condition. The RPC flag condition selects either of two couples of registers which are X- and Y- reg, or X'- and Y'-reg. X- or Y- reg is selected when the RPC flag condition is "0"(RPC=0). X'- or Y'- reg is selected when the RPC flag condition is "1"(RPC=1). The RPC flag condition is set to "1"(RPC=1) by SRPC instruction, and is set to “0”(RPC=0) by RRPC instruction.

  The RPC flag condition is set to “0” on the “RESET” operation.

- CARRY flag(CY)

  When the carry occurs after the adding calculation, the CARRY flag(CY) condition is set to "1"(CY=1), and when no carry, the CY flag condition is set to "0"(CY=0). When the borrow occurs after the subtracting calculation, the CY flag condition is set to "0"(CY=0), and when no borrow, the CY flag condition is set to "1"(CY=1). The bit-operation instruction operates the bit data rotation on the CY flag combined with the accumulator or the other register.

  The CY flag condition is set to "1"(CY=1) by SEC instruction and is set to "0"(CY=0) by CLC instruction. The CY flag condition is kept until the end of the next instruction executing cycle. The CY flag condition is unknown on the “RESET” operation.

- STATUS flag(ST)

STATUS flag(ST) is the conditional flag in accordance with the result of the instruction execution. Its condition is in accordance with follows:

1) to be same as CY flag condition.
2) to be set the condition to "0"(ST=0) when the result of the logical calculation(AND, OR, XOR, YNEA) is zero.
3) to be set the condition to "0"(ST=0) when the result of the comparison(CMP) is zero.

However, ST flag condition is always set to "1"(ST=1) except above three.

ST flag controls the branch operation. Branch instruction does not branch when ST flag condition is "0", and branches when ST flag condition is "1". ST flag condition is kept until the end of the next instruction executing cycle.

The ST flag condition is unknown on the “RESET” operation.

(3) FUNCTIONAL BLOCK

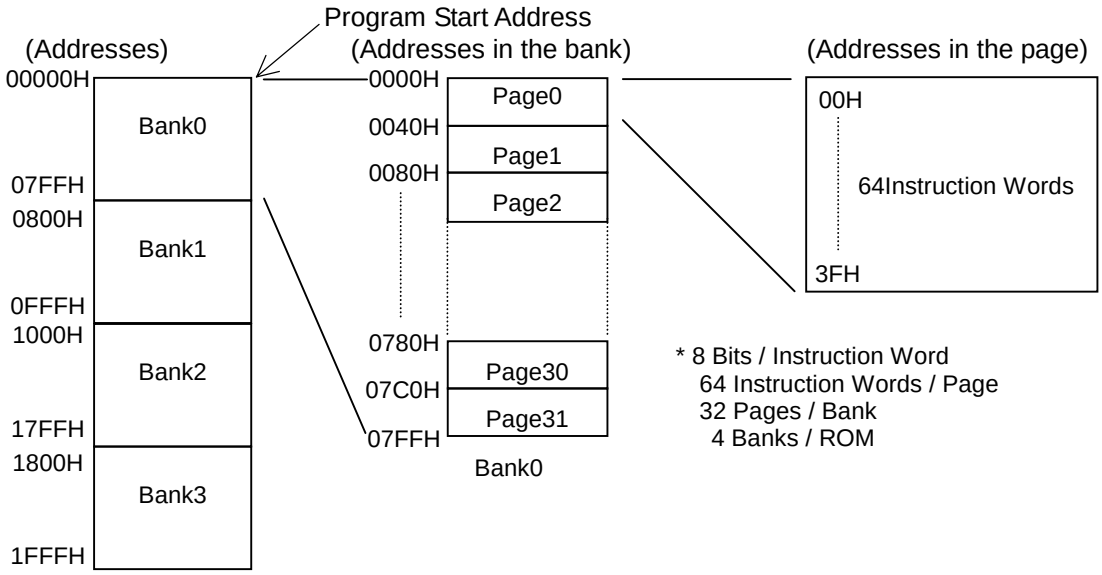
- ARITHMETIC LOGIC UNIT(ALU)

ARITHMETIC LOGIC UNIT(ALU) is a 4-bit binary paralleled calculation circuit operating binary addition, binary subtraction, comparison, logical AND, logical OR, exclusive OR, and SHIFT(Rotation). And it also can detect CARRY, BORROW or ZERO in accordance with the result of each calculation.

- PROGRAM MEMORY(ROM)

PROGRAM MEMORY(ROM) consists of 4 banks, a bank consists of 32 pages, and a page consists of 64 bytes memory capacity. Therefore the **NJU3505** prepares the 8192-byte ROM for the application program. The ROM address is indicated by the Program Counter (PC).

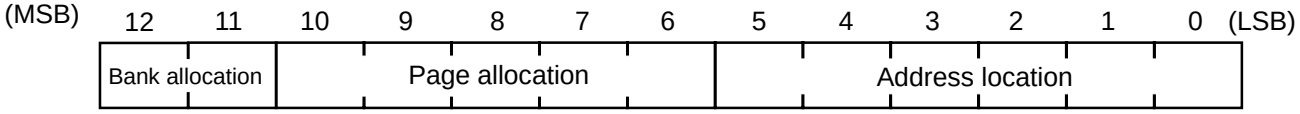
[PROGRAM MEMORY AREA]



■ PROGRAM COUNTER(PC)

PROGRAM COUNTER(PC) consisted of the 13-bit binary counter stores the address for the next operating instruction in ROM. Data figures limited from b0 to b5 on the PC indicate the address in a page, and data figures limited from b6 to b10 on the PC indicate the page in a bank, and data figures limited from b11 to b12 on PC indicates a bank in ROM. Although the ROM address can be indicated 8192 addresses continuously, the target address of JMP instruction is restricted by Paging structure in ROM. The target address of JPL or CALL instruction is restricted by Banking structure in ROM.

The PC condition is set to “0” on the “RESET” operation.



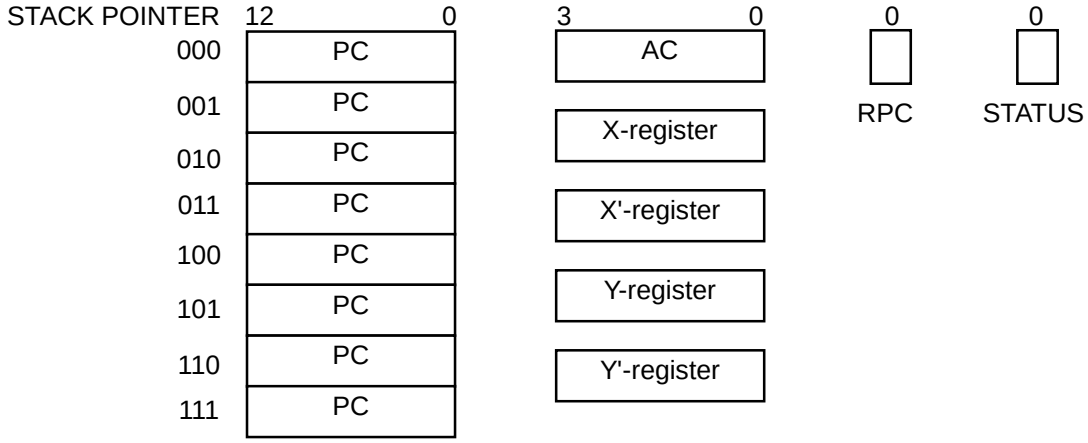
JMP instruction can branch to the optional address in the page. The target address is indicated by the data figures limited from b0 to b5(6 bits) on PC as shown in above. The paging structure can reduce the program size in ROM and the JMP instruction execution time against JPL instruction because JMP instruction is consisted of one byte(8 bits) length. JPL and CALL instructions can branch to the optional address without considering the paging structure, because they consist of two bytes(16 bits) length including the 11 bits of PC. But JPL and CALL instructions can not branch between the banks in ROM.

The memory bank register(PHY15) on the peripheral register table0 selects a bank in ROM. When the branch target address is not found in the bank, the memory bank register requires to change the bank number.

- STACK

STACK consists of three types of registers which are the 8 by 13 bits, the 5 by 4 bits, and the 2 by 1 bit registers. The registers of STACK hold the data of PC automatically when the interrupt routine or the subroutine is called. The 5 by 4 bits registers of STACK hold the data of the internal registers automatically when the interrupt operation is executed. The 2 by 1 bit registers of STACK hold the data of the internal flag automatically when the interrupt operation is executed. In the return (RET or RETI) operation, PC, the internal registers, and the internal flags registers get the held data from STACK automatically.

[For branch(CALL) and interrupt operation] [For interrupt operation]



■ STACK POINTER(SP)

STACK POINTER(SP) consists of the 3 bits binary counter. SP indicates the number of next operating position in the STACK. It counts one up(increment) after the subroutine call(CALL) or the interrupt operation, and it counts one down(decrement) after the return(RET or RETI) operation.

Data storing operation to STACK after that SP overflowed (over than 7) or under flowed(under than 0), breaks the former held data in STACK. Therefore the subroutine nesting level must be cautioned in the application program.

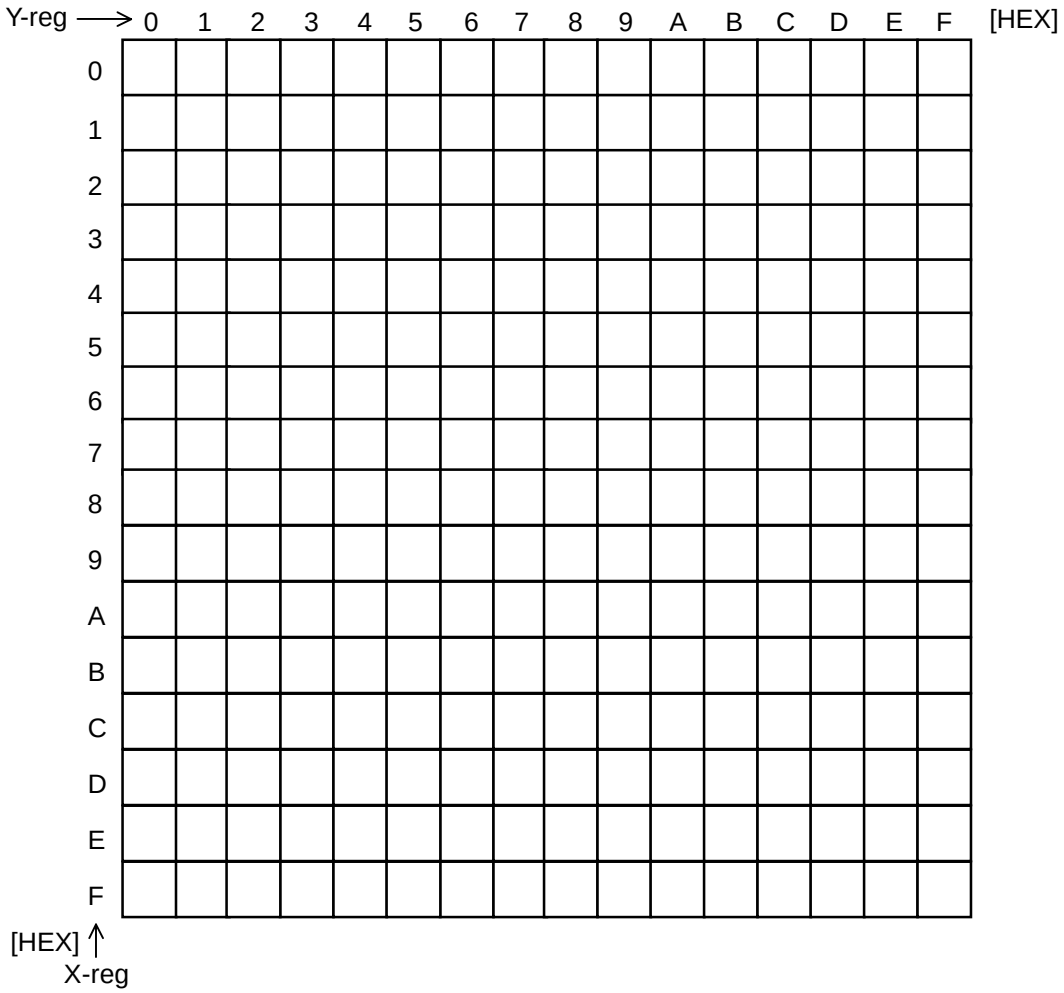
SP condition is set to "0" on “RESET” operation.

- DATA MEMORY(RAM)

DATA MEMORY(RAM) is formed with the 4-bit length a word. The **NJU3505** prepares 256 words(1024 bits) RAM. The data formed with the 4-bit length a word can be read/written from/to RAM, and the data formed with the 1-bit length in a word can be set, reset, or tested by the bit-operation instruction.

The RAM address is indicated indirectly by X-reg and Y-reg.

[RAM ADDRESS MAP]



- PERIPHERAL REGISTERs(PH)

PERIPHERAL REGISTERs(PH) controlling I/O Ports or the ROM address are selected by the data in Y'-reg.

Two Peripheral Register tables called as table0 and table1 in the **NJU3505** consist of 32 registers totally.

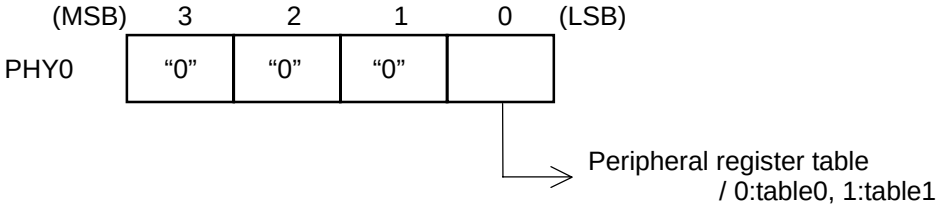
The Peripheral Register assigned for each I/O Port can get the signal data from the external application by reading operation, or can output the signal data to the external application by writing operation in accordance with the type of input or output selected by the mask option. Although the data can be read from the Peripheral Register assigned as the Output, it sometimes takes the incorrect data of the Output Port.

<<Peripheral Register Table Change>>

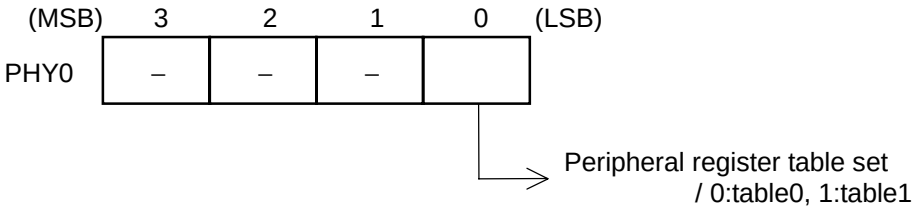
When LSB(b0) of the peripheral register table change register(PHY0) is written “0”, the table0 is selected. When LSB of PHY0 is written “1”, the table1 is selected.

The table0 is selected on “RESET” operation.

[Reading from the Peripheral Register Table Change Register (PHY0)]



[Writing to the Peripheral Register Table Change Register (PHY0)]



[PERIPHERAL REGISTER TABLE0]

Y'-register	Register No.	Peripheral Register Name	Number of Port	Write or Read *1	Data in Reset
0H	PHY0 (00H)	Table Change Register	1	WR	0
1H	PHY1 (01H)	Serial Input/Output Control Register	3	WR	0 *3
2H	PHY2 (02H)	Serial Input/Output Shift Register	8	WR	0 *3
3H	PHY3 (03H)	Timer1/Prescaler Control Register	3	WR	0
4H	PHY4 (04H)	Initial Value Register1 / Timer Counter1	8	WR	0
5H	PHY5 (05H)	Timer2 Control Register	4	WR	0 *6
6H	PHY6 (06H)	Initial Value Register2 / Timer Counter2	8	WR	0
7H	PHY7 (07H)	A/D Converter Control Register1	4	WR	0 *4
8H	PHY8 (08H)	A/D Converter Output Register	8	R	0
9H	PHY9 (09H)	Interrupt Control Register	4	WR	0
AH	PHY10 (0AH)	A/D Coverter Control Register2	1	WR	0 *4
BH	PHY11 (0BH)	Initial Value Register2 / Timer Counter2	4	WR	0
CH	PHY12 (0CH)				
DH	PHY13 (0DH)	ROM Addressing Register L	4	WR	unknown
EH	PHY14 (0EH)	ROM Addressing Register H	1	WR	unknown
FH	PHY15 (0FH)	Memory Bank Register	2	WR	0 *2

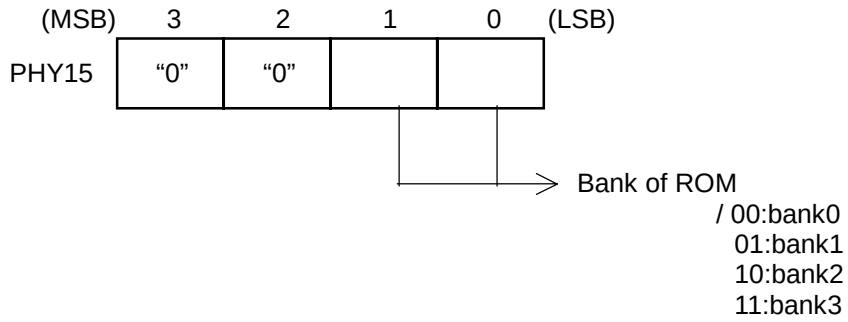
[PERIPHERAL REGISTER TABLE1]

Y'-register	Register No.	Peripheral Register Name	Number of Port	Write or Read *1	Data in Reset
0H	PHY0 (00H)	Table Change Register	1	WR	0
1H	PHY17 (11H)	PORTA Output or PORTA Input	4	WR	0 *4
2H	PHY18 (12H)	PORTB Output or PORTB Input	4	WR	0
3H	PHY19 (13H)	PORTC Output or PORTC Input	2	W / R	0
4H	PHY20 (14H)	PORTD Output or PORTD Input	4	W / R	0
5H	PHY21 (15H)	PORTE Output or PORTE Input	4	W / R	0
6H	PHY22 (16H)	PORTF Output or PORTF Input	3	W / R	0
7H	PHY23 (17H)	PORTG Output or PORTG Input	2	W / R	0
8H	PHY24 (18H)	PORTH Output or PORTH Input	2 / 3	W / R	0
9H	PHY25 (19H)	PORTI Input	4	R	*4
AH	PHY26 (1AH)	PORTJ Input	2	R	*5
BH	PHY27 (1BH)	PORTK Input	2	R	*6
CH	PHY28 (1CH)	PORTL Output or PORTL Input	2 / 1	W / R	0 *3
DH	PHY29 (1DH)	Programmable Input/Output Port Control Register	2	WR	0
EH	PHY30 (1EH)				
FH	PHY31 (1FH)				

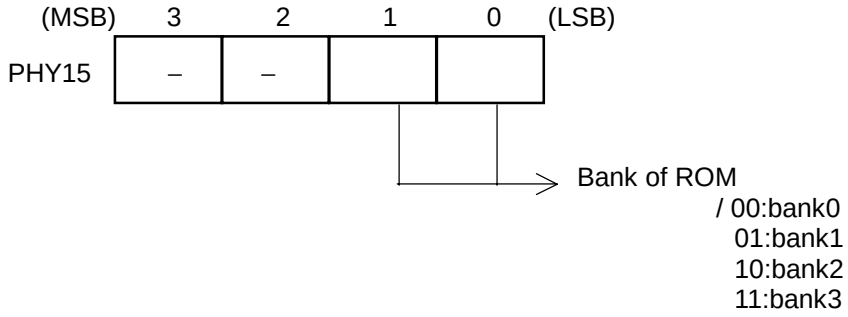
*1
- W : Write only
- R : Read only
- WR : Read and Write
- W / R : Fixed as Read or Write by the mask option

*2 Memory Bank Register(PHY15) selects the Bank0 in ROM when lower 2-bit of PHY15 is written “00”, and selects the Bank1 when lower 2-bit of PHY15 is written “01”, and selects the Bank2 when lower 2-bit of PHY15 is written “10”,and selects the Bank3 when lower 2-bit of PHY15 is written “11”.
The Bank0 is selected on “RESET” operation.

[Reading from the Memory Bank Register (PHY15)]

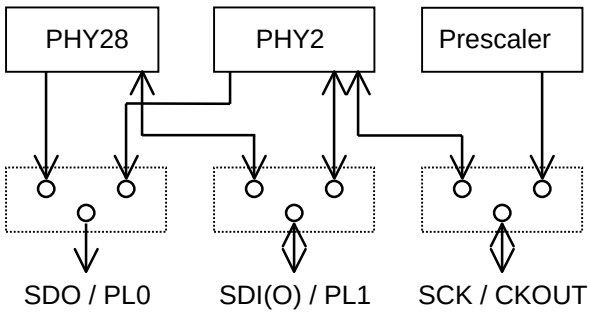


[Writing to Memory Bank Register (PHY15)]

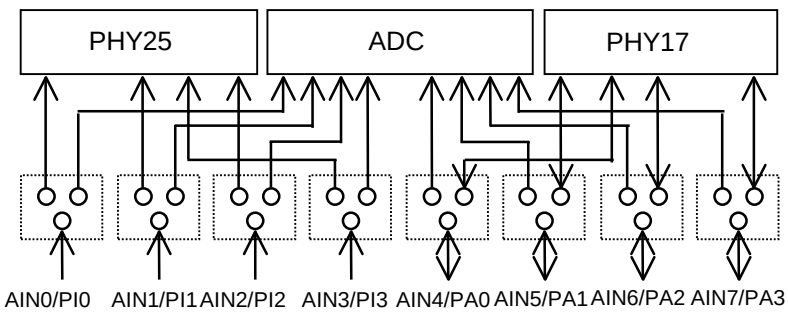


Note) Bank0 Address : 0000H – 07FFH,
Bank1 Address : 0800H – 0FFFH
Bank2 Address : 1000H – 17FFH
Bank3 Address : 1800H – 1FFFH

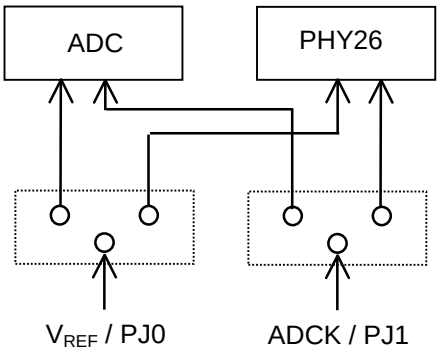
*3 Wiring of terminals
The mask option selects a terminal type from SDO/PL0, SDI(O)/PL1 or SCK/CKOUT as shown in right.



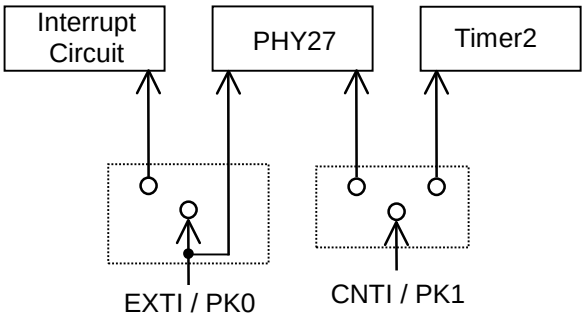
*4 Wiring of terminals
The mask option selects a terminal type from AIN0/PI0, AIN1/PI1, AIN2/PI2, AIN3/PI3, AIN4/PA0, AIN5/PA1, AIN6/PA2, AIN7/PA3 as shown in right.



*5 Wiring of terminals
The mask option selects a terminal type from V_{REF}/PJ0, or ADCK/PJ1 as shown in right.



*6 Wiring of terminals
The mask option selects a terminal type from EXTI/PK0, or CNTI/PK1 as shown in right.



- ROM ADDRESSING REGISTER(PHY13, PHY14)

ROM ADDRESSING REGISTERS (PHY13. PHY14) indicates the address of ROM with Accumulator and X'-reg for the data transference operation (TRM) from ROM to RAM.

The PHY13 and PHY14 condition are unknown on “RESET” operation. The lower a bit(b0) in PHY14 is used as the ROM ADDRESSING and higher 3 bits(b1,b2,b3) are not used,

[ROM ADDRESSING]

no used			A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
b3	b2	b1	b0	b3	b2	b1	b0	b3	b2	b1	b0	b3	b2	b1	b0
PHY14				PHY13				X’				AC			

■ INPUT OUTPUT PORT

The **NJU3505** prepares 21 Input-Output lines and 14 dual-function lines for the interface to an external application circuit. All lines are assigned to each Peripheral Register.

Data reading operation from the peripheral register can input the actual signals through the input terminal. Data writing operation to the peripheral register can output the actual signals through the output terminal.

[PORT FUNCTION TABLE]

PORT NAME	FUNCTION	INPUT/OUTPUT
PORTA	Input / Output port or AIN4 – AIN7	Programmable Input / Output PORT(4-bit).
PORTB	Input / Output port	Programmable Input / Output PORT(4-bit).
PORTC – PORTH	Input / Output port	Input / Output selectable ports by the mask option.
PORTI	Input port or AIN0 – AIN3	Input
PORTJ(PJ0)	Input port or V_{REF}	Input
PORTJ(PJ1)	Input port or ADCK	Input
PORTK(PK0)	Input port or EXTI	Input
PORTK(PK1)	Input port or CNTI	Input
PORTL(PL0)	Output Port or SDO	output
PORTL(PL1)	Input / Output port or SDI(O)	Input / Output selectable ports by the mask option.

Note1) PORTG is not prepared on the **NJU3505**L(SDIP package).
Note2) Pull-up resistance is selected by the mask option.(refer ■ INPUT OUTPUT TERMINAL TYPE)

(1) INPUT OUTPUT PORT

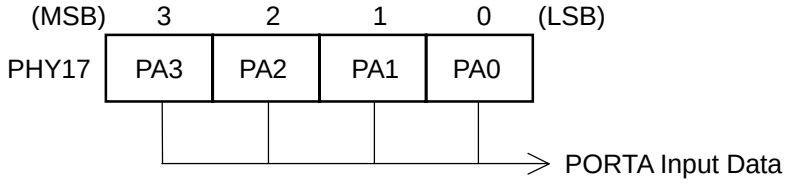
- PORTA(PA0 – PA3)

PORTA is a 4-bit programmable input-output PORT. It operates also as the multiplexed 4-channel analog signal input terminals (AIN4 to AIN7) to the internal A/D converter by the mask option. It is set as the output when LSB of the programmable input/output control register (PHY29) is set to “1”, and is set as the input when LSB of PHY29 is set to “0”. When the PORT is set as the output, the 4-bit signals are output through the output terminals by writing data into the peripheral register assigned for PORTA (PHY17). PHY17 as the output register should be written the output data before the PORTA is set as the output by PHY29, because the conditions of the output terminals are unknown while the output data is not written in PHY17. When this PORT is set as the input, the 4-bit external signals are gotten directly through the input terminals by reading data from PHY17. PHY17 can be written or read independent of the state of PHY29 as the input or output.

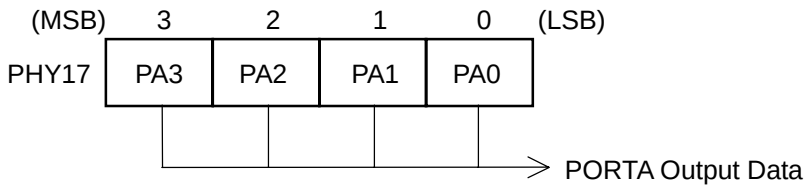
PORTA is set as the input in accordance with the state of PHY29 set to “0” on the “RESET” operation.

Though the output circuit is Nch open drain type, the C-MOS input buffer is connected to the same terminal. Therefore, the operating current of the chip by the short circuit current when the middle level voltage between V_{DD} and V_{SS} is input to this terminal.

[READING PORTA INPUT DATA (PHY17)]



[WRITING PORTA OUTPUT DATA (PHY17)]

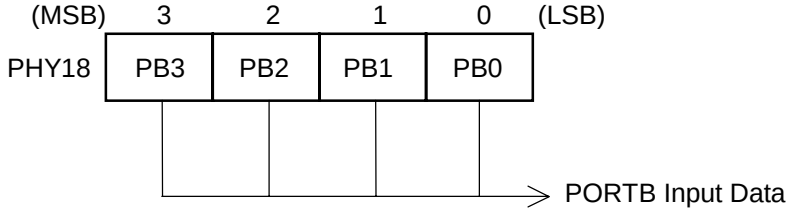


- PORTB(PB0 – PB3)

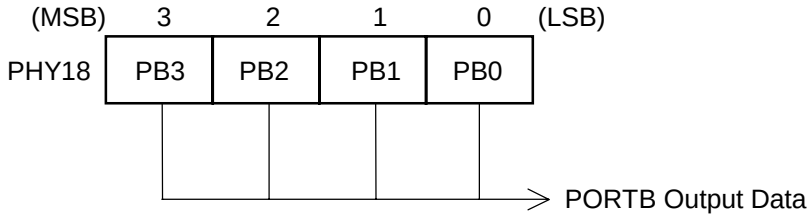
PORTB is a 4-bit programmable input-output PORT. It is set as the output when the second bit (b1) of the programmable input/output control register (PHY29) is set to “1”, and is set as the input when “b1” of PHY29 is set to “0”. When the PORT is set as the output, the 4-bit signals are output through the output terminals by writing data into the peripheral register assigned for PORTB (PHY18). PHY18 as the output register should be written the output data before the PORTB is set as the output by PHY29, because the conditions of the output terminals are unknown while the output data is not written in PHY18. When this PORT is set as the input, the 4-bit external signals are gotten directly through the input terminals by reading data from PHY18. PHY18 can be written or read independent of the state of PHY29 as the input or output.

PORTB is set as the input in accordance with the state of PHY29 set to “0” on the “RESET” operation.

[READING PORTB INPUT DATA (PHY18)]



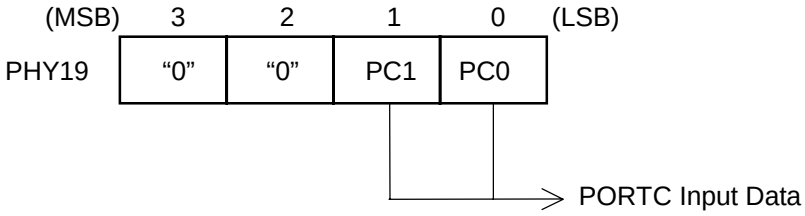
[WRITING PORTB OUTPUT DATA (PHY18)]



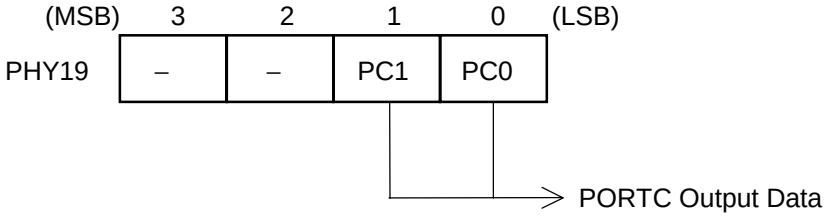
- PORTC(PC0, PC1)

PORTC is a 2-bit input-output PORT. The input or the output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTC register(PHY19). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY19.

[READING PORTC INPUT DATA (PHY19)]



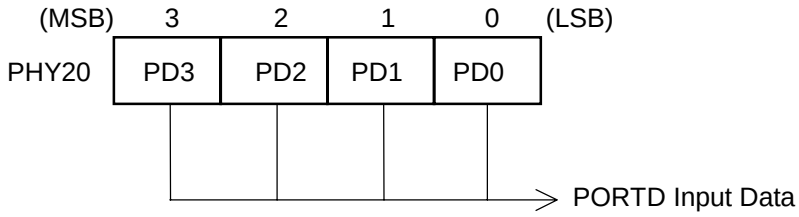
[WRITING PORTC OUTPUT DATA (PHY19)]



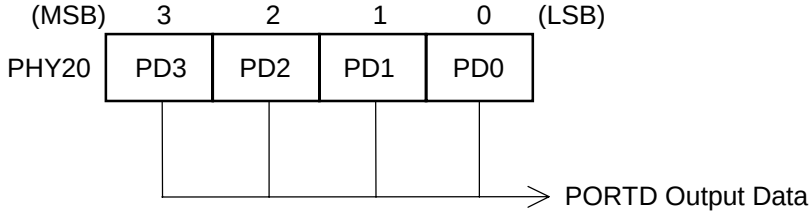
- PORTD(PD0 – PD3)

PORTD is a 4-bit input-output PORT. The input or the output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTD register (PHY20). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY20.

[READING PORTD INPUT DATA (PHY20)]



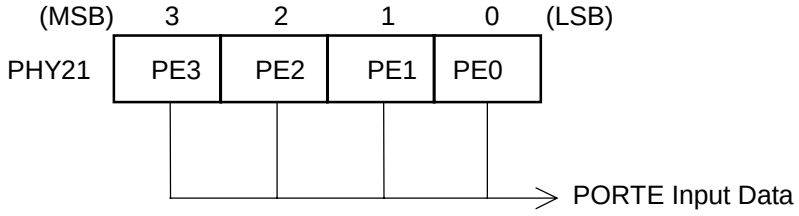
[WRITING PORTD OUTPUT DATA (PHY20)]



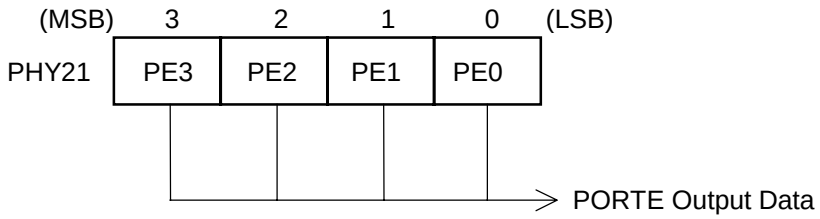
- PORTE(PE0 – PE3)

PORTE is a 4-bit input-output PORT. The input or the output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTE register (PHY21). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY21.

[READING PORTE INPUT DATA (PHY21)]



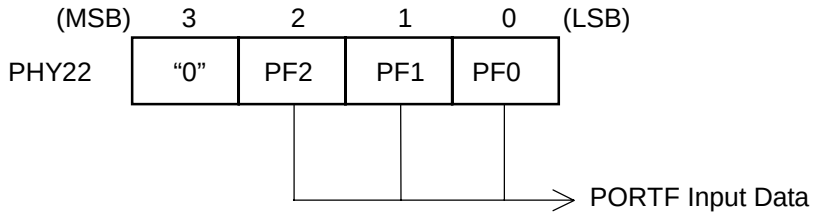
[WRITING PORTE OUTPUT DATA (PHY21)]



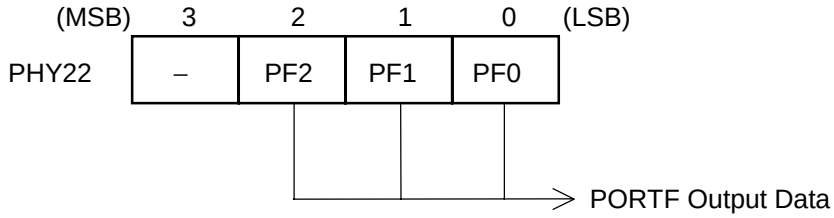
- PORTF(PF0 – PF2)

PORTF is a 3-bit input-output PORT. The input or the output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTF register (PHY22). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY22.

[READING PORTF INPUT DATA (PHY22)]



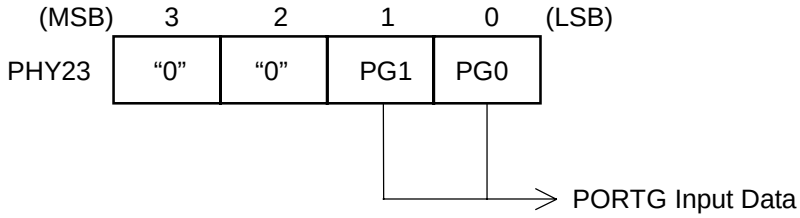
[WRITING PORTF OUTPUT DATA (PHY22)]



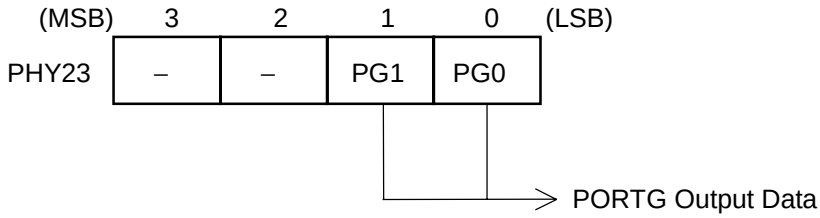
- PORTG(PG0, PG1)

PORTG is a 2-bit input-output PORT. The input or output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTG register (PHY23). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY23.

[READING PORTG INPUT DATA (PHY23)]



[WRITING PORTG OUTPUT DATA (PHY23)]



Note) PORTG is not prepared on the **NJU3505L**(SDIP package).

- PORTH(PH0, PH1)

PORTH is a 2-bit input-output PORT. The input or the output is selected for each bit by the mask option. When the port is set as the output, the signal is output through the output terminal by writing data to the PORTH register (PHY24). When the port is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY24. When this PORTH is set as the input, these two ports perform the extra functions as follows:

a. PH0 TERMINAL

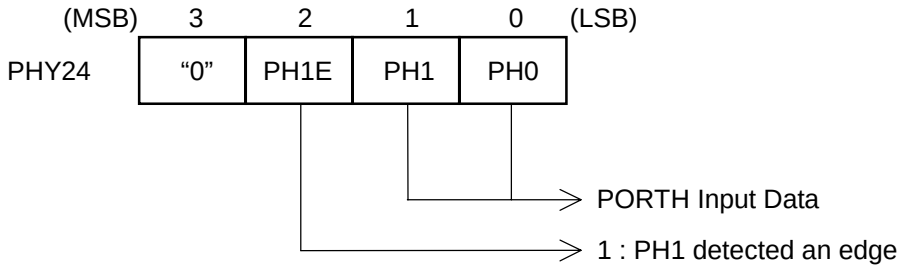
PH0 terminal performs the extra function as the restart signal input terminal to return from the "STANDBY" mode. When the rising edge of the signal from the external circuit is input into the PH0 terminal in mode of "STANDBY", the "STANDBY" mode is released and the CPU starts the execution again from the suspended address of the program. (refer ■STANDBY FUNCTION)

b. PH1 TERMINAL

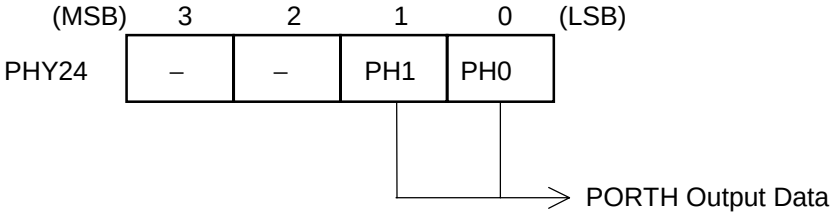
PH1 terminal performs the extra function as the edge detector terminal. When the PH1 terminal detects the edge of the signal from the external circuit, the third bit(b2) condition of PHY24 is set to "1". The “b2” of PHY24 is set to “1” even when the edge is input during the “STANDBY” mode. The condition of “b2” is kept until the writing operation to PHY24.

The polarity as low to high or high to low of the input signal edge can be selected by the mask option.

[READING PORTH INPUT DATA (PHY24)]



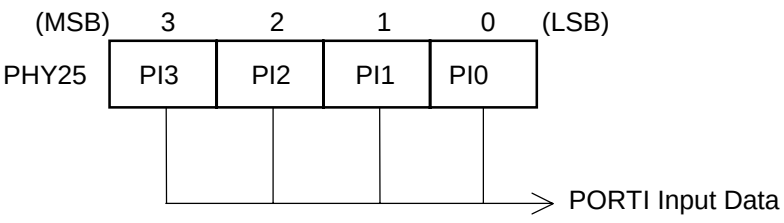
[WRITING PORTH OUTPUT DATA (PHY24)]



- PORTI(PI0 – PI3)

PORTI is a 4-bit input PORT. It operates also as the multiplexed 4-channel analog signal input terminals (AIN0 – AIN3) to the internal A/D converter by the mask option. When the PORTI is set as the input PORT, the four external signals are gotten directly though the input terminals by reading data from PHY25.

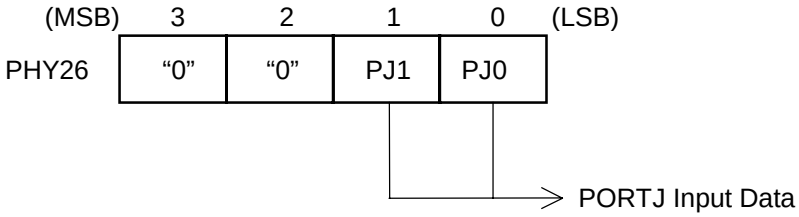
[READING PORTI INPUT DATA (PHY25)]



- PORTJ(PJ0, PJ1)

PORTJ is a 2-bit input PORT. It operates also as V_{REF} and ADCK terminals of the internal A/D converter by the mask option. When the PORTJ is set as the input PORT, the two external signals are gotten directly through the input terminals by reading data from PHY26.

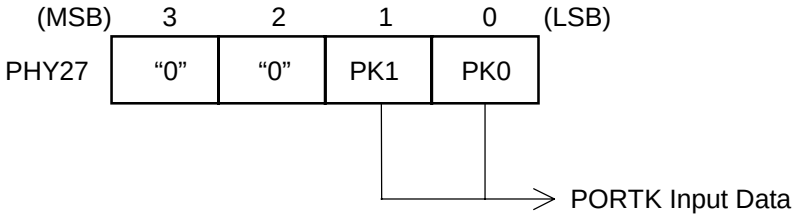
[READING PORTJ INPUT DATA (PHY26)]



- PORTK(PK0, PK1)

PORTK is a 2-bit input PORT. It operates also as EXTI input terminal for the external interrupt input and CNTI terminal for the event counter external clock input by the mask option. When the PORTK is set as the input PORT, the two external signals are gotten directly from the input terminals by reading data from PHY27.

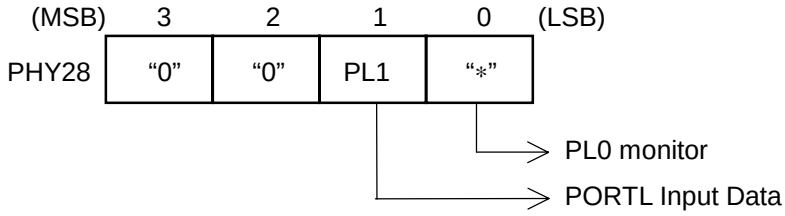
[READING PORTK INPUT DATA (PHY27)]



- PORTL(PL0, PL1)

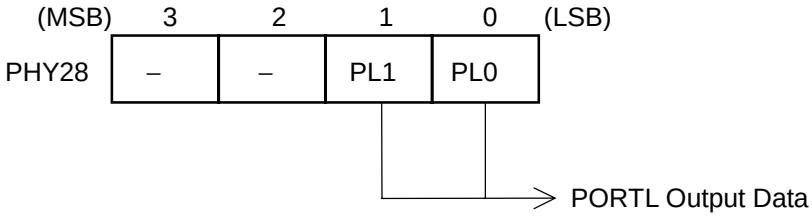
PORTL is a 2-bit input-output PORT. It operates also as SDO and SDI(O) terminals for the 8-bit serial interface by the mask option. When the PORTL is selected as the input-output PORT, PL0 is fixed as the output and PL1 can be selected as the input or the output by the mask option. When the PORTL is selected as the output, the two signals are output through the output terminals to the external circuit by writing data to the PORTL register(PHY28). When PL1 is selected as the input, the external signal is gotten directly through the input terminal by reading data from PHY28.

[READING PORTL INPUT DATA (PHY28)]



When PL0 is output, its output condition can be monitored.

[WRITING PORTL OUTPUT DATA (PHY28)]

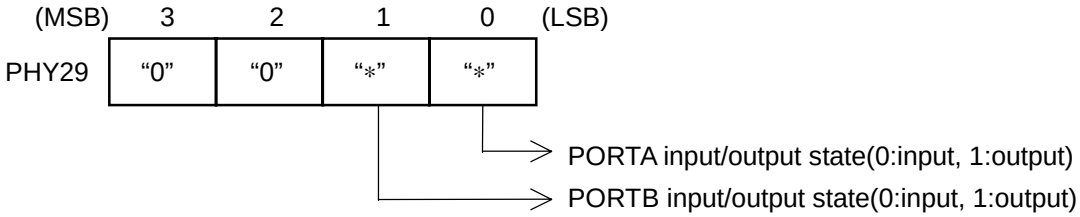


- PROGRAMMABLE INPUT/OUTPUT PORT CONTROL REGISTER(PHY29)

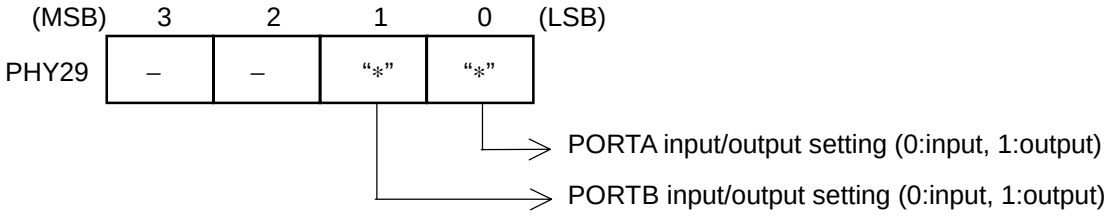
Programmable Input / Output Port Control Register(PHY29) is a peripheral register to set the programmable input/output PORTs(PORTA and PORTB) as either the input or the output. All bits in PORTA are set as the output when LSB(b0) of PHY29 is set to “1”. All bits in PORTA are set as the input when “b0” of PHY29 is set to “0”. All bits in PORTB are set as the output when b1 of PHY29 is set to “1”. All bits in PORTB are set as the input when “b1” of PHY29 is set to “0”.

PORTA and PORTB are set as the input in accordance with the state of PHY29 which is set to “0” on the “RESET” operation.

[READING Programmable Input / Output Port Control Register(PHY29)]



[WRITING Programmable Input / Output Port Control Register(PHY29)]



(2) PROGRAMMABLE INPUT/OUTPUT PORT OPERATION

a. The output operation example

PB0 and PB1 of PORTB output “H”, and PB2 and PB3 of PORTB output “L”.

```
        :
SRPC                ;
LDI     Y,0         ;  ) Peripheral table is
LDI     A,%0001     ;  )   set as the table1
TAP                 ;  )
LDI     Y,2         ;PHY18 is pointed
LDI     A,%0011     ;"0011" is stored into Accumulator
TAP                 ;Data in Accumulator is transmitted to PHY18
                    ;    (PORTB output register)
LDI     Y,13        ;PHY29 is pointed                          ) PORTB is
LDI     A,%0010     ;"0010" is stored into Accumulator         )   set as the output
TAP                 ;Data in Accumulator is transmitted to PHY29 )
        :
```

b. The input operation example

Accumulator gets the input data from PORTB.

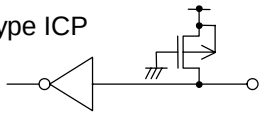
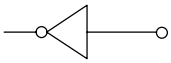
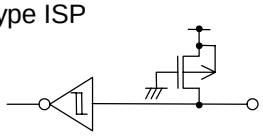
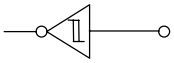
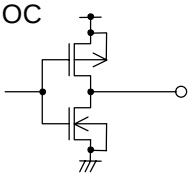
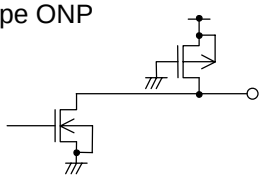
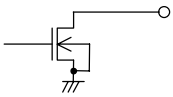
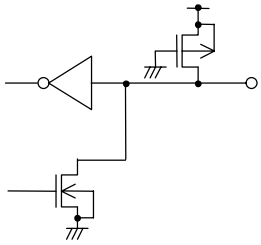
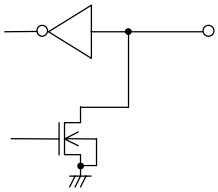
```
        :
SRPC                ;
LDI     Y,0         ;  ) Peripheral table is
LDI     A,%0001     ;  )   set as the table1
TAP                 ;  )
LDI     Y,13        ;PHY29 is pointed                          ) PORTB is
LDI     A,%0000     ;"0000" is stored into Accumulator         )   set as the input
TAP                 ;Data in Accumulator is transferred to PHY29 )
LDI     Y,2         ;PHY18 is pointed
TPA                 ;The input data from PHY18 is transferred to Accumulator
        :
```

The signal from PB0 terminal is stored into the LSB of Accumulator, the signal from PB1 terminal is stored into the b1 of Accumulator, the signal from PB2 terminal is stored into the b2 of Accumulator, and the signal from PB3 terminal is stored into the b3 of Accumulator.

■ INPUT OUTPUT TERMINAL TYPE

Each terminal of PORTA, B, C, D, E, F, G, H, I, J, K, and L can select a terminal type from the following by the mask option which is the same mask of the program coding into ROM and the others. But PORTI, J, and K select only the input terminal type. PL0 of PORTL selects only the output terminal type.

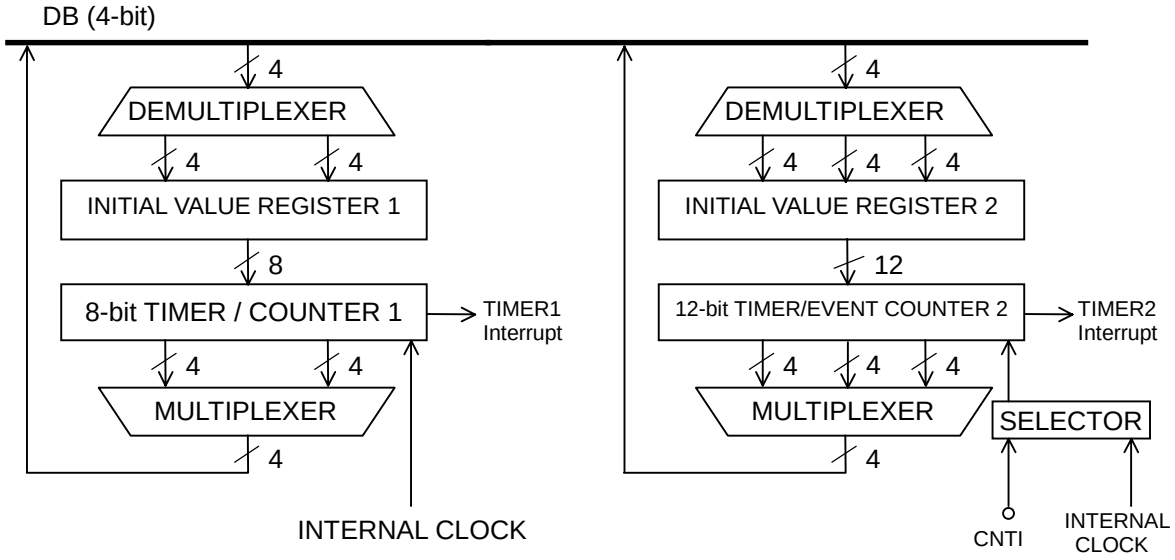
INPUT OUTPUT TERMINAL TYPES

	Types	With Pull-up	Without Pull-up	Terminals
INPUT TERMINAL	C-MOS	Type ICP 	Type IC 	PC0, PC1, PD0–PD3, PE0–PE3, AIN0/PI0– AIN3/PI3, SDI(O)/PL1
	SCHMITT TRIGGER	Type ISP 	Type IS 	PF0–PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1
OUTPUT TERMINAL	C-MOS		Type OC 	PD0–PD3, PE0–PE3, PF0–PF2, PG0, PG1, PH0, PH1, SDO/PL0, SDI(O)/PL1
	N-channel (Nch) OPEN DRAIN	Type ONP 	Type ON 	PC0, PC1
PROGRAMMABLE INPUT OUTPUT TERMINAL	C-MOS INPUT / N-channel (Nch) OPEN DRAIN OUTPUT	Type IOP 	Type IO 	AIN4/PA0– AIN7/PA3, PB0–PB3

■ TIMER

The **NJU3505** prepares a couple of Programmable Timer / Counter(Timer1, Timer2) consisted of the 8-bit and 12-bit binary counter.

[Structure of Timer / Counter]



PHY3 | – | b2 | b1 | b0 |

TIMER1 CONTROL REGISTER

PHY5 | b3 | b2 | b1 | b0 |

TIMER2 CONTROL REGISTER

Timer1 counts only the internal clock and Timer2 counts either of the internal clock or the external clock in accordance with the condition of bit2(b2) of the Timer2 Control Register(PHY5). The initial value of the counter can be set the optional value by the program which instructs to write the data(a value of the time-interval or the event-count) into the Initial Value Register(Timer1 or Timer2 is set the each value independently). In enabling the timer1 interrupt, when the Timer1 counter counts from “FF” to “00” (overflow), the timer1 interrupt request occurs and the internal interrupt process starts the own operation. In enabling the timer2 interrupt, when the Timer2 counter counts from “FFF” to “000” (overflow), the timer2 interrupt request occurs and the internal interrupt process starts the own operation.

In the repeat mode of the Timer operation, when the counter overflows, the initial value is loaded into the counter automatically and the counter continues the count from the loaded initial value(Auto re-load function: See the repeat mode of the Timer operation timing chart). In the single mode of the Timer operation, when the counter overflows, the count is stopped (See the single mode of the Timer operation timing chart). For starting the count operation again, the start bit (LSB) of the Timer1 or Timer2 Control Register must be set to “1”. The latest initial value is set into the counter and the counter starts the count.

In enabling the interrupt operation, when the counter overflows, the Timer / Counter overflow flag is set to "1" and the internal interrupt process starts to the own operation. In disabling the timer interrupt, the Timer / Counter overflow flag is not set. The Timer / Counter overflow flag is initialized by the Timer Start or the Reset signal.

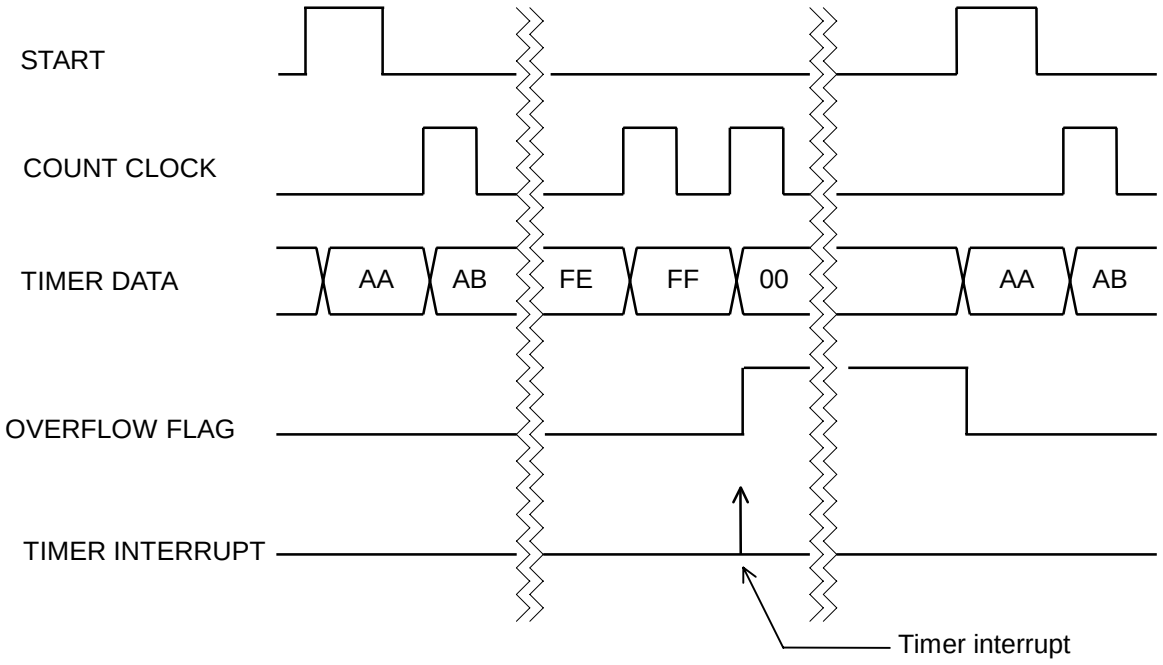
The internal clock into the counter is the divided clock from the internal prescaler. The frequency of the clock can be selected by the mask option from follows which are the dividing numbers based on the inverse of the 1-instruction executing period($1/f_{OSC}$ x 6).

1/2, 1/4, 1/8, 1/16, 1/32,1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048,1/4096

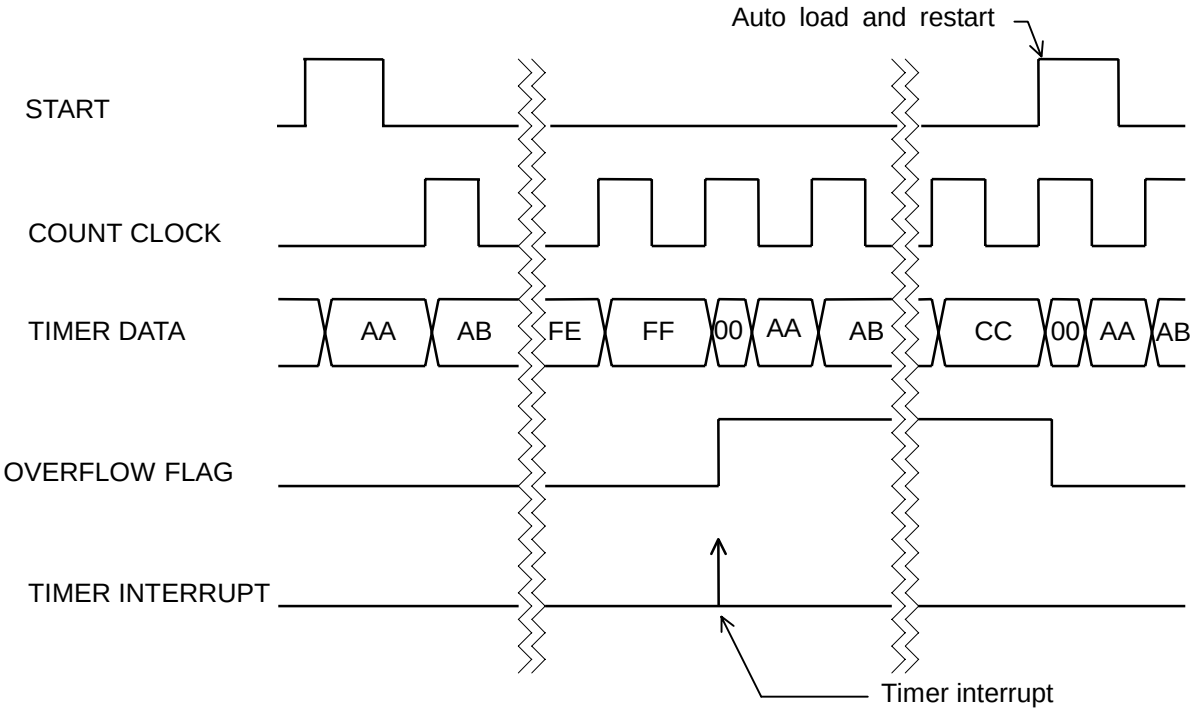
When the bit2(b2) of the Timer1 / Prescaler Control Register is set to "1", the prescaler generating the internal count clock is stopped the operation. As the result, Timer / Counter stops the count operation.

In the external clock operation of Timer2, the external clock must be input to CNTI terminal. The Timer2 Control Register selects either the internal clock operation or the external clock operation.

[THE SINGLE MODE OF THE TIMER OPERATION TIMING] (The initial value is set to "AAh")



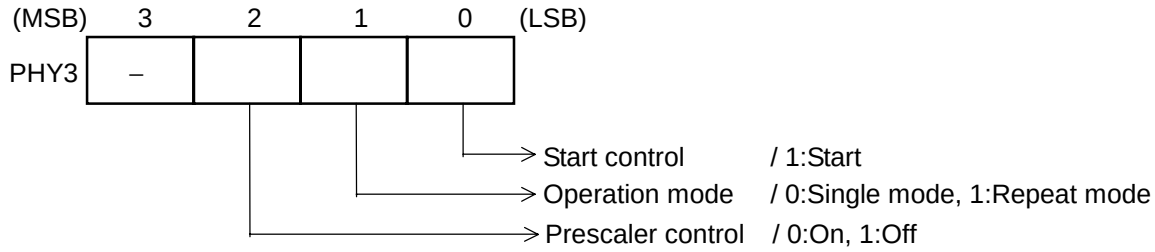
[THE REPEAT MODE OF THE TIMER OPERATION TIMING] (The initial value is set to "AAh")



* The difference between Timer1 and Timer2 counters is bit-number of counter.
  Timer1 is 8bits. Timer2 is 12bits.

- TIMER1 / PRESCALER CONTROL REGISTER { PHY3 ; (Y'=3, Peripheral register table 0) }

[Writing to the Timer1 / Prescaler Control Register]

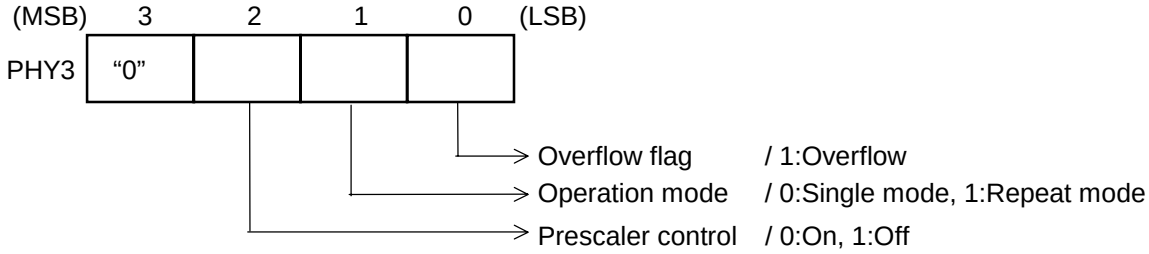


EX.) An example of the start procedure in the single mode and the internal clock operation.

```
        :
        :
SRPC            ;
LDI     Y,3     ;PHY3(Timer1/Prescaler Control Register) is pointed.
LDI     A,%0000 ;"0000"(BIN) is stored to accumulator          } Single mode,
TAP             ;Data is transferred from accumulator to PHY3 } Prescaler is enable
LDI     A,%0001 ;"0001"(BIN) is stored to accumulator          }
TAP             ;Data is transferred from accumulator to PHY3 } The count is started.
        :
        :
```

Remarks) When the prescaler generating the internal count clock is stopped the operation, Timer is also stopped. But the data in the counter is kept. Therefore Timer can continue to count from the kept condition of the counter when the prescaler is started the operation again. However, the clocks from the prescaler are delivered to Serial I/O, CKOUT terminal and A/D converter controller, therefore the prescaler requires careful operation, especially stop or start.
When the prescaler is started the operation again after it was stopped, it is reset and start to count from “zero”.

[Reading from the Timer1 / Prescaler Control Register]



EX.) An example of the overflow in the single mode and the internal clock operation.(The data of the Timer1 / Prescaler Control Register is "0001"(BIN).)

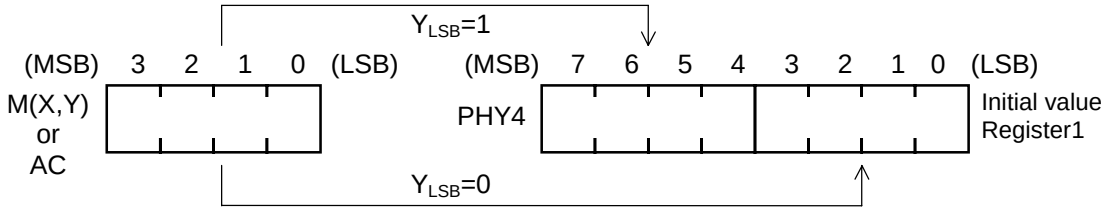
```
        :
        :
SRPC            ;
LDI     Y,3     ;PHY3(Timer1/Prescaler Control Register) is pointed.
TPA             ;"0001"(BIN) of PHY3 is transferred to accumulator.
        :
        :
```

- INITIAL VALUE REGISTER1 / TIMER COUNTER1 { PHY4; (Y'=4, Peripheral register table 0) }

The Initial Value Register1 consisted of a 8-bit register sets the initial value to the counter, or gets the counted value from the counter.

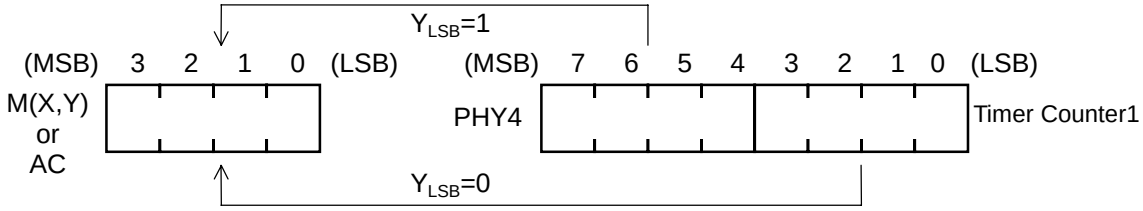
[Writing to the Initial Value Register1]

When a data in RAM or Accumulator is transferred to the Initial Value Register1, the data is loaded into the higher 4-bit(b7 to b4) or lower(b3 to b0) of the Initial Value Register1 in accordance with the condition of LSB of Y-register.



[Reading from the Timer Counter1]

When a current data in the Timer Counter1 is transferred into RAM or Accumulator, the data is gotten from higher 4-bit(b7 to b4) or lower(b3 to b0) of the Timer Counter1 or Timer Counter2 in accordance with the condition of LSB of Y-register.

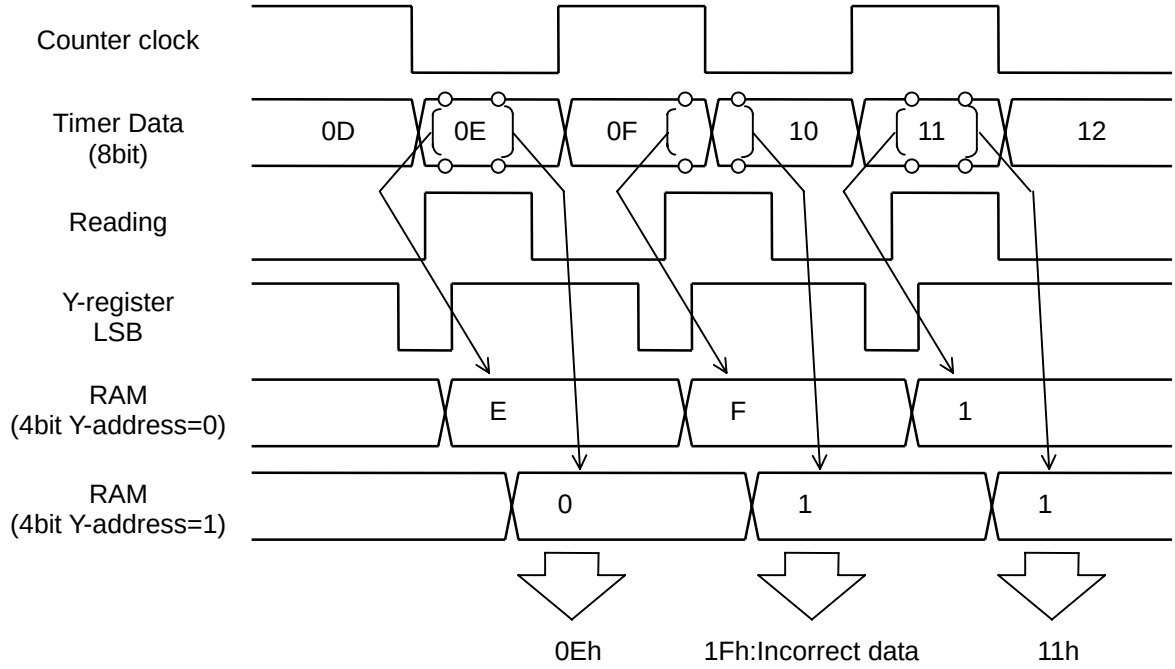


[Reading data from 8-bit Timer Counter1 to RAM]

Though the data of the Timer and Counter can be read in the count operation, the read data is sometimes incorrect when the clock inputs to the counter during the reading operation.

When the 8-bit counter data is read in count operation as shown in the following timing chart (An example of data reading from the counter to RAM), Timer often counts up between the first 4-bit data reading and the second. In case of the following chart, though the timer data is "0Fh" when the lower 4-bit data is gotten, it is "10h" when the higher 4-bit data is gotten. Therefore the final data becomes to be "1Fh".

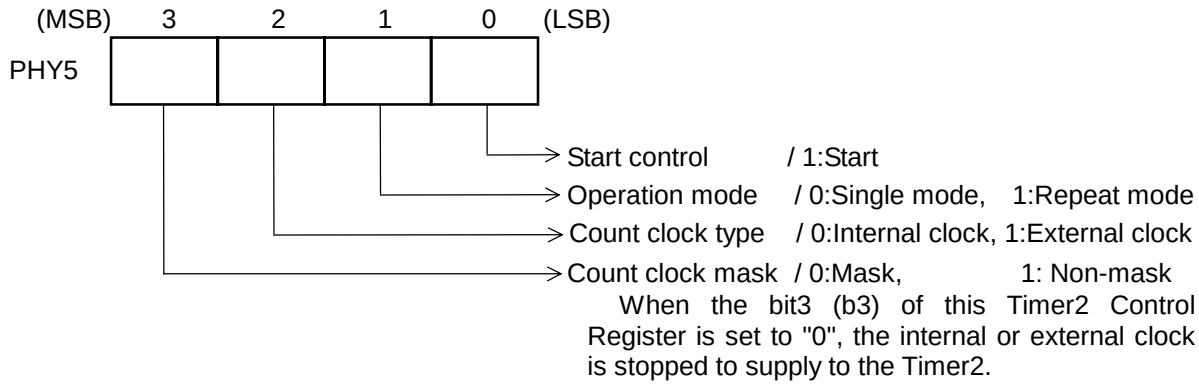
[An example of data reading from Timer Counter1 to RAM]



There are some other cases to read the incorrect data from the 8-bit counter during the count operation depending on the relation with the external clock speed and the system execution speed.

- TIMER2 CONTROL REGISTER { PHY5 ; (Y'=5, Peripheral register table 0) }

[Writing to the Timer2 Control Register]



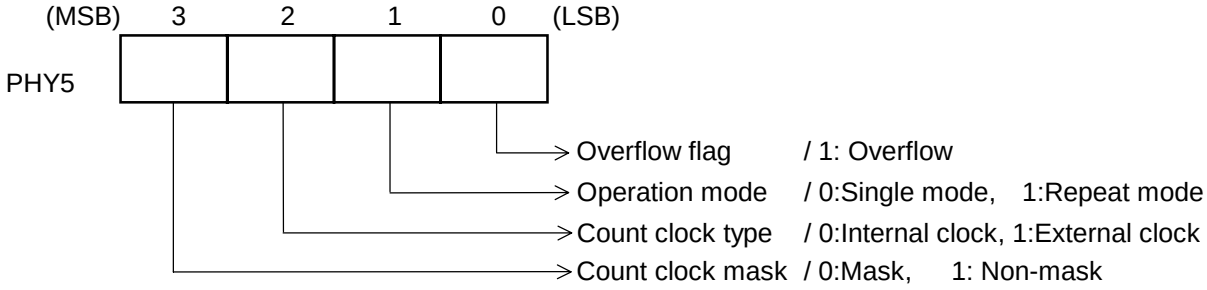
When the bit3 (b3) of this Timer2 Control Register is set to "0", the internal or external clock is stopped to supply to the Timer2.

EX.) An example of the start procedure for the repeat mode, the external clock operation and releasing the count clock mask.

```
        :
        :
SRPC            ;
LDI     Y,5     ;PHY5(Timer2 Control Register) is pointed.
LDI     A,%1110 ;"1110"(BIN) is stored to accumulator          Repeat mode, External
TAP             ;Data is transferred from accumulator to PHY5 clock operation.
LDI     A,%1111 ;"1111"(BIN) is stored to accumulator
TAP             ;Data is transferred from accumulator to PHY5 The count is started.
        :
        :
```

Remarks) In the Timer2 operation, when the count clock mask bit(b3) of the Timer2 Control Register is set to "0", the Timer2 is stopped to count and it holds the latest data of the 12-bit counter2. When the b3 is set to "1", the Timer2 starts to count from the hold data of the 12-bit counter2.

[Reading from the Timer2 Control Register]



EX.)An example of the Timer2 starting information as the Single mode, the internal clock operation and the released clock mask. (The data of Timer2 Control Register is "1001"(BIN).)

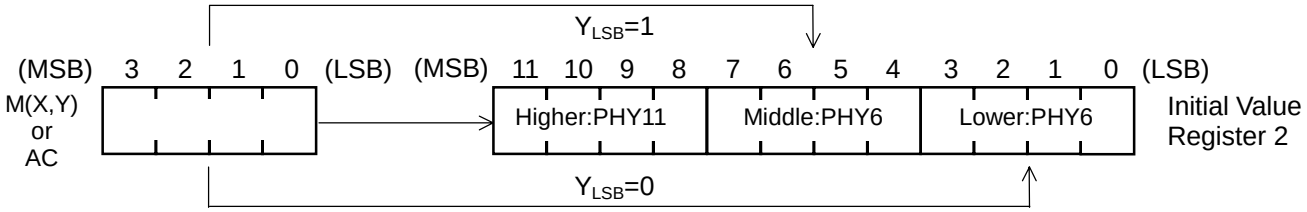
```
        :
        :
SRPC            ;
LDI     Y,5     ;PHY5(Timer2 Control Register) is pointed
TPA             ;Data is transferred "1001"(BIN) of PHY5 to accumulator
        :
        :
```

- INITIAL VALUE REGISTER2 / TIMER COUNTER2 {PHY6, PHY11;(Y'=6,Y'=11 Peripheral register table 0)}

The Initial Value Register2 consisted of a 12-bit register sets the initial value to the counter, or gets the counted value from the counter.

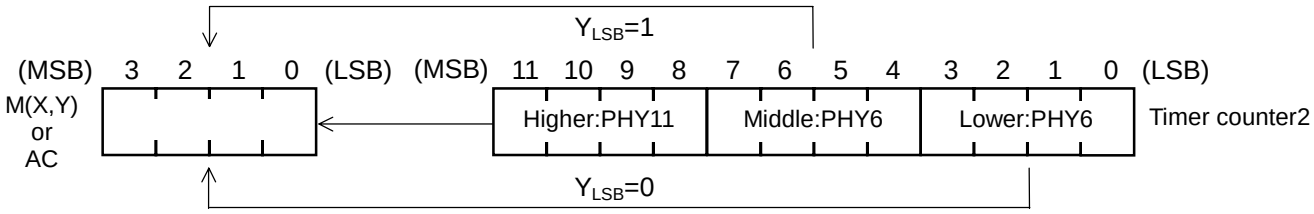
[Writing to the Initial Value Register2]

When a data in RAM or Accumulator is transferred to the Initial Value Register2, the data is loaded into the middle 4-bit(b7 to b4) or lower4-bit(b3 - b0) is accordance with the condition of LSB of Y-register. But the higher 4-bit(b11 to b8) can load the data without any conditions.



[Reading from the Timer Counter 2]

When a current data in the Timer Counter2 is transferred into RAM or Accumulator, the data is gotten from the middle 4-bit(b7 to b4) or lower 4-bit(b3 to b0) of the Timer Counter2 in accordance with the condition of LSB of Y-register. But the higher 4-bit(b11 to b8) can output the data without any conditions.

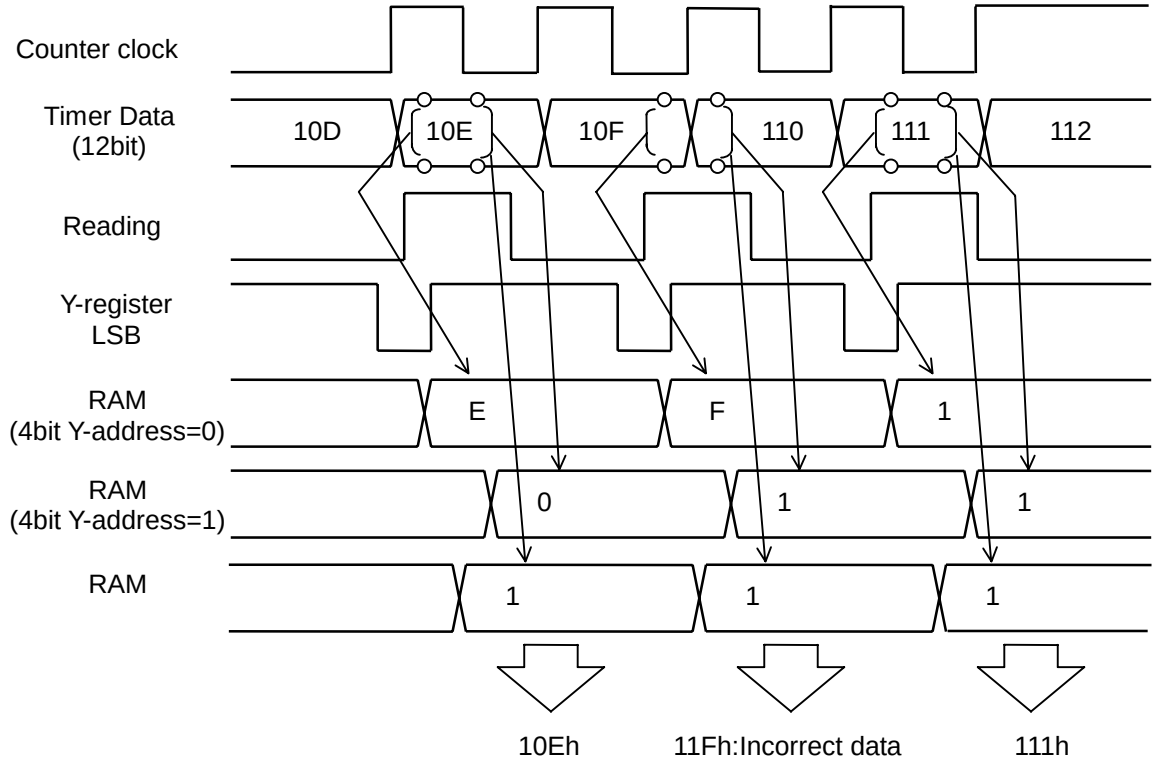


[Reading data from 12-bit Timer Counter2 to RAM]

Though the data of the Timer and Counter can be read in the count operation, the read data is sometimes incorrect when the clock inputs to the counter during the reading operation.

When the 12-bit counter data is read in count operation as shown in the following timing chart(An example of data reading from the counter to RAM), Timer often counts up between the first 4-bit data reading and the second. In case of the following chart, though the timer data is "110h" when the lower 4-bit data is gotten, it is "10Fh" when the higher 4-bit data is gotten. Therefore the final data becomes to be "11Fh".

[An example of data reading from 12-bit Timer Counter2 to RAM]

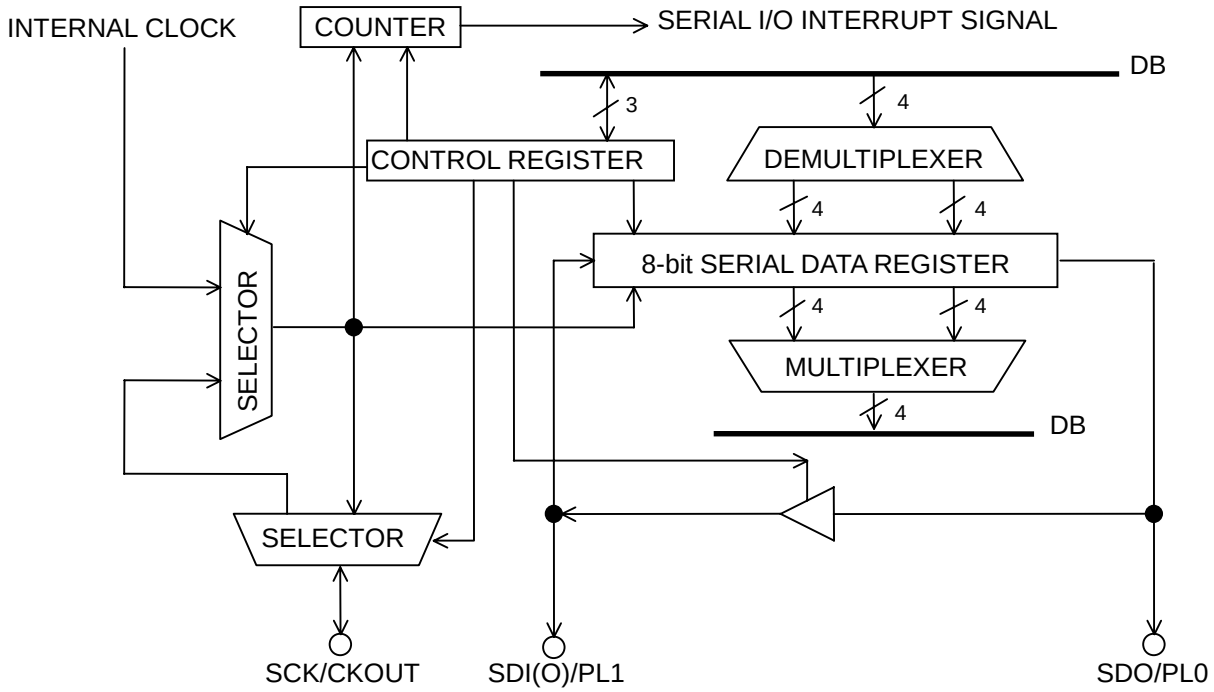


There are some other cases to read the incorrect data from the 12-bit counter during the count operation depending on the relation with the external clock speed and the system execution speed.

■ SERIAL INPUT OUTPUT

SERIAL INPUT OUTPUT consists of the sift registers to convert from 8-bit parallel data to serial data, the 3-bit serial clock counter, and the 3-bit serial control register. It operates as the 8-bit serial input or output. The external or internal clock is selected as the shift clock in accordance with the Serial Input / Output control register.

[Block diagram of the Serial Input Output]



The serial input or output operation starts when the LSB of the Serial Input / Output control register(PHY1) is set to "1". In the external clock operation, the serial input or output operation waits to start until the external clock come in.

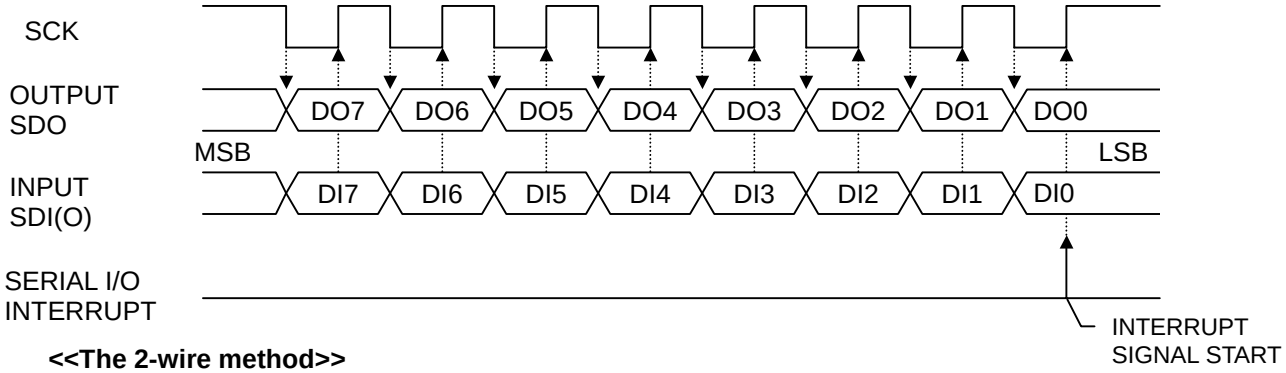
When the serial shift register (PHY2) is set the data in advance, the data is output(transmitted) through the SDO or the SDI(O) terminal. The SDI(O) terminal can be changed as a transmitter or a receiver in accordance with the bit3(b3) of PHY1. The data order, MSB or LSB first, is selected by the mask option.

Serial Input Output operates as the 3-wire method using SDI(O), SCK and SDO terminals, or the 2-wire using SDI(O) and SCK terminal.

<<The 3-wire method>>

The data synchronized with the falling edge of the SCK clock is output(transmitted) through the SDO terminal. The data synchronized with the rising edge of the SCK clock is input(received) through the SDI(O) terminals.

[The 3-wire transmission timing chart (MSB first)]

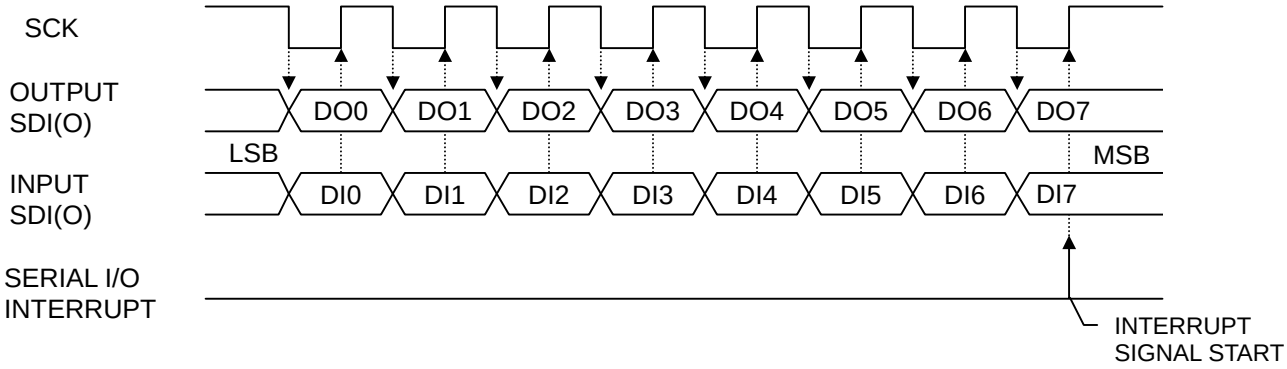


<<The 2-wire method>>

The data synchronized with the falling edge of the SCK clock is transmitted through the SDI(O) terminal. The data synchronized with the rising edge of the SCK clock is received through the SDI(O) terminal.

* In case of the data transmission through the SDI(O) terminal, the SDI(O) terminal must be set as the output by the condition of the bit3(b3) of the Serial Input / Output control register(PHY1) set to "1". In case of the data reception through the SDI(O) terminal, the SDI(O) terminal must be set as the input by the condition of the b3 of PHY1 set to "0".

[The 2-wire transmission timing chart (LSB first)]



In case of the external clock operation, the external clock is input as the SCK clock to the SCK terminal as shown in the serial transmission-timing chart. The signal condition into the SCK terminal must be kept as “HIGH” until the external clock come in. In the transmission, when the SCK with the noise or other redundant signals from the outside of the **NJU3505** input to the SCK terminal, Serial Input Output operates incorrectly. The maximum frequency of the SCK is 500kHz.

In case of the internal clock operation, the SCK outputs through the SCK terminal as shown in the serial transmission-timing chart. The internal interrupt signal occurs when the 3-bit counter has counted the SCK clock up to 8 times that means 1-byte serial data transmission end. The internal clock as the SCK is the divided clock in the internal prescaler, and the frequency of the clock can be selected by the mask option from follows which are dividing numbers based on the inverse of the 1-instruction executing period($1/f_{OSC}$ x 6).

1/2, 1/4, 1/8, 1/16, 1/32,1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048,1/4096

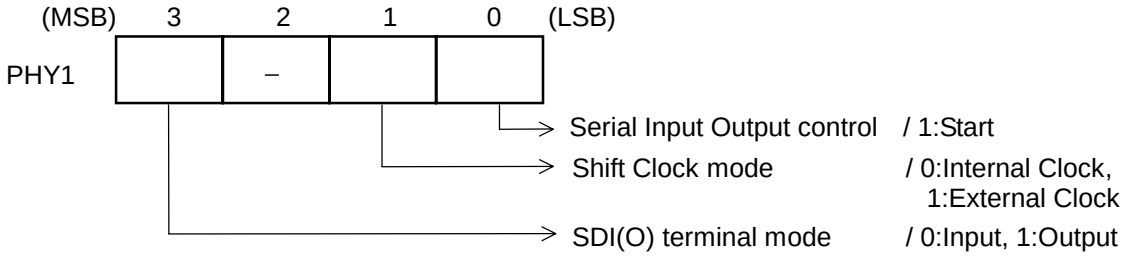
Remarks 1) When the bit2(b2) of Timer1 / Prescaler control register(PHY3) is set to "1", the prescaler generating the internal serial clock is stopped and the internal serial clock is also stopped. Accordingly, Serial Input Output does not operate.

Remarks 2) If the writing operation is operated to the Serial Input / Output shift register(PHY2) or the Serial Input / Output control register during the transmission or the reception operation, the 3-bit counter is reset and the serial data transmission or reception is stopped. Therefore the writing operation to the above registers must not be operated during the transmission or reception operation.

- SERIAL INPUT/OUTPUT CONTROL REGISTER { PHY1 ; (Y'=1) }

When the data of bit1(b1) and bit3(b3) of the Serial Input / Output control register are changed, the operation must be performed before starting the serial transmission. (See the following sample program) In changing the condition of b1 or b2 of PHY1 and setting the LSB of PHY1 to start the transmission are operated in the mean time, Serial Input Output operation does not operate correctly.

[Writing to the Serial Input / Output Control Register]

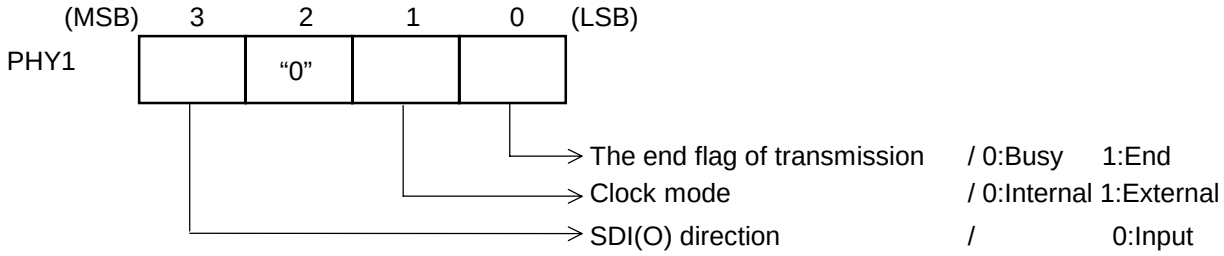


EX.)An example of the start procedure in the 3-wire serial data transmission, the external clock operation and the SDI(O) terminal setting as the input .

```
        :
        :
SRPC                ;
LDI     Y,1         ;PHY1(Serial Input / Output control register) is pointed
LDI     A,%0010     ;"0010"(BIN) is stored to accumulator      External clock,
TAP                 ;Data is transferred from accumulator to PHY1  ) Input mode
LDI     A,%0011     ;"0011"(BIN) is stored to accumulator          ) Transmission
TAP                 ;Data is transferred from accumulator to PHY1  ) Starts.
        :                                                          )
        :
```

Remarks 3) In case of the external clock operation at the both of the transmission and reception mode, inputting the external clock must wait while the 2-instruction execution period after that LSB of Serial Input / Output control register is set to "1"(START). (one instruction execution period = 1 / f_{OSC} X 6)
If the external clock is input within the 2-instruction execution period, the Serial Input / Output shift register can not recognize the first SCK. The number of the shift operation is decreased a time, 8 times to 7.

[Reading from the Serial Input / Output Control Register]



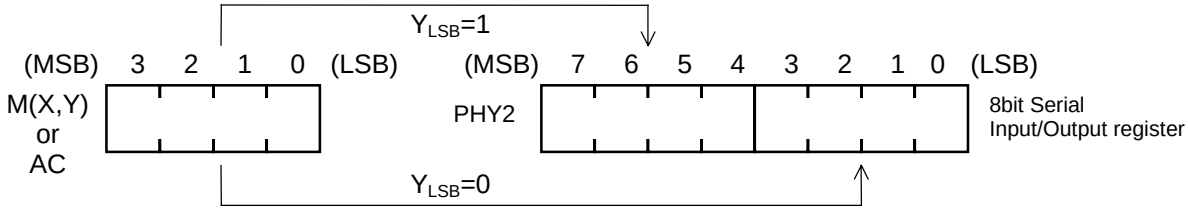
Remarks 4) The end flag of transmission is set to "1" when the serial data(8 bits) transmission operation is ended. It is cleared by setting the serial data transmission start signal in the Serial Input /Output control register.

- SERIAL INPUT/OUTPUT SHIFT REGISTER { PHY2 ; (Y'=2) }

The Serial Input / Output Shift register consisted of a 8-bit register operates to set the transmission data or to get the reception data.

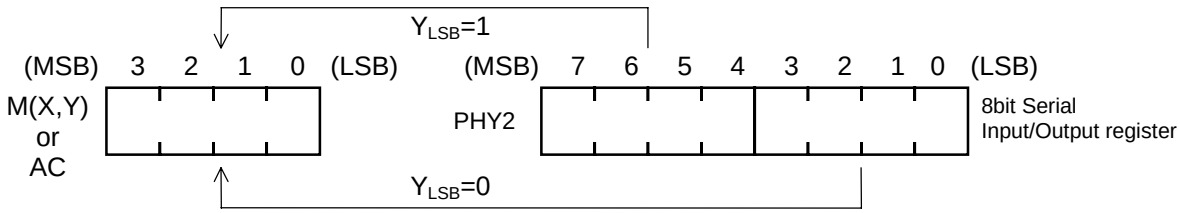
[Writing to the Serial Input / Output Shift Register]

The data in RAM or Accumulator is transferred to the Serial Input / Output Shift register, and it is loaded into lower 4-bit(b0 – b3) or higher(b4 – b7) in PHY2 in accordance with the condition of LSB of Y-register.



[Reading from the Serial Input / Output Shift Register]

The Serial Input data is transferred to RAM or Accumulator, it is loaded from lower 4-bit(b0 – b3) or higher(b4 – b7) of PHY2 in accordance with the condition of LSB of Y-register.



An example of the serial data reception program)

In the internal clock operation, SDI(O) terminal is set as the input and the serial input data is transferred to RAM.

```
          :
          :
;---- Interrupt process ----
          ORG   $40                ;Interrupt vector address of FULL or EMPTY
SINT      SRPC                     ;
          LDI   Y,1                ;The Serial Input / Output control register is set
          TPA                      ;
          TBA   0                  ;The end flag of transmission is tested
          JMP   SIO_OK             ;
          JMP   SINT_E             ;
;
SIO_OK    LDI   Y,2                ;The Serial Input / Output shift register is set
          RRPC                     ;RAM to store the serial input data is pointed
          LDI   X,SIO_DAT.X        ;RAM address, X=0
          LDI   Y,SIO_DAT.Y        ;RAM address, Y=0
          TPMICY                   ;The serial input data is transferred to RAM(lower
                                   ;      4-bit) and Y-register is incremented
          TPMICY                   ;The serial input data is transferred to RAM(higher
                                   ;      4-bit) and Y-register is incremented
;
SINT_E    RETI                     ; End of the interrupt process
;
;------ Serial data inputting process ------
SIO_IN    SRPC                     ;
          LDI   Y,0                ;The peripheral register table is set
          CLA                      ;
          TAP                      ;
          LDI   Y,1                ;The Serial Input / Output control register is set
          LDI   A,%0000            ;The internal clock operation is set and the SDI(O)
                                   ;      terminal is set as the input
          TAP                      ;
          LDI   A,%0001            ;The serial data reception is started
          TAP                      ;
;
          :
          :
          WSEG                     ;The RAM area is set
SIO_DAT   DS    2                  ;The area to store the serial input data is secured
```

An example of the serial data transmitting program)

In the internal clock operation, the SDI(O) terminal is set as the output and the data in RAM is transmitted.

```
                :
                :
;---- Interrupt process ----
                ORG     $40                 ;Interrupt vector address of FULL or EMPTY
SINT            SRPC                        ;
                LDI     Y,1                 ;The Serial Input / Output control register is set
                TPA                         ;
                TBA     0                   ;The end flag of transmission is tested
                JMP     SIO_OK              ;
                JMP     SINT_E              ;
;
SIO_OK          RRPC                        ;The end flag of transmission is set
                LDI     X,SIO_FLG.X         ;
                LDI     Y,SIO_FLG.Y         ;
                LDI     A,1                 ;
                TAM                         ;
;
SINT_E          RETI                        ;End of the interrupt process
;
;------ Serial data transmitting process ------
SIO_OUT         SRPC                        ;
                LDI     Y,0                 ;The peripheral register table is set
                CLA                         ;
                TAP                         ;
;
                LDI     Y,2                 ;The Serial Input / Output shift register is set
;
                RRPC                        ;RAM to store the serial output data is set
                LDI     X,SIO_DAT.X         ;RAM address, X=0
                LDI     Y,SIO_DAT.Y         ;RAM address, Y=1
                TMPICY                      ;The data in RAM is transferred to the Serial Input /
                                            ;       Output shift register(lower 4-bit)
                                            ;       and Y-register is incremented
                TMPICY                      ;The data in RAM is transferred to the Serial Input /
                                            ;       Output shift register(higher 4-bit)
                                            ;       & Increments Y
;
                SRPC                        ;
                LDI     Y,1                 ;The Serial Input / Output control register is set
                LDI     A,%1000             ;The internal clock operation and the transmission
                                            ;       mode are set
                TAP                         ;
                LDI     A,%1001             ;The serial data transmitting operation is started
                TAP                         ;
;
                :
                :
                WSEG                        ;The RAM area
SIO_DAT         DS      2                   ;The area to store the serial output data
SIO_FLG         DS      1                   ;The end flag of transmission
```

■ INTERRUPT

The **NJU3505** prepares four kinds of the interrupt. The interrupt "enable" or "disable" is controlled by the program. The interrupt operates as single process and no multiple. However, when new interrupt request occurs during the other interrupt process, the request is kept, and then the new interrupt process starts after the prior interrupt process. The priority order of the interrupt is that the first is (1)External interrupt-1, the second is (2)Internal interrupt-1, the third is (3)Internal interrupt-2, and the fourth is (4)Internal interrupt-3 as shown below.

When the interrupt request flag is set by the own factor, the interrupt enabled by the interrupt control register (PHY9) stores the data of Program Counter, Accumulator, X-reg, X'-reg, Y-reg, Y'-reg, RPC, and STATUS into the STACK register, and sets the interrupt vector address into Program Counter, and then the interrupt process is started. The return from the interrupt process by "RETI" instruction resets the corresponded interrupt request flag, and regain the held data from STACK, and then the operation before the interrupt process is started continuously. When the interrupt control register disables the interrupt process, the interrupt request flag is not set.

[THE PRIORITY ORDER OF FOUR INTERRUPTS]

Order	Interrupt	Vector Address(H:HEX)
(1)	External interrupt-1	10H
(2)	Internal interrupt-1 Timer/Counter-1 Overflow	20H
(3)	Internal interrupt-2 Timer/Counter-2 Overflow	30H
(4)	Internal interrupt-3 Serial shift register Full/Empty	40H

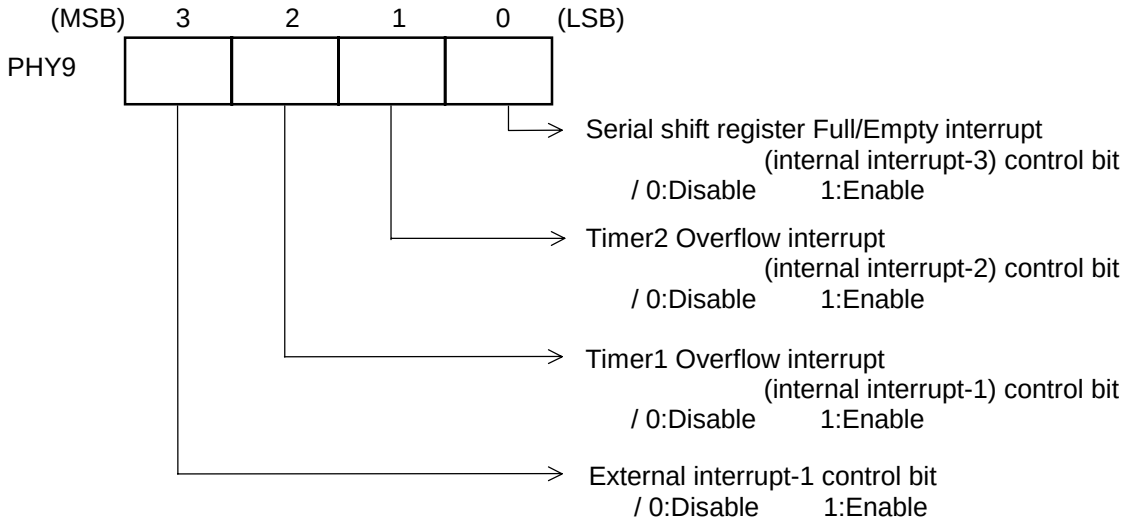
The External interrupt-1 enabled by PHY9 is started the interrupt process when the rising edge of signal pulse is input to the external interrupt signal input terminal(EXTI). The External interrupt-1 request flag is reset by 'RETI' instruction. When the external interrupt-1 occurs during the standby mode by the HALT instruction, the External interrupt-1 request signal is latched and its interrupt process is started after that the standby mode is released.

The Internal interrupt enabled by PHY9 is started the interrupt process when the internal interrupt request flag is set.

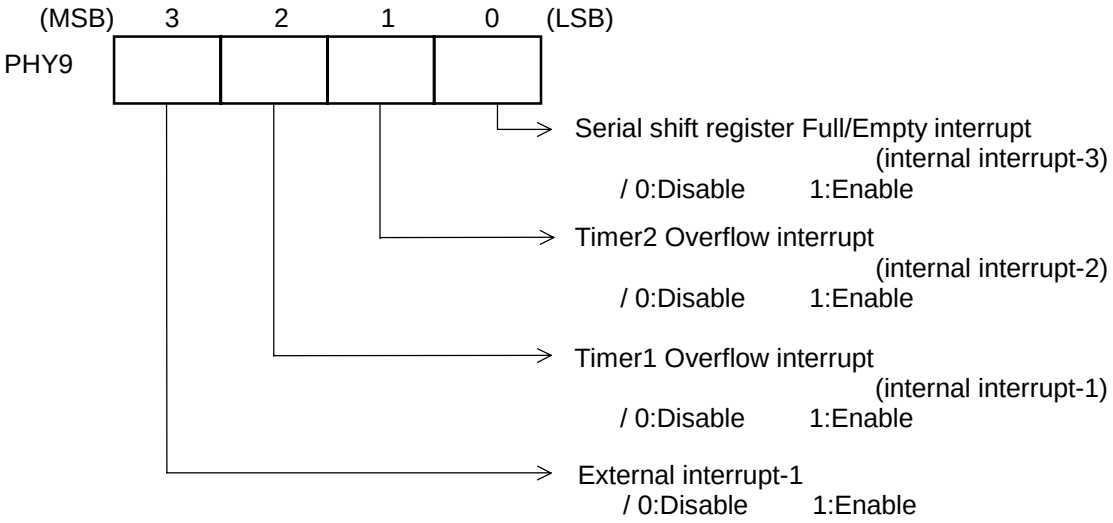
The Timer1 and the Timer2 interrupt request flags are independent of the overflow flag, and they are reset by "RETI" instruction, (TIMER)START signal of the Timer control register, or RESET signal from the external circuit. Serial Input Output interrupt request flag is set synchronizing with the transmission end flag when its interrupt is enabled by PHY9. And the flag is reset by the "RETI" instruction or the RESET signal from the external circuit.

- INTERRUPT CONTROL REGISTER { PHY9 ; (Y'=9) }

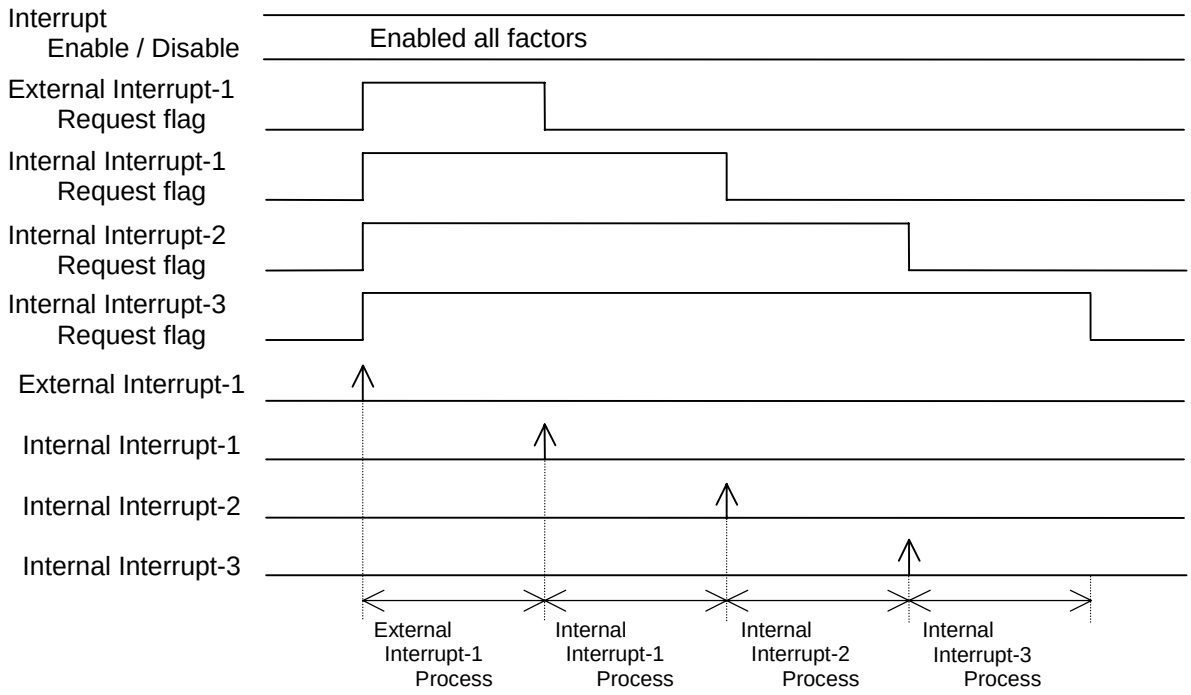
[Writing to the Interrupt Control Register]



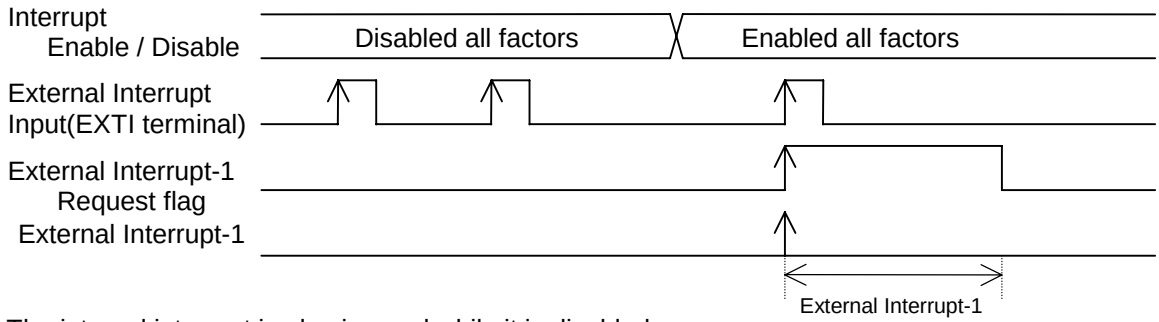
[Reading from the Interrupt Control Register]



[Enabled all factors (b0 to b3 of PHY9 were set to "1")]

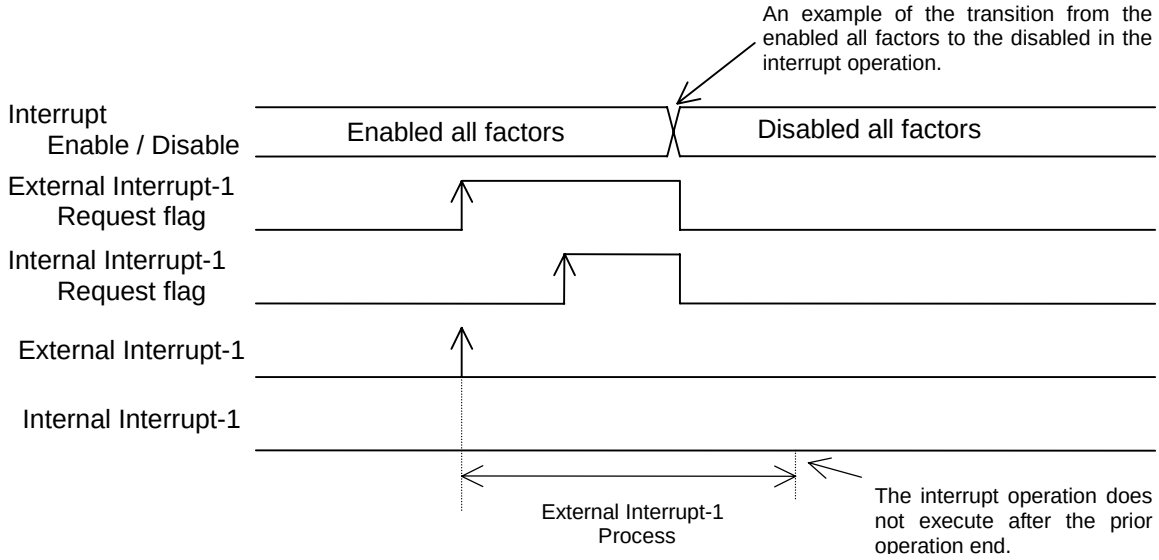


[From the all factors disabled to the enabled (b0 to b3 of PHY9 are changed from "0" to "1")]



* The internal interrupt is also ignored while it is disabled.

[From the all factors enabled to the disabled (b0 to b3 of PHY9 are changed from "1" to "0")]



* When the interrupt is enabled, the latest interrupt request occurred during the prior other interrupt process starts its interrupt process after the prior interrupt operation. However, when the interrupt is disabled during the prior interrupt process as shown in above timing chart, the latest interrupt request does not start. But the prior interrupt process is completed.

■ A/D CONVERTER

The A/D converter operates with the following specification.

- A/D Conversion : Successive Approximation method
- Minimum conversion Time : 40µsec (V_{DD}=5V, V_{REF}=5V, f_{ADCK}=225kHz)
- Resolution : 8 bit (256 step)
- Absolute Accuracy : ±2 LSB (V_{DD}=5V, V_{REF}=5V)
- Reference Voltage : 2.4V–AV_{DD}
- Analog Input Voltage : AV_{SS}–V_{REF}
- Channel : Multiplexed 8-channel Input

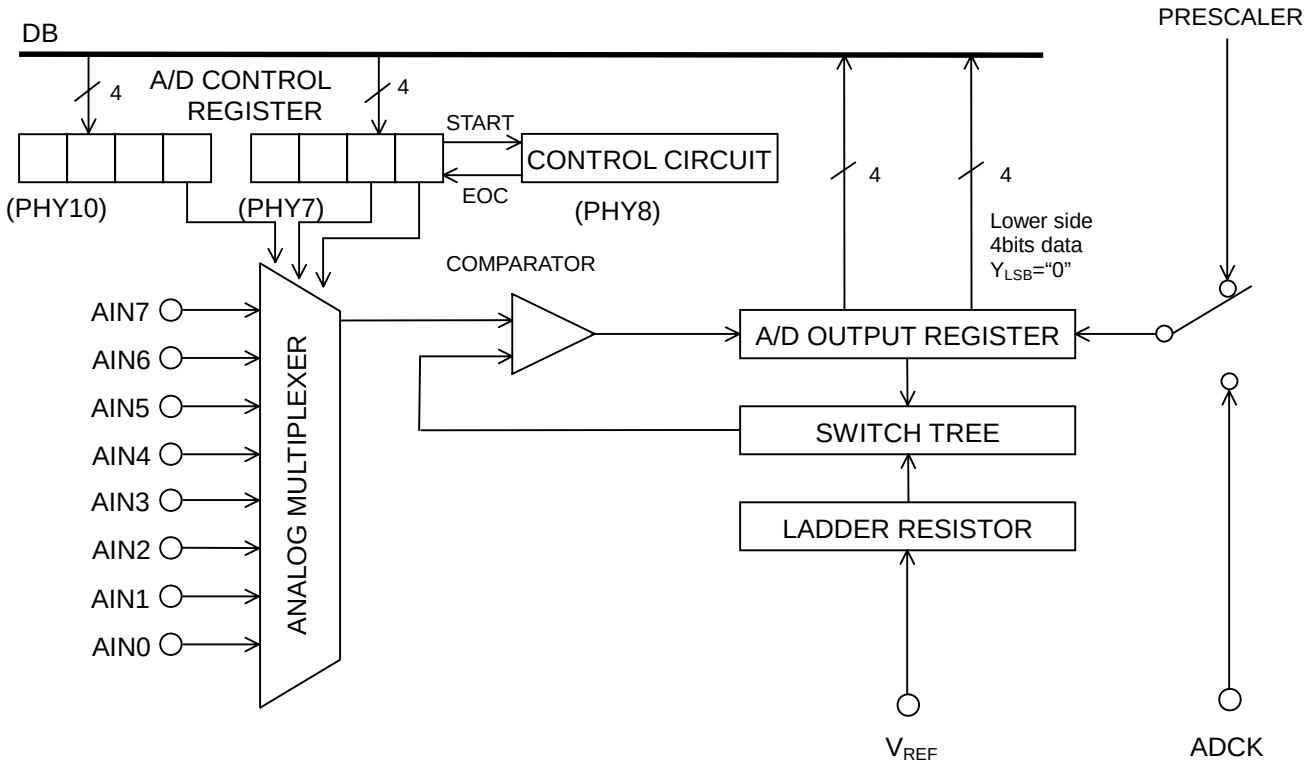
The A/D converter block diagram and the timing chart are shown below.

The lower 2 bits of the A/D converter control register(PHY7) or the lower 1 bit of the A/D control converter (PHY10) are the switches to select an analog input channel from four multiplexed inputs(AIN0 – AIN7). The analog input signal to the analog input port selected by the A/D converter control register is converted to the digital data, and then the digital data is stored into the A/D converter output register(PHY8).

The A/D control clock can selected either the external clock or the internal by the mask option. In the external clock operation, the input clock from the "ADCK" terminal operates as the A/D control clock. In the internal clock operation, the clock divided in the internal Prescaler operates as the A/D control clock. The frequency of the clock from the internal Prescaler can be selected by the mask option from the following which are dividing numbers based on the inverse of one instruction execution time($1/f_{OSC}$ X 6).

1/2, 1/4, 1/8, 1/16, 1/32,1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048,1/4096

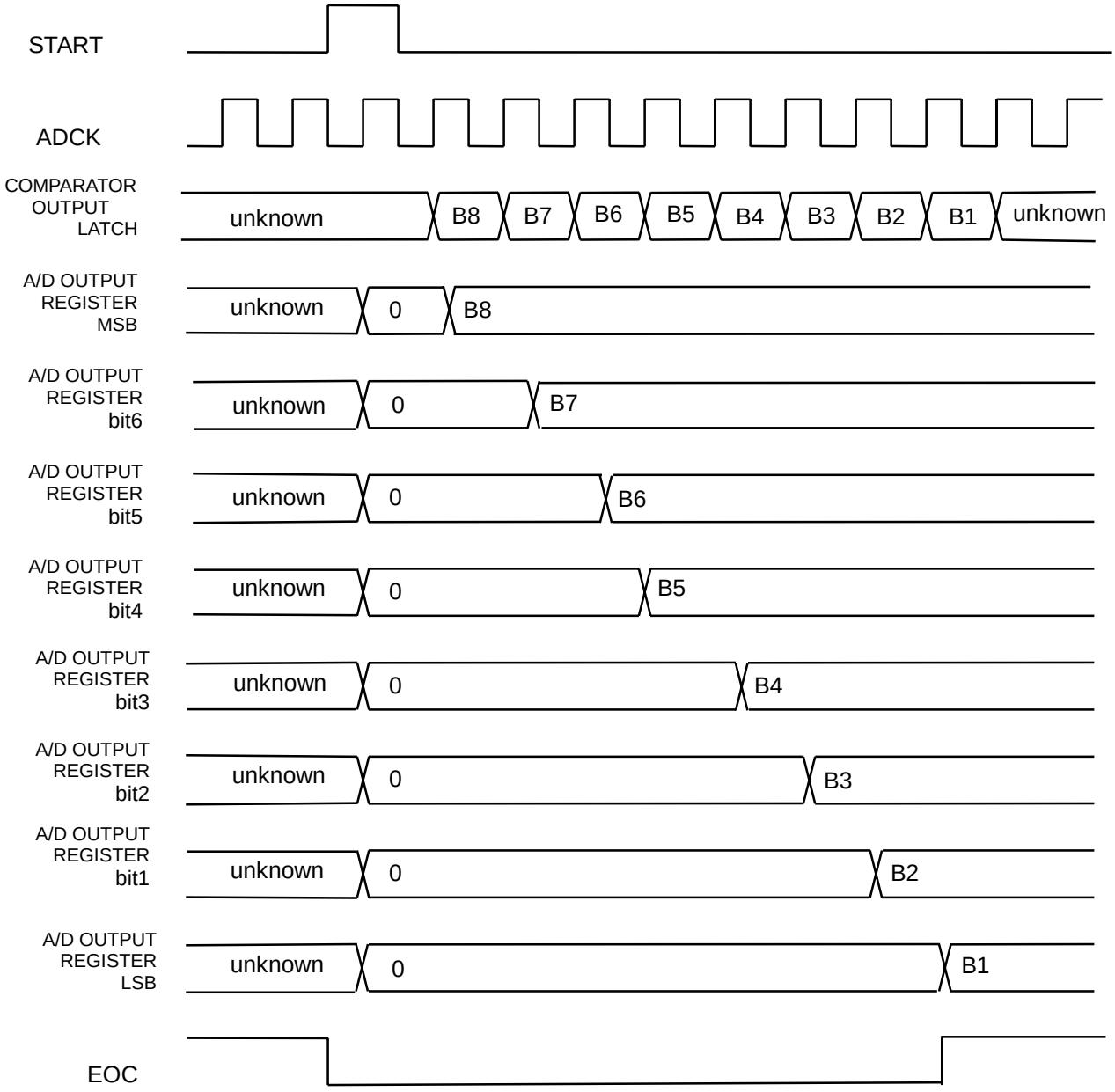
[A/D CONVERTER BLOCK DIAGRAM]



Remarks) The A/D control clock can be selected either the external clock from the ADCK terminal or the internal clock from the Prescaler by the mask option. The Prescaler supplies clocks to Timer/Counter, Serial Input Output, and A/D converter.

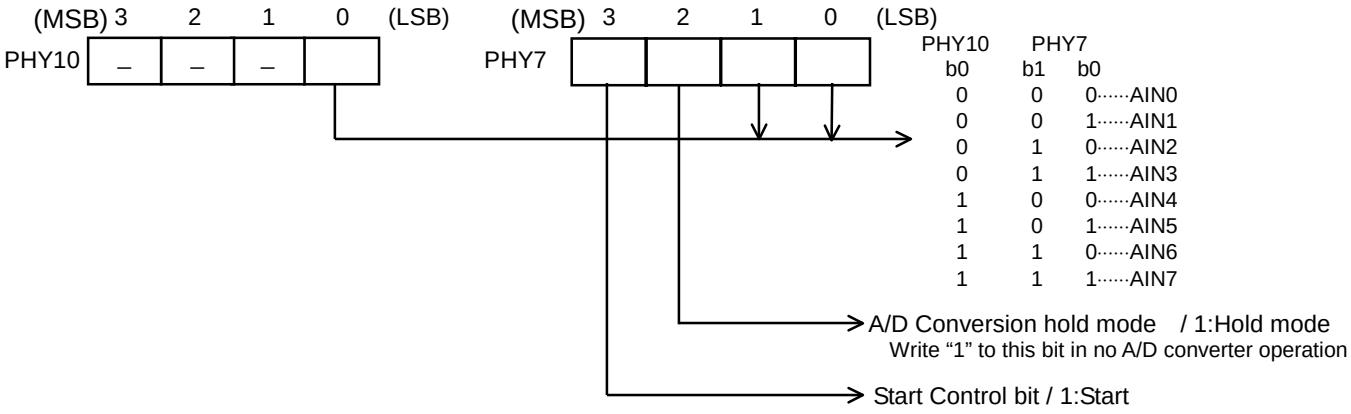
The maximum frequency of the A/D control clock is 225kHz in the both of the internal and the external clock operation.

[A/D CONVERTER OPERATION TIMING CHART]



- A/D CONTROL REGISTER { PHY7; (Y'=7), PHY10; (Y'=10) }

[Writing to the A/D Control Register { PHY7; (Y'=7), PHY10; (Y'=10) }]

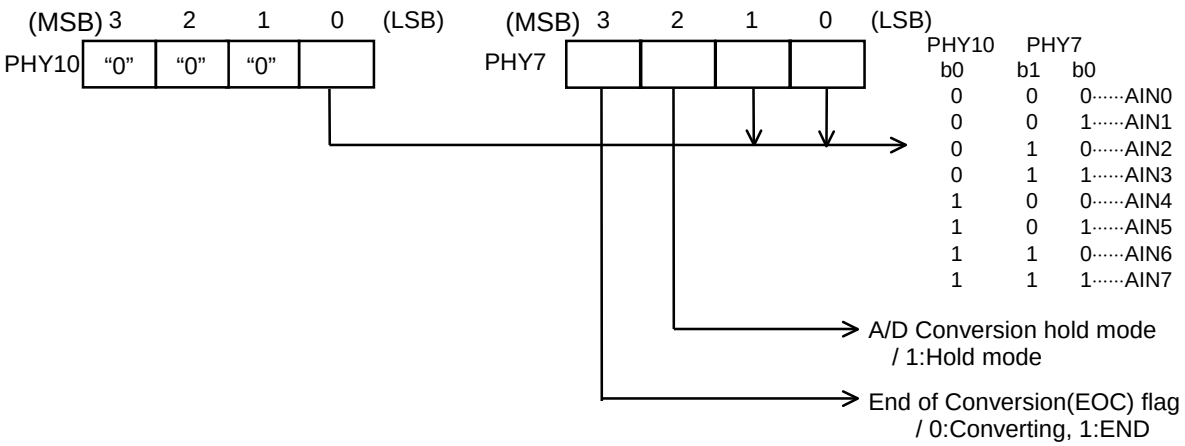


EX.) An example of A/D converter start procedure for selecting AIN1 as the input and releasing the A/D hold mode.

```
        :
        :
SRPC                ;
LDI     Y,10        ; PHY10(A/D control register) is pointed
LDI     A,%0000     ; "0000"(BIN) is stored to AC
TAP                 ;Data transferred from AC to PHY10      AIN1 as the input,
LDI     Y,7         ;PHY7(A/D control register) is pointed  Releasing Hold mode
LDI     A,%0001     ;"0001"(BIN) is stored to AC
TAP                 ;Data transferred from AC to PHY7
LDI     A,%1001     ;"1001"(BIN) is stored to AC            Start of conversion
TAP                 ;Data transferred from AC to PHY7
        :
        :
```

Remarks) In the external clock operation, the external clock must be input to the ADCK terminal before the start of A/D conversion.

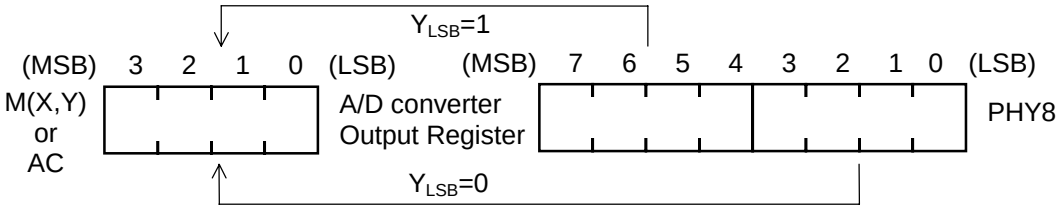
[Reading from the A/D Control Register]



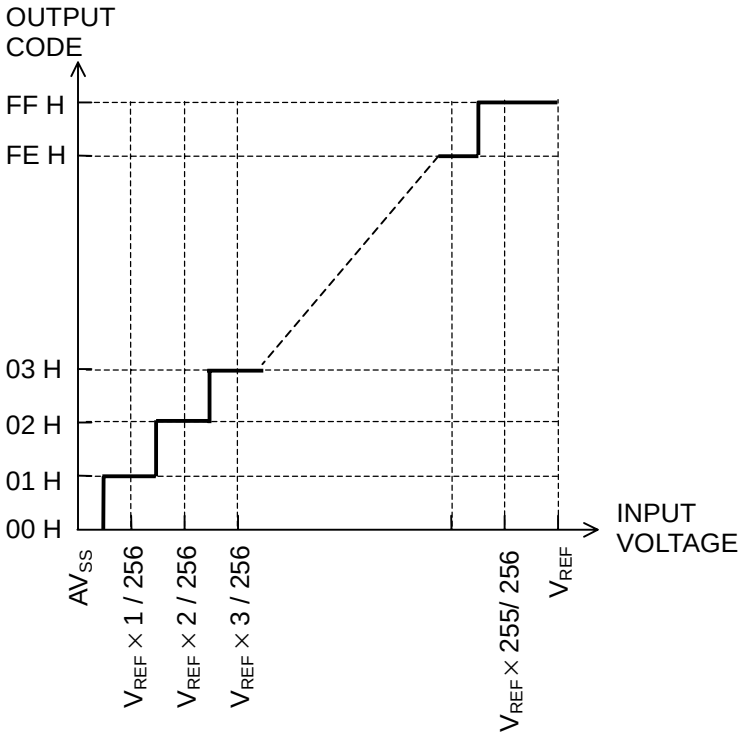
- A/D OUTPUT REGISTER { PHY8; (Y'=8) }

  The 8-bit data converted by the A/D converter can be transferred to RAM or Accumulator. Either the higher 4-bit data or the lower is gotten in accordance with the condition of LSB of Y-register.

[Reading from the A/D Output Register]



[Analog input voltage vs Output digital data]



An example of A/D conversion operation)

AIN2 terminal is selected and the result of the A/D conversion is transferred to RAM.

```
                :
                :
ADC_EXE     SRPC                    ;
            LDI     Y,0             ;Peripheral register table 0
            CLA                     ;
            TAP                     ;
;
            LDI     Y,10            ;
            LDI     A,%0000         ;
            TAP                     ;A/D control register
            LDI     Y,7             ;AIN2 as the input
            LDI     A,%0010         ;
            TAP                     ;
            LDI     A,%1010         ;Start of A/D conversion
            TAP                     ; & AIN2 terminal
;
LP_ADC      TPA                     ;End of conversion ?
            TBA     3               ;
            JMP     ADC_END         ;
            JMP     LP_ADC          ;
;
ADC_END     LDI     Y,8             ;A/D conversion register
;
            RRPC                    ;RAM to store the result of A/D conversion
            LDI     X,ADC_DAT.X     ;RAM address X=0
            LDI     Y,ADC_DAT.Y     ;RAM address Y=0
            TPMICY                  ;The A/D converted data to RAM
                                    ;     lower 4-bit at YLSB=0
            TPMICY                  ;The A/D converted data to RAM
                                    ;     higher 4-bit at YLSB=1
                :
                :
            WSEG                    ;RAM area
ADC_DAT     DS      2               ;Are for the result of A/D conversion
```

■ STANDBY FUNCTION

STANDBY FUNCTION halts the IC operation and reduces the current consumption.

The STANDBY function starts by the HLT instruction. After the HLT instruction execution cycle, the internal oscillator operation is stopped and all of the operation is halted. In case of the external clock operation, the clock is stopped automatically delivering into the internal system by the internal circuit, and all of the operation is halted as same as the internal oscillator operation. This is STANDBY mode.

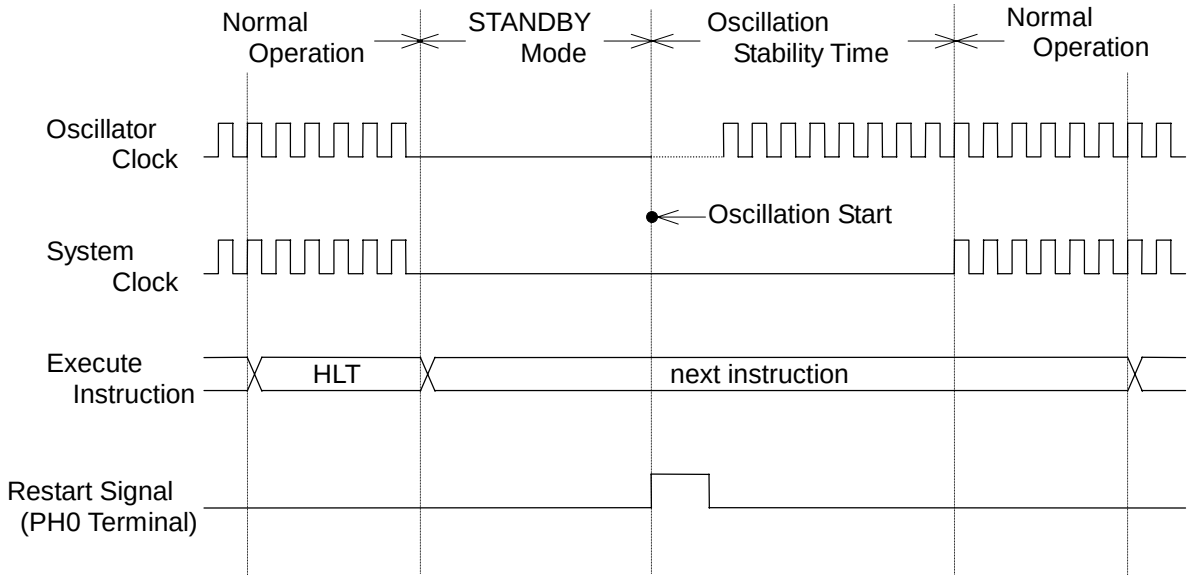
In the STANDBY mode, the operating current can be reduced. Though the clock into the internal system is stopped and all of the operation is halted, all conditions of Program Counter, Registers, and data in RAM are kept certainly.

Two ways to release from the STANDBY mode are prepared. One way is the reset operation that when the reset signal is input to RESET terminal, the operation starts from the initial condition. The other way is the restart operation that when the restart signal is input to PH0 terminal, the operation starts from the kept Program Counter location which is the program address after the final operation. In case of the restart signal operation, if the rising signal, low to high, is input to PH0 terminal, the internal oscillator circuit starts at first. After the stabilized clock from the internal oscillator was counted eight times, the clock is started delivering into the internal system. Then the **NJU3505** starts to operate from the kept Program Counter location with all of the kept conditions.(See *1)

In case of the external clock operation, the external clock must be started to supply to the OSC1 terminal before the STANDBY mode is released. The external clock is recommended to stop supplying to the OSC1 terminal for reducing the power consumption during the STANDBY mode.

*1: When the restart signal is input to PH0 terminal to release the STANDBY mode, PORTH must be selected as the input by the mask option.

[STANDBY MODE TIMING CHART]



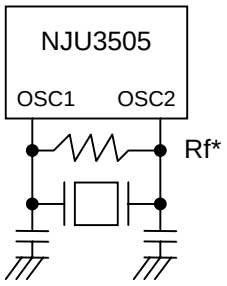
■ CLOCK GENERATION

The system clock is generated in the internal oscillator circuit with the external crystal or ceramic resonator, or the resistor connected to OSC1 and OSC2 terminals. Furthermore, the **NJU3505** can operate by the external clock to the OSC1 terminal for the system clock. In the external clock operation, the OSC2 terminal must be opened.

The typical application examples for each oscillator circuit are shown below. However a Crystal or a Ceramic operation requires the considered evaluation, because the oscillator operates in accordance with the characteristics of each component.

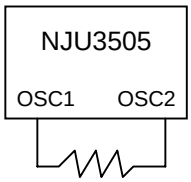
[OSCILLATOR APPLICATION EXAMPLES]

1) X'tal/Ceramic oscillation

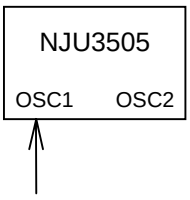


The resistor Rf* is sometimes required to connect when the Crystal operation.

2) CR oscillation



3) External clock input

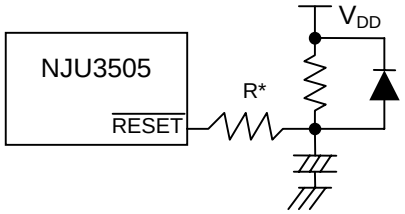


■ RESET OPERATION

All of the internal circuits are initialized by inputting the low level signal to the RESET terminal.

A circuit example for Power On Reset Operation with a resistor, a capacitor, and a diode is shown below. Power On Reset Operation requires to keep the low level of the input signal to RESET terminal until the stabilized oscillation of the internal oscillator. Therefore the constants on the reset circuit must be decided in accordance with the characteristics of the clock generator circuit.

[An example of Power On Reset circuit]



R*:A resistor is RESET terminal protector. It is required depending on the condition of an application.

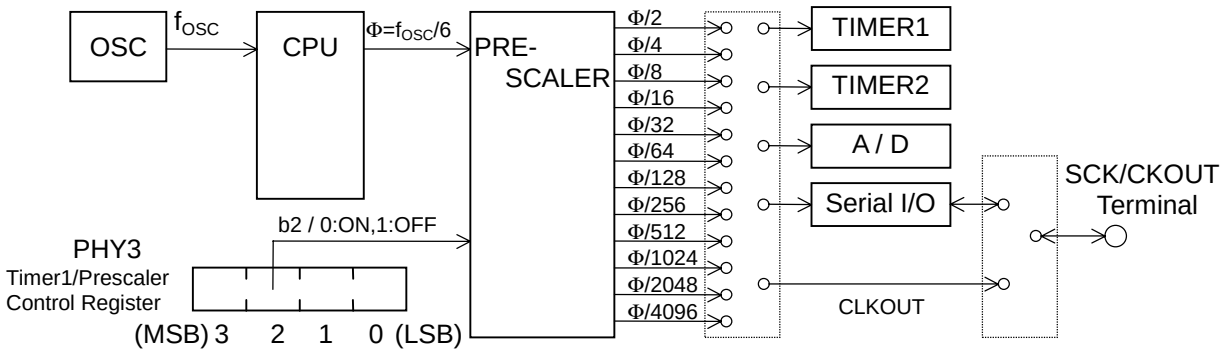
■ PRESCALER

The **NJU3505** prepares a built-in Prescaler consisted of 12-bit binary counter which counts the machine cycle period clock($1/f_{OSC}$ x 6) from 2 to 4096 times. The Prescaler can supply the clock to Timer1 and 2, Serial Input Output, A/D converter, and the external application through the “SCK/CKOUT” terminal. A frequency of the clock can be selected from 12 kinds shown in follows.

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

When the bit2(b2) of Timer1/Prescaler control register(PHY3) is set to "1", the Prescaler operation is stopped, but the output clock is also stopped to Timer1 and 2, Serial Input Output, A/D converter and the external application through the "SCK/CKOUT" terminal. When the b2 of PHY3 is set to "0", the Prescaler operation is started to count from "0".

[AROUND THE PRESCALER BLOCK DIAGRAM]



EX.)The output frequency of Prescaler at f_{OSC} = 4MHz (Φ=4MHz/6)

Prescaler Divider		Output Frequency
Φ/2	.....	333.33kHz
Φ/4	.....	166.67kHz
Φ/8	.....	83.33kHz
Φ/16	.....	41.67kHz
Φ/32	.....	20.83kHz
Φ/64	.....	10.42kHz
Φ/128	.....	5.21kHz
Φ/256	.....	2.60kHz
Φ/512	.....	1.30kHz
Φ/1024	.....	651kHz
Φ/2048	.....	326kHz
Φ/4096	.....	163kHz

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 – +7.0	V
Input Voltage	V_{IN}	-0.3 – V_{DD}+0.3	V
Output Voltage	V_{OUT}	-0.3 – V_{DD}+0.3	V
Analog Supply Voltage	AV_{DD}	-0.3 – V_{DD}+0.3	V
Analog Reference Voltage	V_{REF}	-0.3 – AV_{DD}+0.3	V
Analog Input Voltage	AIN0–AIN7	-0.3 – AV_{DD}+0.3	V
Operating Temperature	T_{opr}	-20 – +75	°C
Storage Temperature	T_{stg}	-55 – +125	°C

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS 1-1 (V_{DD}=3.6–5.5V, V_{SS}=0V, Ta= -20–75°C)

PARAMETER	SYMBOL	C O N D I T I O N S	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	3.6		5.5	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=5V,f_{OSC}=2MHz X'tal Oscillation In Reset		0.8	1.2	mA	*3
	I_{DD2}	V_{DD} V_{DD}=5V,f_{OSC}=2MHz Ceramic Oscillation In Reset		0.8	1.2	mA	*3
	I_{DD3}	V_{DD} V_{DD}=5V,f_{OSC}=2MHz CR Oscillation In Reset		1.1	1.6	mA	*3
	I_{DD4}	V_{DD} V_{DD}=5V,f_{OSC}=4MHz Operating (Except ADC)		2.6	4.0	mA	*3
	I_{DD5}	V_{DD} V_{DD}=5V,STANDBY Mode			4.0	μA	*3
	I_{ADD}	AV_{DD} AV_{DD}=V_{DD}=V_{REF}=5V, ADCK=225kHz		3.0	5.0	mA	*3
High-Level Input Voltage	V_{IH1}	AIN4/PA0–AIN7/PA3, PB0–PB3, PC0, PC1, PD0–PD3, PE0–PE3, AIN0/PI0–AIN3/PI3, SDI(O)/PL1, SCK/CKOUT	0.7V_{DD}		V_{DD}	V	*1
	V_{IH2}	PF0–PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, $\overline{\text{EXTI}}$/PK0, CNTI/PK1, $\overline{\text{RESET}}$	0.8V_{DD}		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-1.0		V_{DD}	V	
Low-Level Input Voltage	V_{IL1}	AIN4/PA0–AIN7/PA3, PB0–PB3, PC0, PC1, PD0–PD3, PE0–PE3, AIN0/PI0–AIN3/PI3, SDI(O)/PL1, SCK/CKOUT	0		0.3V_{DD}	V	*1
	V_{IL2}	PF0–PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, $\overline{\text{EXTI}}$/PK0, CNTI/PK1, $\overline{\text{RESET}}$	0		0.2V_{DD}	V	*1
	V_{IL3}	OSC1	0		1.0	V	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Excludes the current drawn though internal pull-up resistors.

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS 1-2 (V_{DD}=3.6–5.5V, V_{SS}=0V, Ta= -20–75°C)

PARAMETER	SYMBOL	C O N D I T I O N S	MIN	TYP	MAX	UNIT	NOTE
High-Level Input Current	I_{IH1}	V_{DD}=5.5V,V_{IN}=5.5V AIN4/PA0–AIN7/PA3, PB0–PB3, PC0,PC1, PD0–PD3, PE0–PE3, PF0–PF2, PG0,PG1, PH0,PH1, AIN0/PI0–AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1, SCK/CKOUT, RESET			10	µA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=5.5V,V_{IN}=0V Without Pull-up Resistance AIN4/PA0–AIN7/PA3, PB0–PB3,PC0, PC1, PD0–PD3, PE0–PE3, PF0–PF2, PG0,PG1, PH0,PH1, AIN0/PI0–AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1,SCK/CKOUT, RESET			-10	µA	*1
	I_{IL2}	V_{DD}=5.5V,V_{IN}=0V With Pull-up Resistance AIN4/PA0–AIN7/PA3, PB0–PB3, PC0, PC1, PD0–PD3, PE0–PE3, PF0–PF2,PG0,PG1,PH0,PH1, AIN0/PI0–AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1,SCK/CKOUT			-100	µA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-100µA PD0–PD3, PE0–PE3, PF0–PF2, PG0,PG1, PH0, PH1, SDO/PL0, SDI(O)/PL1, SCK/CKOUT	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=400µA PD0–PD3, PE0–PE3, PF0–PF2, PG0,PG1, PH0,PH1, SDO/PL0, SDI(O)/PL1 SCK/CKOUT			0.5	V	*2
	V_{OL2}	I_{OL2}=15mA AIN4/PA0–AIN7/PA3, PB0–PB3, PC0, PC1			2.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=5.5V, V_{OH}=5.5V AIN4/PA0–AIN7PA3, PB0–PB3, PC0, PC1			10	µA	*2
Input Capacitance	C_{IN}	Except V_{DD}, V_{SS} terminals f_{OSC}=1MHz		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS 2-1 (V_{DD}=2.4–3.6V, V_{SS}=0V, Ta= -20–75°C)

PARAMETER	SYMBOL	C O N D I T I O N S	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	2.4		3.6	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=3V,f_{OSC}=1MHz X'tal Oscillation In Reset		0.3	0.5	mA	*3
	I_{DD2}	V_{DD} V_{DD}=3V,f_{OSC}=1MHz Ceramic Oscillation In Reset		0.3	0.5	mA	*3
	I_{DD3}	V_{DD} V_{DD}=3V,f_{OSC}=1MHz CR Oscillation In Reset		0.4	0.6	mA	*3
	I_{DD4}	V_{DD} V_{DD}=3V,f_{OSC}=2MHz Operating (Except ADC)		0.6	1.0	mA	*3
	I_{DD5}	V_{DD} V_{DD}=3V, STANDBY Mode			2.0	μA	*3
	I_{ADD}	AV_{DD} AV_{DD}=V_{DD}=V_{REF}=3V, ADCK=225kHz		2.5	3.5	mA	*3
High-Level Input Voltage	V_{IH1}	AIN4/PA0–AIN7/PA3, PB0–PB3, PC0, PC1, PD0–PD3, PE0–PE3, AIN0/PI0–AIN3/PI3, SDI(O)/PL1, SCK/CKOUT	0.8V_{DD}		V_{DD}	V	*1
	V_{IH2}	PF0–PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, $\overline{\text{EXTI}}$/PK0, CNTI/PK1, $\overline{\text{RESET}}$	0.85V_{DD}		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-0.3		V_{DD}	V	
Low-Level Input Voltage	V_{IL1}	AIN4/PA0–AIN7/PA3, PB0–PB3, PC0, PC1, PD0–PD3, PE0–PE3, AIN0/PI0–AIN3/PI3, SDI(O)/PL1, SCK/CKOUT	0		0.2V_{DD}	V	*1
	V_{IL2}	PF0–PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, $\overline{\text{EXTI}}$/PK0, CNTI/PK1, $\overline{\text{RESET}}$	0		0.15V_{DD}	V	*1
	V_{IL3}	OSC1	0		0.3	V	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Excludes the current drawn though internal pull-up resistors.

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS 2-2 (V_{DD}=2.4–3.6V, V_{SS}=0V, Ta=-20–75°C)

PARAMETER	SYMBOL	C O N D I T I O N S	MIN	TYP	MAX	UNIT	NOTE
High-Level Input Current	I_{IH}	V_{DD}=3.6V,V_{IN}=3.6V AIN4/PA0–AIN7/PA3, PB0–PB3, PC0,PC1, PD0–PD3, PE0–PE3, PF0–PF2, PG0,PG1, PH0, PH1, AIN0/PI0–AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1,SCK/CKOUT, $\overline{\text{RESET}}$			10	μA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=3.6V,V_{IN}=0V Without Pull-up Resistance AIN4/PA0–AIN7/PA3, PB0–PB3, PC0,PC1, PD0–PD3, PE0–PE3, PF0–PF2, PG0,PG1,PH0,PH1, AIN0/PI0–AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1,SCK/CKOUT $\overline{\text{RESET}}$			-10	μA	*1
	I_{IL2}	V_{DD}=3.6V,V_{IN}=0V With Pull-up Resistance AIN4/PA0–AIN7/PA3, PB0–PB3, PC0,PC1, PD0–PD3, PE0–PE3, PF0–PF2, PG0,PG1,PH0,PH1, AIN0/PI0–AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1,SCK/CKOUT			-100	μA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-80μA PD0–PD3, PE0–PE3, PF0–PF2, PG0,PG1,PH0,PH1, SDO/PL0, SDI(O)/PL1, SCK/CKOUT	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=350μA PD0–PD3, PE0–PE3, PF0–PF2, PG0,PG1,PH0,PH1, SDO/PL0, SDI(O)/PL1, SCK/CKOUT			0.5	V	*2
	V_{OL2}	I_{OL2}=5mA AIN4/PA0–AIN7/PA3, PB0–PB3, PC0, PC1			1.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=3.6V, V_{OH}=3.6V AIN4/PA0–AIN7/PA3, PB0–PB3, PC0, PC1			10	μA	*2
Input Capacitance	C_{IN}	Except V_{DD},V_{SS} terminals f_{OSC}=1MHz		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.

■ ELECTRICAL CHARACTERISTICS

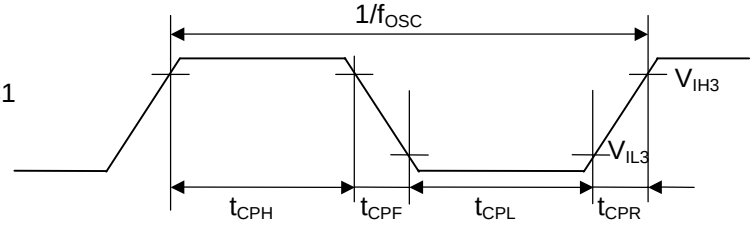
AC CHARACTERISTICS 1 (V_{SS}=0V, Ta=-20–75°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Frequency	f_{OSC}	V_{DD}=2.4–3.6V	X'tal Resonator	0.03		2.0	MHz
			Ceramic Resonator	0.03		2.0	
			External Resistor Oscillation	0.03		1.0	
			External Clock	0.03		2.0	
		V_{DD}=3.6–5.5V	X'tal Resonator	0.03		4.0	
			Ceramic Resonator	0.03		4.0	
			External Resistor Oscillation	0.03		2.0	
			External Clock	0.03		4.0	
Instruction Cycle Time	t_C				$6/f_{OSC}$		s
External Clock Pulse Width	t_{CPH}	V_{DD}=2.4–3.6V		250		16600	ns
	t_{CPL}	V_{DD}=3.6–5.5V		125		16600	
External Clock Rise Time / Fall Time	t_{CPR} / t_{CPF}	V_{DD}=2.4–5.5V				20	ns
RESET Low-Level Width	t_{RST}	V_{DD}=2.4–5.5V		$4/f_{OSC}$			s
RESET Rise Time	t_{RSR}	V_{DD}=2.4–5.5V				20	ms
Port Input Level Width	t_{PIN}	V_{DD}=2.4–5.5V		$6/f_{OSC}$			s
Edge Detection Rise Time / Fall Time	t_{EDR} / t_{EDF}	V_{DD}=2.4–5.5V PH1 terminal				200	ns
Restart Signal Rise Time	t_{STR}	V_{DD}=2.4–5.5V PH0 terminal				200	ns
External Interrupt Signal Rise Time / Fall Time	t_{EXR} / t_{EXF}	V_{DD}=2.4–5.5V EXTI/PK0 terminal				200	ns
CNTI Clock Frequency	f_{CT}	V_{DD}=2.4–5.5V CNTI/PK1 terminal				$f_{OSC}/64$	Hz
CNTI High Level Width	t_{CT}	V_{DD}=2.4–5.5V CNTI/PK1 terminal		$6/f_{OSC}$			s
CNTI Rise Time / Fall Time	t_{CTR} / t_{CTF}	V_{DD}=2.4–5.5V CNTI/PK1 terminal				200	ns

■ AC CHARACTERISTICS 1 TIMING CHART

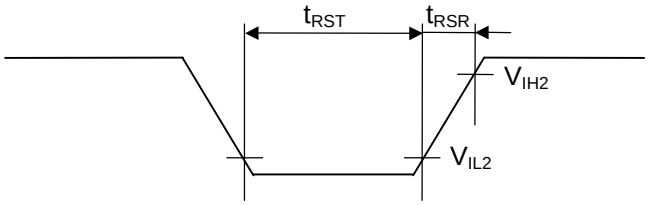
EXTERNAL CLOCK

OSC1



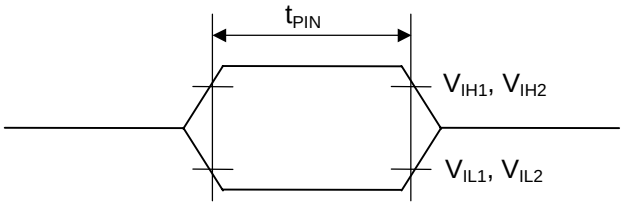
RESET INPUT

$\overline{\text{RESET}}$



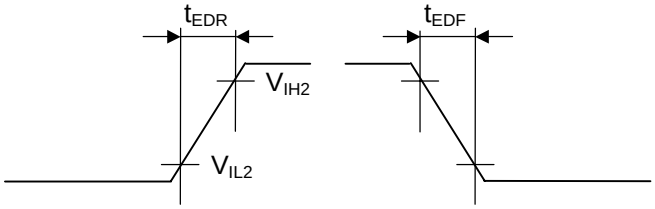
PORT INPUT

PORT



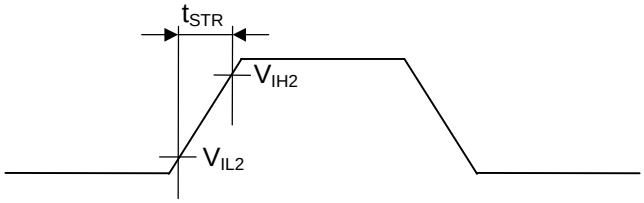
EDGE DETECTOR INPUT

PH1



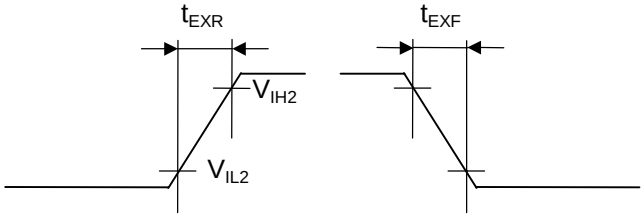
RESTART SIGNAL INPUT

PH0



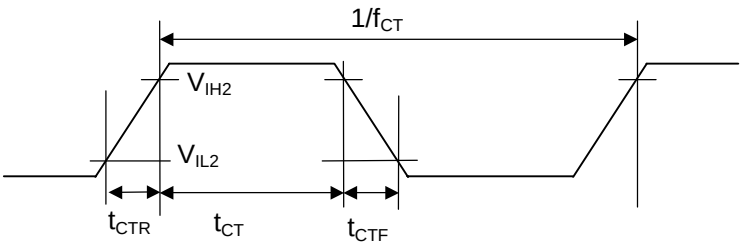
EXTERNAL INTERRUPT

EXTI



CNTI CLOCK

CNTI



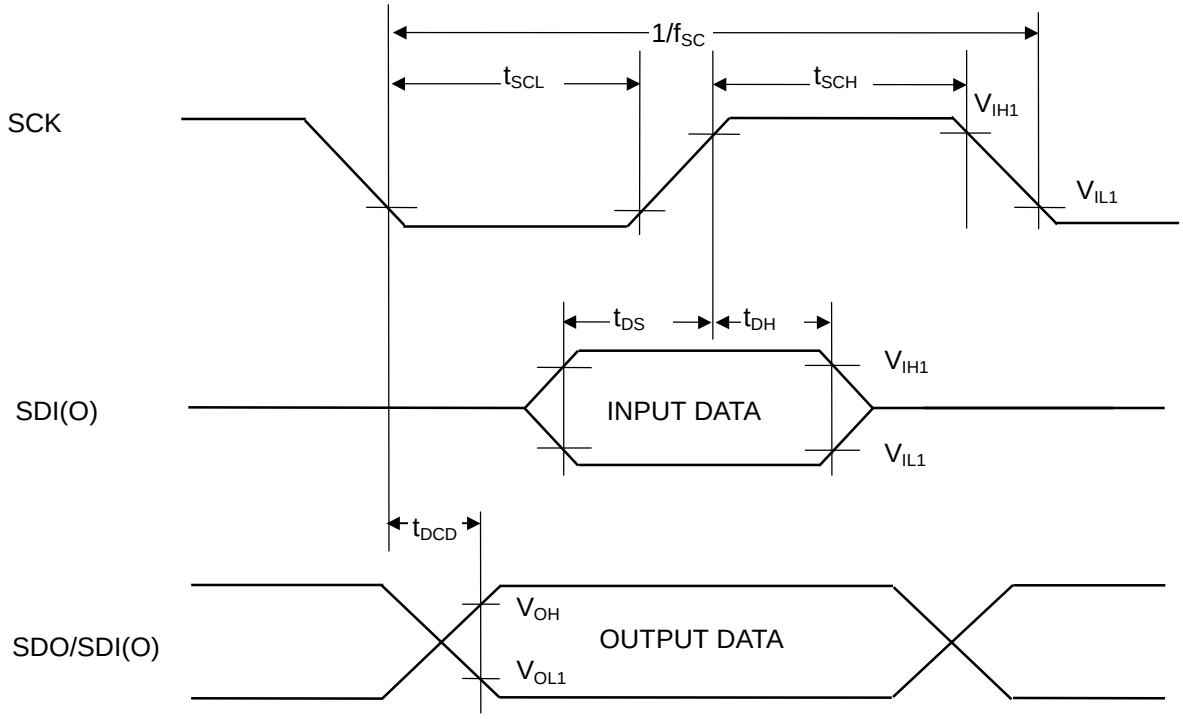
■ ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS 2 SERIAL INTERFACE (V_{DD}=2.4–5.5V, V_{SS}=0V, Ta=-20–75°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Serial Operating Frequency	f_{SC}	Internal Clock				(1/12)×f_{OSC}*	Hz
		External Clock				500k	
Clock Pulse Width Low-Level	t_{SCL}	Internal Clock	V_{DD}=2.4–3.6V f_{OSC}=2MHz	3.0			µs
			V_{DD}=3.6–5.5V f_{OSC}=4MHz	1.5			
		External Clock		1.0			
Clock Pulse Width High-Level	t_{SCH}	Internal Clock	V_{DD}=2.4–3.6V f_{OSC}=2MHz	3.0			µs
			V_{DD}=3.6–5.5V f_{OSC}=4MHz	1.5			
		External Clock		1.0			
SDI setup Time To SCK ↑	t_{DS}			0.5			µs
SDI Hold time To SCK ↑	t_{DH}			0.5			µs
SDO Data Fix Time To SCK ↓	t_{DCD}					0.5	µs

***** The maximum frequency of the internal serial clock f_{SC} is selected the one-divided output of the prescaler by the mask option.

■ AC CHARACTERISTICS 2 SERIAL INTERFACE TIMING CHART



■ ELECTRICAL CHARACTERISTICS

A/D CONVERTER CHARACTERISTICS

(V_{DD}=AV_{DD}=2.4–5.5V, V_{SS}=AV_{SS}=0V, Ta=25°C, f_{OSC}=4MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution	–		–	8	–	bits
Absolute Accuracy	–	V_{DD}=5V,AV_{DD}=5V,V_{REF}=5V			±2	LSB
Conversion time	t_{CONV}	V_{DD}=5V,AV_{DD}=5V,V_{REF}=5V	40			µs
Reference Voltage	V_{REF}		2.4		AV_{DD}	V
Analog Input Voltage	V_{IA}		AV_{SS}		V_{REF}	V
ADCK frequency	f_{ADCK}				225	kHz

■ MASK OPTION

The **NJU3505** can set or select the following options by the mask option using the same mask of program coding in ROM.

1) INPUT OUTPUT Terminal Selection

All of input-output terminals can select a type for each port from the following table1 to table2 by the mask option.

[CIRCUIT TYPE TABLE 1]

SYMBOL	TERMINAL TYPES					REMARKS	
	Input / Output Terminal *1			EXTRA FUNCTION			
	Port of Input	Port of Output	Programmable Input / Output				
AIN4 / PA0			IOP IO	AD	Analog input (AIN4)		
AIN5 / PA1			IOP IO	AD	Analog input (AIN5)		
AIN6 / PA2			IOP IO	AD	Analog input (AIN6)		
AIN7 / PA3			IOP IO	AD	Analog input (AIN7)		
PB0			IOP IO				
PB1			IOP IO				
PB2			IOP IO				
PB3			IOP IO				
PC0	ICP IC	ONP ON					
PC1	ICP IC	ONP ON					
PD0	ICP IC	OC					
PD1	ICP IC	OC					
PD2	ICP IC	OC					
PD3	ICP IC	OC					
PE0	ICP IC	OC					
PE1	ICP IC	OC					
PE2	ICP IC	OC					
PE3	ICP IC	OC					

Note) “AD, IC, ICP, IO, IOP, OC, ON, ONP” are symbols using on MASK OPTION GENERATOR(MOG).

*1) The symbol and the detail circuits of INPUT OUTPUT TERMINAL are written in INPUT OUTPUT TERMINAL TYPE.

[CIRCUIT TYPE TABLE 2]

SYMBOL	TERMINAL TYPES					REMARKS	
	Input / Output Terminal *1			EXTRA FUNCTION			
	Port of Input	Port of Output	Programmable Input / Output				
PF0	ISP IS	OC					
PF1	ISP IS	OC					
PF2	ISP IS	OC					
PG0	ISP IS	OC					
PG1	ISP IS	OC					
PH0	ISP IS	OC			Restart signal input	E D	Restart signal input Not Restart
PH1	ISP IS	OC			Edge detector	R F D	Rising edge detector Falling edge detector Not edge detector
AIN0 / PI0	ICP IC			AD	Analog input (AIN0)		
AIN1 / PI1	ICP IC			AD	Analog input (AIN1)		
AIN2 / PI2	ICP IC			AD	Analog input (AIN2)		
AIN3 / PI3	ICP IC			AD	Analog input (AIN3)		
V_{REF} / PJ0	ISP IS			AD	Reference input		
ADCK / PJ1 *2	ISP IS			ACP AC	External clock input		
EXTI / PK0 *2	ISP IS			IIP II	External Interrupt input	R F	Rising edge Falling edge
CNTI / PK1 *2	ISP IS			IIP II	External clock to Timer2 input		
SDO / PL0		OC		SO	Serial data output	MSB LSB	MSB first LSB first
SDI(O) / PL1 *2	ICP IC	OC		SDP SD	Serial data input / output		
SCK / CKOUT *2 *3				SCP SC	Serial clock input-output		
				-	Output clock divide by prescaler		

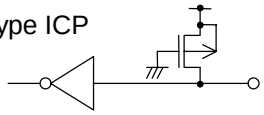
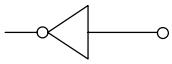
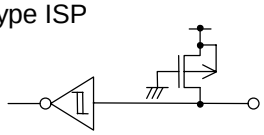
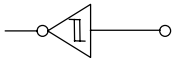
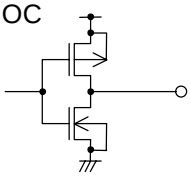
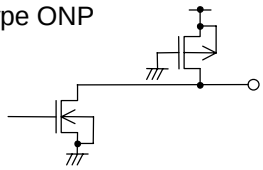
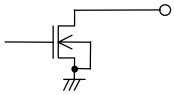
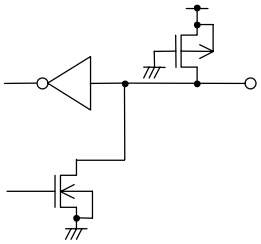
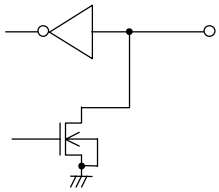
Note) “AC, ACP, AD, D, E, F, IC, ICP, II, IIP, IS, ISP, LSB, MSB, OC, R, SC, SCP, SD, SDP, SO” are symbols using on MASK OPTION GENERATOR(MOG).

*1) The symbol and the detail circuits of INPUT OUTPUT TERMINAL are written in INPUT OUTPUT TERMINAL TYPE.

*2) The pull-up resistance is added to the terminal selected as the extra function.

*3) When Serial INPUT-OUTPUT is selected, “SCK” is selected automatically. When it is not selected, “CKOUT” is selected automatically.

INPUT OUTPUT TERMINAL TYPES

	Types	With Pull-up	Without Pull-up	Terminals
INPUT TERMINAL	C-MOS	Type ICP 	Type IC 	PC0, PC1, PD0–PD3, PE0–PE3, AIN0/PI0– AIN3/PI3, SDI(O)/PL1
	SCHMITT TRIGGER	Type ISP 	Type IS 	PF0–PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1
OUTPUT TERMINAL	C-MOS		Type OC 	PD0–PD3, PE0–PE3, PF0–PF2, PG0, PG1, PH0, PH1, SDO/PL0, SDI(O)/PL1
	N-channel (Nch) OPEN DRAIN	Type ONP 	Type ON 	PC0, PC1
PROGRAMMABLE INPUT OUTPUT TERMINAL	C-MOS INPUT / N-channel (Nch) OPEN DRAIN OUTPUT	Type IOP 	Type IO 	AIN4/PA0– AIN7/PA3, PB0–PB3

2) Restart signal Input Selection

PH0 terminal performs the extra function as the restart signal input terminal to return from the "STANDBY" mode. When the rising edge of the signal from the external circuit is input into the PH0 terminal in mode of "STANDBY", the "STANDBY" mode is released and the CPU starts the execution again from the suspended address of the program.

3)Edge Detector Selection

PH1 terminal performs the extra function as the edge detector terminal. When the PH1 terminal detects the edge of the signal from the external circuit, the third bit(b2) condition of PHY24 is set to "1". The “b2” of PHY24 is set to “1” even when the edge is input during the “STANDBY” mode. The condition of “b2” is kept until the writing operation to PHY24.

The polarity as low to high or high to low of the input signal edge can be selected by the mask option.

4)External Interrupt of the edge Selection

When PK0 terminal operates as EXTI Input terminal for the external interrupt, the polarity of the edge, rising as “low to high” or falling as “high to low”, is selected by the mask option.

5)The data order(MSB, LSB) of the Serial Interface

The data order of the Serial Interface can select either MSB or LSB first by the mask option.

6)A/D Control Clock

A/D Control Clock can select either the external clock from ADCK terminal or the internal clock from the Prescaler by the mask option.

7)Each Internal Clock

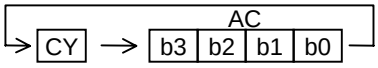
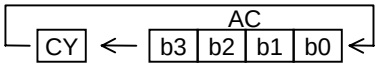
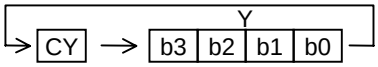
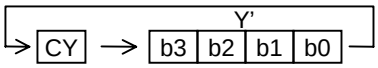
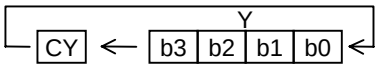
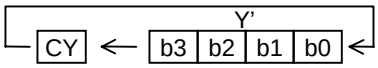
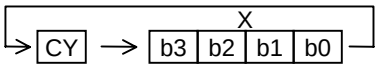
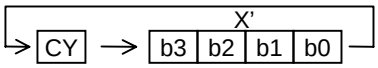
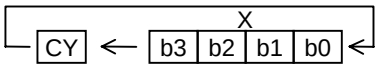
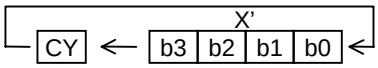
The count clocks of Timer1 and Timer2, the Internal shift clock of the Serial Interface, the clock of the A/D control clock and the output clock through the SCK/CKOUT terminal are clocks divided in the internal prescaler, and the frequency of this clock can be selected by the mask option from follows which are dividing numbers based on the inverse of the 1-instruction executing period $(1/f_{OSC} \times 6)$.

1/2, 1/4, 1/8, 1/16, 1/32,1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048,1/4096

Note) Count clock of Timer2 can select the internal or external clock by the program.
The shift clock of the serial interface can select the internal or external clock by the program.

■ MNEMONIC LIST

	Mnemonic	Operation code	Function	Status	Cycle	Memo
DATA TRANSFERENCE	TAY	04	Y←AC	1	1	RPC=0
			Y'←AC	1	1	RPC=1
	TYA	14	AC←Y	1	1	RPC=0
			AC←Y'	1	1	RPC=1
	XAX	1B	AC↔X	1	1	RPC=0
			AC↔X'	1	1	RPC=1
	TAP	26	PH(Y')←AC	1	1	
	TPA	16	AC←PH(Y')	1	1	
	TAPICY	17	PH(Y')←AC, Y←Y+1	*	1	
	TAPDCY	27	PH(Y')←AC, Y←Y-1	*	1	
	TMA	0D	AC←M(X,Y)	1	1	
	TAM	1D	M(X,Y)←AC	1	1	
	TAMICY	0A	M(X,Y)←AC, Y←Y+1	*	1	
	TAMDCY	1A	M(X,Y)←AC, Y←Y-1	*	1	
	TMY	05	Y←M(X,Y)	1	1	RPC=0
			Y'←M(X,Y)	1	1	RPC=1
	XMA	0B	AC↔M(X,Y)	1	1	
	TPMICY	03	M(X,Y)←PH(Y'), Y←Y+1	*	1	
	TMPICY	13	PH(Y')←M(X,Y), Y←Y+1	*	1	
	TRM	23	M(X,Y)←ROM(PHY13,X',AC)	1	2	Y = an even number : ROM of 4bit low-data
						Y = an odd number : ROM of 4bit hi-data
	CLA	80	AC←0	1	1	
	LDI A,#K	80–8F	AC←#K	1	1	#K=0–15
	LDI Y,#K	90–9F	Y←#K	1	1	RPC=0, #K=0–15
			Y'←#K	1	1	RPC=1, #K=0–15
	LDI X,#K	A0–AF	X←#K	1	1	RPC=0, #K=0–15
			X'←#K	1	1	RPC=1, #K=0–15
CALCULATING	ADD A,M	0E	AC←AC+M(X,Y)	*	1	
	INC A	71	AC←AC+1	*	1	
	DEC A	7F	AC←AC-1	*	1	
	ADD A,#K	70–7F	AC←AC+#K	*	1	#K=0–15
	AND A,M	0F	AC←AC∧M(X,Y)	*	1	
	CMP A,M	2E	AC< >M(X,Y)	*	1	
	CMP Y,#K	B0–BF	Y< >#K	*	1	#K=0–15
	INC Y	08	Y←Y+1	*	1	RPC=0
			Y'←Y'+1	*	1	RPC=1
	DEC Y	18	Y←Y-1	*	1	RPC=0
			Y'←Y'-1	*	1	RPC=1
	INC M	09	AC←M(X,Y)+1	*	1	
	DEC M	19	AC←M(X,Y)-1	*	1	
	YNEA	01	Y< >AC	*	1	
	OR A,M	1F	AC←AC∨M(X,Y)	*	1	
	XOR A,M	2F	AC←AC⊕M(X,Y)	*	1	
	NEG	2D	AC←0-AC	1	1	
	SUB A,M	1E	AC←M(X,Y)-AC	*	1	
	AND A,#K	40–4F	AC←AC∧#K	*	1	#K=0–15
	OR A,#K	50–5F	AC←AC∨#K	*	1	#K=0–15

	Mnemonic	Operation code	Function	Status	Cycle	Memo
BRANCH	JPL addr	68–6F	ST=1:PC←addr, ST=0:No branch	1	2	2byte Mnemonic
	JMP addr	C0–FF	ST=1:PC←addr, ST=0:No branch	1	1	
	CALL addr	60–67	ST=1:(SP)←PC+2, SP←SP+1, PC←addr ST=0:No branch	1	2	2byte Mnemonic
	RET	2B	PC←(SP), SP←SP-1	1	1	
	RETI	2C	PC←(SP), AC←(SP), SP←SP-1 X←(SP), X'←(SP), Y←(SP), Y' ←(SP) RPC← (SP), ST← (SP)	*	1	
BIT OPERATION	SBIT b	30–33	M(X,Y)b←1	1	1	B=0–3
	RBIT b	34–37	M(X,Y)b←0	1	1	B=0–3
	TBIT b	38–3B	ST←M(X,Y)b	*	1	B=0–3
	TBA b	3C–3F	ST←(AC)b	*	1	B=0–3
	RAR	21		*	1	
	RAL	22		*	1	
	RYR	24		*	1	RPC=0
				*	1	RPC=1
	RYL	25		*	1	RPC=0
				*	1	RPC=1
	RXR	28		*	1	RPC=0
				*	1	RPC=1
	RXL	29		*	1	RPC=0
				*	1	RPC=1
	SEC	0C	CY←1	1	1	
	CLC	1C	CY←0	0	1	
	SRPC	10	RPC←1	1	1	
	RRPC	20	RPC←0	1	1	
SPECIAL	NOP	00	No Operation	1	1	
	HLT	07	CPU Halted	1	1	
	MDT	06	Memory Dump Test	–	–	

Note)

←	:Transfer direction	AC	:Accumulator	SP	:Stack pointer
∧	:AND	X	:Xregister	RPC	:RPC flag
∨	:OR	X'	:X'register	CY	:Carry flag
⊕	:Exclusive OR	Y	:Yregister	ST	:Status flag
+	:Add	Y'	:Y'register	#K	:Immediate data
-	:Subtraction	PH	:Peripheral register	addr	:Blanch address
< >	:Comparison	M	:Data memory	( )	:A content of register or memory pointed by the address indicated in ( ).
		ROM	:Program memory		
		PC	:Program counter	b	:Bit position

Status description)

0:After the command execution, ST-flag is always set to "0".

1:After the command execution, ST-flag is always set to "1".

*:Status

[CAUTION]
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