CY7C1354C, CY7C1356C

9-Mbit (256K x 36/512K x 18) Pipelined SRAM with NoBL™ Architecture

Features

- Pin-compatible and Functionally equivalent to ZBT
- Supports 250 MHz Bus Operations with Zero Wait States
  - Available speed grades are 250, 200, and 166 MHz
- Internally Self-timed Output Buffer Control to eliminate the need to use Asynchronous $\overline{OE}$
- Fully Registered (Inputs and Outputs) for Pipelined Operation
- Byte Write capability
- Single 3.3V Power Supply (V_{DD})
- 3.3V or 2.5V I/O Power Supply (V_{DDQ})
- Fast Clock-to-output Times
  - 2.8 ns (for 250 MHz device)
- Clock Enable ($\overline{CEN}$) Pin to suspend Operation
- Synchronous Self-timed Writes
- Available in Pb-free 100-Pin TQFP Package, Pb-free, and non Pb-free 119-Ball BGA Package and 165-Ball FBGA Package
- IEEE 1149.1 JTAG-Compatible Boundary Scan
- Burst Capability – Linear or Interleaved Burst Order
- "ZZ" Sleep Mode option and Stop Clock option

Functional Description

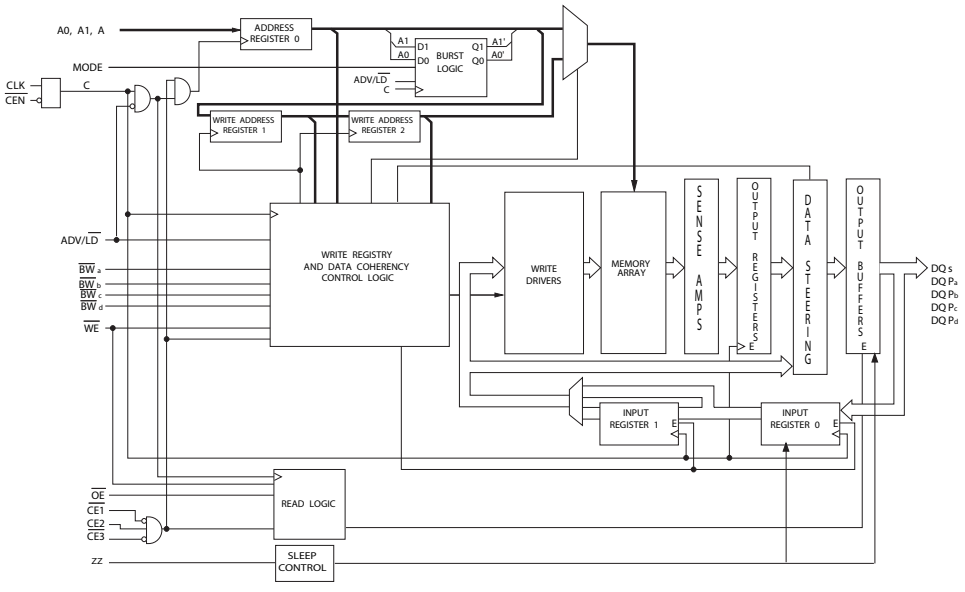
The CY7C1354C and CY7C1356C[1] are 3.3V, 256K x 36 and 512K x 18 Synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back read/write operations with no wait states. The CY7C1354C and CY7C1356C are equipped with the advanced (NoBL) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature greatly improves the throughput of data in systems that require frequent write/read transitions. The CY7C1354C and CY7C1356C are pin compatible and functionally equivalent to ZBT devices.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.

Write operations are controlled by the Byte Write Selects ($\overline{BW_a}$–$\overline{BW_d}$ for CY7C1354C and $\overline{BW_a}$–$\overline{BW_b}$ for CY7C1356C) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output tristate control. To avoid bus contention, the output drivers are synchronously tristated during the data portion of a write sequence.

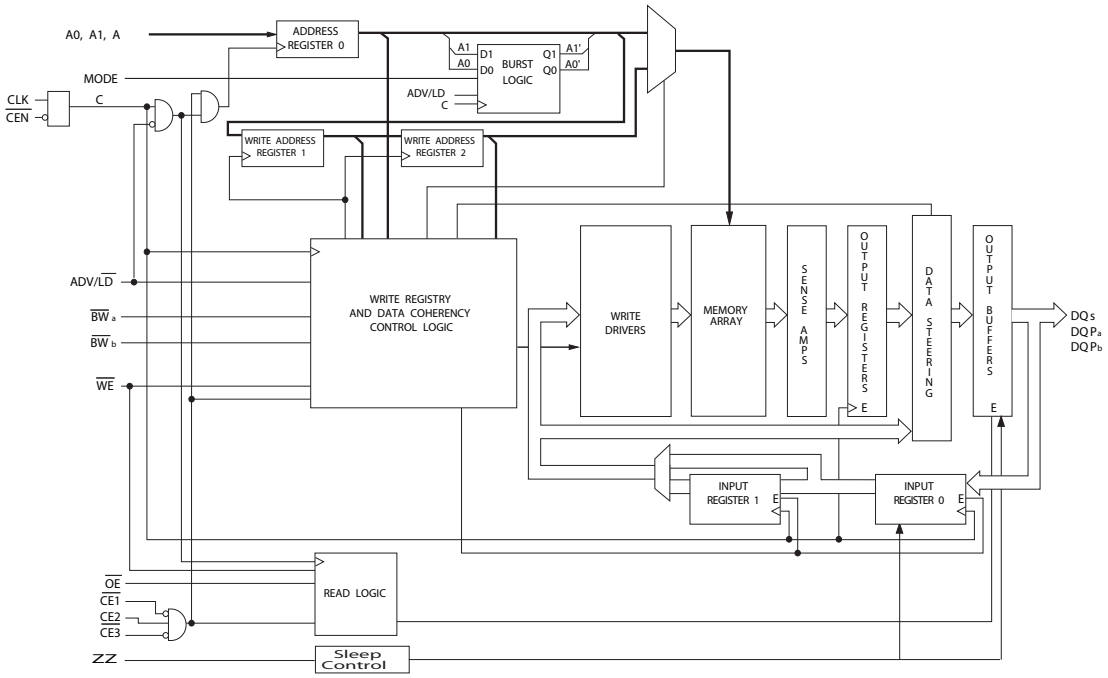
Logic Block Diagram–CY7C1354C (256K x 36)



Note

1. For best-practices recommendations, refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Logic Block Diagram–CY7C1356C (512K x 18)



Selection Guide

Description	250 MHz	200 MHz	166 MHz	Unit
Maximum Access Time	2.8	3.2	3.5	ns
Maximum Operating Current	250	220	180	mA
Maximum CMOS Standby Current	40	40	40	mA

Pin Configurations (continued)

Figure 1. 100-Pin TQFP

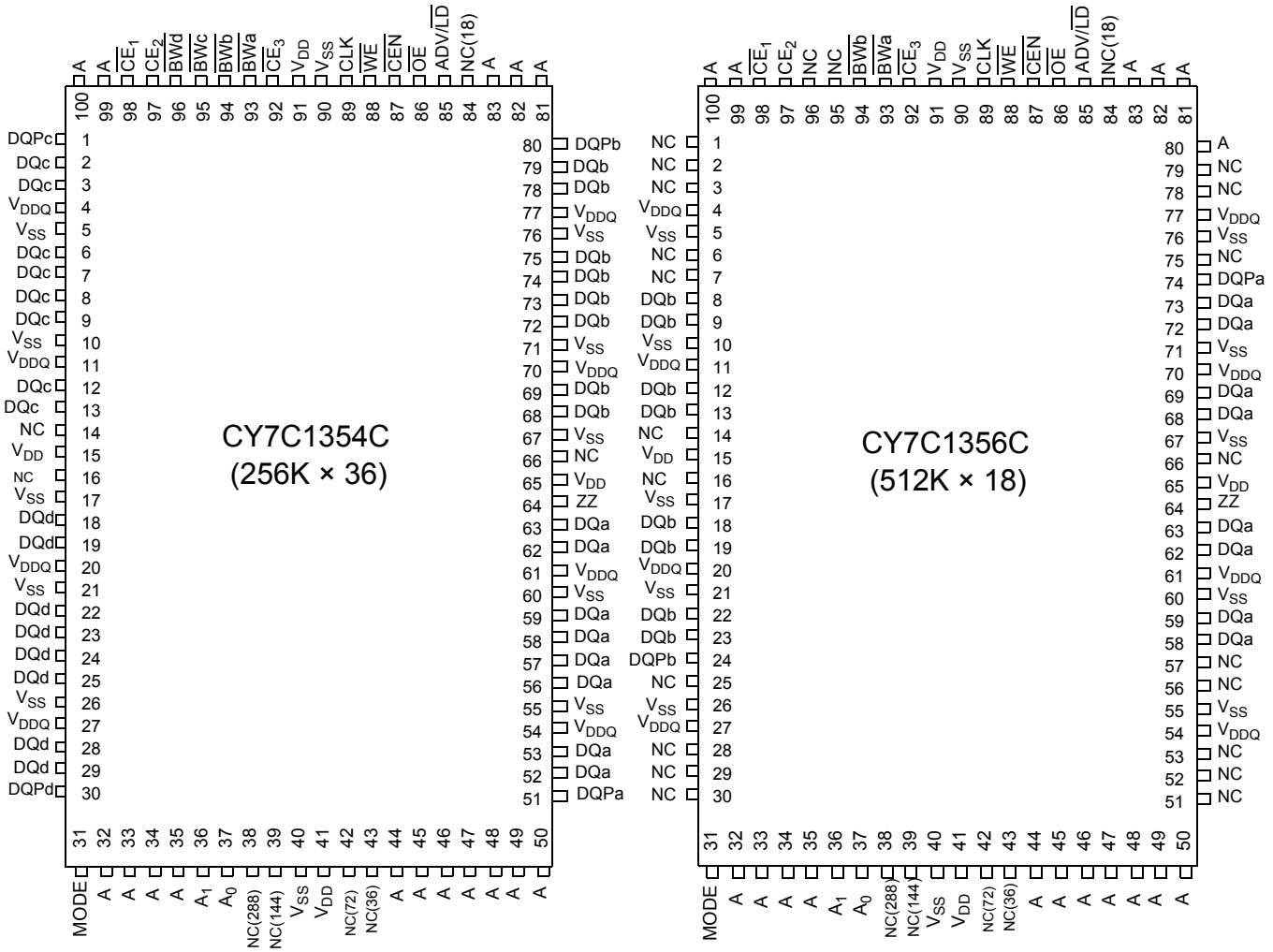


Figure 2. 119-Ball BGA Pinout

CY7C1354C (256K × 36)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC/18M	A	A	V_{DDQ}
B	NC/576M	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC/1G	A	A	V_{DD}	A	A	NC
D	DQ_c	DQP_c	V_{SS}	NC	V_{SS}	DQP_b	DQ_b
E	DQ_c	DQ_c	V_{SS}	$\overline{CE_1}$	V_{SS}	DQ_b	DQ_b
F	V_{DDQ}	DQ_c	V_{SS}	$\overline{OE}$	V_{SS}	DQ_b	V_{DDQ}
G	DQ_c	DQ_c	$\overline{BW_c}$	A	$\overline{BW_b}$	DQ_b	DQ_b
H	DQ_c	DQ_c	V_{SS}	$\overline{WE}$	V_{SS}	DQ_b	DQ_b
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_d	DQ_d	V_{SS}	CLK	V_{SS}	DQ_a	DQ_a
L	DQ_d	DQ_d	$\overline{BW_d}$	NC	$\overline{BW_a}$	DQ_a	DQ_a
M	V_{DDQ}	DQ_d	V_{SS}	$\overline{CEN}$	V_{SS}	DQ_a	V_{DDQ}
N	DQ_d	DQ_d	V_{SS}	A1	V_{SS}	DQ_a	DQ_a
P	DQ_d	DQP_d	V_{SS}	A0	V_{SS}	DQP_a	DQ_a
R	NC/144M	A	MODE	V_{DD}	NC	A	NC/288M
T	NC	NC/72M	A	A	A	NC/36M	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

CY7C1356C (512K x 18)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC/18M	A	A	V_{DDQ}
B	NC/576M	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE_3}$	NC
C	NC/1G	A	A	V_{DD}	A	A	NC
D	DQ_b	NC	V_{SS}	NC	V_{SS}	DQP_a	NC
E	NC	DQ_b	V_{SS}	$\overline{CE_1}$	V_{SS}	NC	DQ_a
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_a	V_{DDQ}
G	NC	DQ_b	$\overline{BW_b}$	A	V_{SS}	NC	DQ_a
H	DQ_b	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQ_a	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_b	V_{SS}	CLK	V_{SS}	NC	DQ_a
L	DQ_b	NC	V_{SS}	NC	$\overline{BW_a}$	DQ_a	NC
M	V_{DDQ}	DQ_b	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	DQ_b	NC	V_{SS}	A1	V_{SS}	DQ_a	NC
P	NC	DQP_b	V_{SS}	A0	V_{SS}	NC	DQ_a
R	NC/144M	A	MODE	V_{DD}	NC	A	NC/288M
T	NC/72M	A	A	NC/36M	A	A	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Figure 3. 165-Ball FBGA

CY7C1354C (256K × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_c$	$\overline{BW}_b$	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC/1G	A	CE2	$\overline{BW}_d$	$\overline{BW}_a$	CLK	$\overline{WE}$	$\overline{OE}$	NC/18M	A	NC
C	DQP_c	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_b
D	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
E	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
F	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
G	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
K	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
L	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
M	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
N	DQP_d	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_a
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

CY7C1356C (512K × 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_b$	NC	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	A
B	NC/1G	A	CE2	NC	$\overline{BW}_a$	CLK	$\overline{WE}$	$\overline{OE}$	NC/18M	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_a
D	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
E	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
F	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
G	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
K	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
L	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
M	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
N	DQP_b	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

Pin Definitions

Pin Name	I/O Type	Pin Description
A0, A1 A	Input- Synchronous	**Address Inputs used to select one of the address locations**. Sampled at the rising edge of the CLK.
$\overline{BW}_a$,$\overline{BW}_b$, $\overline{BW}_c$,$\overline{BW}_d$,	Input- Synchronous	**Byte Write Select Inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW}_a$ controls DQ_a and DQP_a, $\overline{BW}_b$ controls DQ_b and DQP_b, $\overline{BW}_c$ controls DQ_c and DQP_c, $\overline{BW}_d$ controls DQ_d and DQP_d.
$\overline{WE}$	Input- Synchronous	**Write Enable Input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input- Synchronous	**Advance/Load Input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW to load a new address.
CLK	Input- Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input- Synchronous	**Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input- Synchronous	**Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input- Synchronous	**Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input- Asynchronous	**Output Enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a Write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input- Synchronous	**Clock Enable Input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_S	I/O- Synchronous	**Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by addresses during the previous clock rise of the Read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_d are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O- Synchronous	**Bidirectional Data Parity I/O lines**. Functionally, these signals are identical to $DQ_{[a:d]}$. During write sequences, DQP_a is controlled by BW_a, DQP_b is controlled by BW_b, DQP_c is controlled by BW_c, and DQP_d is controlled by BW_d.
MODE	Input Strap Pin	**Mode Input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.
TDO	JTAG serial output Synchronous	**Serial data out to the JTAG circuit**. Delivers data on the negative edge of TCK.
TDI	JTAG serial input Synchronous	**Serial data In to the JTAG circuit**. Sampled on the rising edge of TCK.
TMS	Test Mode Select Synchronous	**This pin controls the Test Access Port state machine**. Sampled on the rising edge of TCK.
TCK	JTAG-Clock	**Clock input to the JTAG circuitry**.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.

Pin Definitions (continued)

Pin Name	I/O Type	Pin Description
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
NC	–	**No connects**. This pin is not connected to the die.
NC (18, 36, 72, 144, 288, 576, 1G)	–	**These pins are not connected**. They will be used for expansion to the 18M, 36M, 72M, 144M 288M, 576M, and 1G densities.
ZZ	Input-Asynchronous	**ZZ "sleep" Input**. This active HIGH input places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.

Functional Overview

The CY7C1354C and CY7C1356C are synchronous-pipelined Burst NoBL SRAMs designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 2.8 ns (250 MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a Read or Write operation, depending on the status of the Write Enable ($\overline{WE}$). $BW_{[d:a]}$ can be used to conduct Byte Write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All Writes are simplified with on-chip synchronous self-timed Write circuitry. Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and enables the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and to the data bus within 2.8 ns (250 MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output tristates following the next clock rise.

Burst Read Accesses

The CY7C1354C and CY7C1356C have an on-chip burst counter that enables the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load a new address into the SRAM, as described in the Single Read Accesses section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wrap around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ increments the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are ALL asserted active, and (3) the Write signal $\overline{WE}$ is asserted LOW. The address presented to A_0–A_{16} is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically tristated regardless of the state of the $\overline{OE}$ input signal. This enables the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354C and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356C). In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the address register if the appropriate control signals are asserted.

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354C and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356C or a subset for byte write operations, see the table Partial Write Cycle Description on page 9 for details) inputs is latched into the device and the Write is complete.

The data written during the Write operation is controlled by $\overline{BW}$ ($\overline{BW}_{a,b,c,d}$ for CY7C1354C and $\overline{BW}_{a,b}$ for CY7C1356C) signals. The CY7C1354C/CY7C1356C provides Byte Write capability that is described in the Write Cycle Description table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BW}$) input will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation remain unaltered. A synchronous self-timed write mechanism is provided to simplify the Write operations. Byte Write capability is included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple Byte Write operations.

Because the CY7C1354C and CY7C1356C are common I/O devices, data should not be driven into the device while the outputs are active. The Output Enable ($\overline{OE}$) can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354C and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356C) inputs. Doing so will tristate the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354C and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356C) are automatically tristated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1354C/CY7C1356C has an on-chip burst counter that enables the user the ability to supply a single address and conduct up to four WRITE operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load the initial address, as described in Single Write Accesses on page 7. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the chip enables ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct BW ($\overline{BW}_{a,b,c,d}$ for CY7C1354C and $\overline{BW}_{a,b}$ for CY7C1356C) inputs must be driven in each cycle of the burst write to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation ‘sleep’ mode. Two clock cycles are required to enter into or exit from this ‘sleep’ mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Table 1. Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address	Second Address	Third Address	Fourth Address
A1,A0	A1,A0	A1,A0	A1,A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Table 2. Linear Burst Address Table (MODE = GND)

First Address	Second Address	Third Address	Fourth Address
A1,A0	A1,A0	A1,A0	A1,A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Table 3. ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq V_{DD} - 0.2V$		50	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Truth Table

The Truth Table for CY7C1354C and CY7C1356C follows. [2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE}$	ZZ	$\overline{ADV/LD}$	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	L	L	X	X	X	L	L-H	Tri-State
Continue Deselect Cycle	None	X	L	H	X	X	X	L	L-H	Tri-State
Read Cycle (Begin Burst)	External	L	L	L	H	X	L	L	L-H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	L	H	X	X	L	L	L-H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	L	L	H	X	H	L	L-H	Tri-State
Dummy Read (Continue Burst)	Next	X	L	H	X	X	H	L	L-H	Tri-State
Write Cycle (Begin Burst)	External	L	L	L	L	L	X	L	L-H	Data In (D)
Write Cycle (Continue Burst)	Next	X	L	H	X	L	X	L	L-H	Data In (D)
NOP/WRITE ABORT (Begin Burst)	None	L	L	L	L	H	X	L	L-H	Tri-State
WRITE ABORT (Continue Burst)	Next	X	L	H	X	H	X	L	L-H	Tri-State
IGNORE CLOCK EDGE (Stall)	Current	X	L	X	X	X	X	H	L-H	-
SLEEP MODE	None	X	H	X	X	X	X	X	X	Tri-State

Partial Write Cycle Description

The following table lists the Partial Write Cycle Description for CY7C1354C.[2, 3, 4, 9]

Function (CY7C1354C)	$\overline{WE}$	$\overline{BW_d}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	X	X	X	X
Write –No bytes written	L	H	H	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	H	H	L
Write Byte b – (DQ_b and DQP_b)	L	H	ThH	L	H
Write Bytes b, a	L	H	H	L	L
Write Byte c – (DQ_c and DQP_c)	L	H	L	H	H
Write Bytes c, a	L	H	L	H	L
Write Bytes c, b	L	H	L	L	H
Write Bytes c, b, a	L	H	L	L	L
Write Byte d – (DQ_d and DQP_d)	L	L	H	H	H
Write Bytes d, a	L	L	H	H	L
Write Bytes d, b	L	L	H	L	H
Write Bytes d, b, a	L	L	H	L	L
Write Bytes d, c	L	L	L	H	H
Write Bytes d, c, a	L	L	L	H	L

Notes
2. X = “Don't Care”, H = Logic HIGH, L = Logic LOW, CE stands for ALL Chip Enables active. BWx = L signifies at least one Byte Write Select is active, BWx = Valid signifies that the desired Byte Write Selects are asserted, see Write Cycle Description table for details.
3. Write is defined by WE and BWX. See Write Cycle Description table for details.
4. When a write cycle is detected, all I/Os are tri-stated, even during Byte Writes.
5. The DQ and DQP pins are controlled by the current cycle and the OE signal.
6. CEN = H inserts wait states.
7. Device will power up deselected and the I/Os in a tri-state condition, regardless of OE.
8. OE is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQPX = Tri-state when OE is inactive or when the device is deselected, and DQs = data when OE is active.
9. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW_X}$ is valid. Appropriate write will be done based on which byte write is active.

Partial Write Cycle Description

The following table lists the Partial Write Cycle Description for CY7C1354C.[2, 3, 4, 9]

Function (CY7C1354C)	$\overline{WE}$	$\overline{BW_d}$	$\overline{BW_c}$	$\overline{BW_b}$	$\overline{BW_a}$
Write Bytes d, c, b	L	L	L	L	H
Write All Bytes	L	L	L	L	L

Partial Write Cycle Description

The following table lists the Partial Write Cycle Description for CY7C1356C.[2, 3, 4, 9]

Function (CY7C1356C)	$\overline{WE}$	$\overline{BW_b}$	$\overline{BW_a}$
Read	H	x	x
Write – No Bytes Written	L	H	H
Write Byte a – (DQ_a and $DQP_{a)}$	L	H	L
Write Byte b – (DQ_b and $DQP_{b)}$	L	L	H
Write Both Bytes	L	L	L

IEEE 1149.1 Serial Boundary Scan (JTAG)

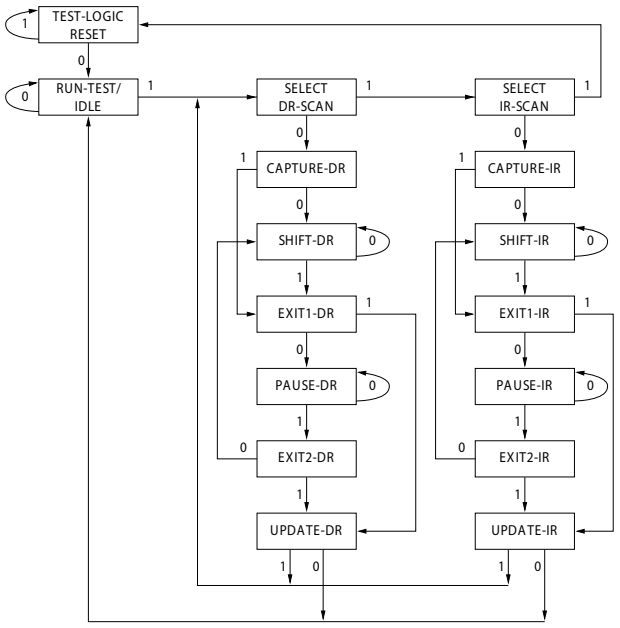
The CY7C1354C/CY7C1356C incorporates a serial boundary scan test access port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This part operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 3.3V or 2.5V I/O logic levels.

The CY7C1354C/CY7C1356C contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO should be left unconnected. Upon power up, the device comes up in a reset state which does not interfere with the operation of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

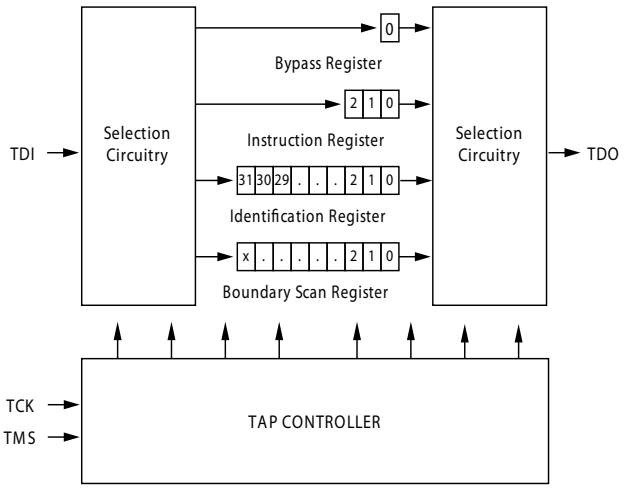
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See the TAP Controller Block Diagram.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See the TAP Controller State Diagram.)

TAP Controller Block Diagram



Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the TAP Controller Block Diagram on page 11. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The tables Boundary Scan Exit Order (256K × 36) on page 16 and Boundary Scan Exit Order (512K × 18) on page 17 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 14.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail in this section.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required - that is, while data captured is shifted out, the preloaded data can be shifted in.

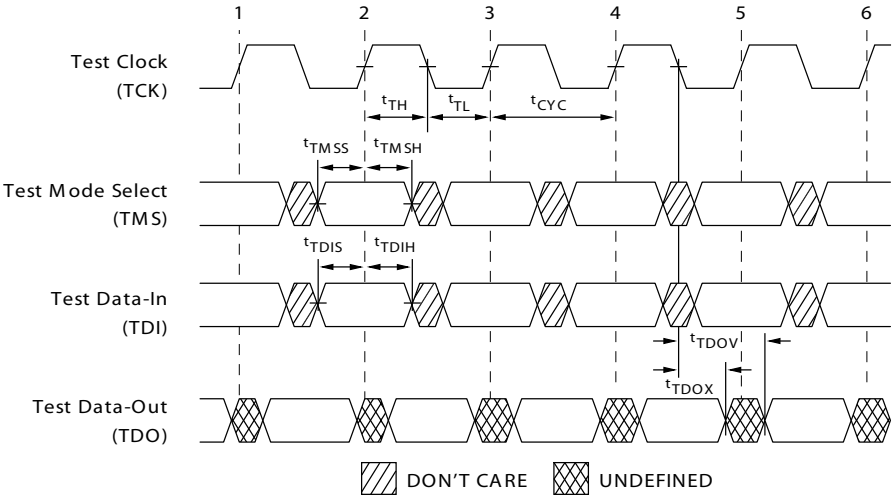
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



TAP AC Switching Characteristics Over the Operating Range[10, 11]

Parameter	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH time	20		ns
t_{TL}	TCK Clock LOW time	20		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

Notes

10. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
11. Test conditions are specified using the load in TAP AC test Conditions. t_R/t_F = 1 ns.

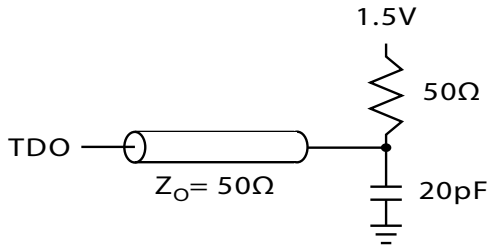
3.3V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 3.3V
Input rise and fall times ..... 1 ns
Input timing reference levels 1.5V
Output reference levels 1.5V
Test load termination supply voltage 1.5V

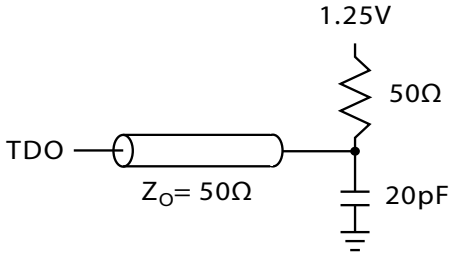
2.5V TAP AC Test Conditions

Input pulse levels ..... V_{SS} to 2.5V
Input rise and fall time ..... 1 ns
Input timing reference levels 1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

3.3V TAP AC Output Load Equivalent



2.5V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

(0°C < TA < +70°C; V_{DD} = 3.3V ±0.165V unless otherwise noted)[12]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –4.0 mA, V_{DDQ} = 3.3V		2.4		V
		I_{OH} = –1.0 mA, V_{DDQ} = 2.5V		2.0		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	V_{DDQ} = 3.3V	2.9		V
			V_{DDQ} = 2.5V	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 8.0 mA	V_{DDQ} = 3.3V		0.4	V
			V_{DDQ} = 2.5V		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA	V_{DDQ} = 3.3V		0.2	V
			V_{DDQ} = 2.5V		0.2	V
V_{IH}	Input HIGH Voltage		V_{DDQ} = 3.3V	2.0	V_{DD} + 0.3	V
			V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		V_{DDQ} = 3.3V	–0.3	0.8	V
			V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_{IN} ≤ V_{DDQ}		–5	5	µA

Identification Register Definitions

Instruction Field	CY7C1354C	CY7C1356C	Description
Revision Number (31:29)	000	000	Reserved for version number.
Cypress Device ID (28:12)[13]	01011001000100110	01011001000010110	Reserved for future use.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	Indicate the presence of an ID register.

Notes
12. All voltages referenced to V_{SS} (GND).
13. Bit #24 is “1” in the Register Definitions for both 2.5V and 3.3V versions of this device.

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (119-ball BGA package)	69	69
Boundary Scan Order (165-ball FBGA package)	69	69

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Exit Order (256K × 36)

Bit #	119-ball ID	165-ball ID	Bit #	119-ball ID	165-ball ID
1	K4	B6	31	B5	R9
2	H4	B7	32	A5	P9
3	M4	A7	33	C6	R8
4	F4	B8	34	A6	P8
5	B4	A8	35	P4	R6
6	G4	A9	36	N4	P6
7	C3	B10	37	R6	R4
8	B3	A10	38	T5	P4
9	D6	C11	39	T3	R3
10	H7	E10	40	R2	P3
11	G6	F10	41	R3	R1
12	E6	G10	42	P2	N1
13	D7	D10	43	P1	L2
14	E7	D11	44	L2	K2
15	F6	E11	45	K1	J2
16	G7	F11	46	N2	M2
17	H6	G11	47	N1	M1
18	T7	H11	48	M2	L1
19	K7	J10	49	L1	K1
20	L6	K10	50	K2	J1
21	N6	L10	51	Not Bonded (Preset to 1)	Not Bonded (Preset to 1)
22	P7	M10	52	H1	G2
23	N7	J11	53	G2	F2
24	M6	K11	54	E2	E2
25	L7	L11	55	D1	D2
26	K6	M11	56	H2	G1
27	P6	N11	57	G1	F1
28	T4	R11	58	F2	E1
29	A3	R10	59	E1	D1
30	C5	P10	60	D2	C1
			61	C2	B2

Boundary Scan Exit Order (512K × 18)

Bit #	119-ball ID	165-ball ID	Bit #	119-ball ID	165-ball ID
1	K4	B6	37	R6	R4
2	H4	B7	38	T5	P4
3	M4	A7	39	T3	R3
4	F4	B8	40	R2	P3
5	B4	A8	41	R3	R1
6	G4	A9	42	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
7	C3	B10	43	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
8	B3	A10	44	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
9	T2	A11	45	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
10	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)	46	P2	N1
11	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)	47	N1	M1
12	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)	48	M2	L1
13	D6	C11	49	L1	K1
14	E7	D11	50	K2	J1
15	F6	E11	51	Not Bonded (Preset to 1)	Not Bonded (Preset to 1)
16	G7	F11	52	H1	G2
17	H6	G11	53	G2	F2
18	T7	H11	54	E2	E2
19	K7	J10	55	D1	D2
20	L6	K10	56	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
21	N6	L10	57	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
22	P7	M10	58	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
23	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)	59	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
24	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)	60	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
25	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)	61	C2	B2
26	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)	62	A2	A2
27	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)	63	E4	A3
28	T6	R11	64	B2	B3
29	A3	R10	65	Not Bonded (Preset to 0)	Not Bonded (Preset to 0)
30	C5	P10	66	G3	Not Bonded (Preset to 0)
31	B5	R9	67	Not Bonded (Preset to 0)	A4
32	A5	P9	68	L5	B5
33	C6	R8	69	B6	A6
34	A6	P8			
35	P4	R6			
36	N4	P6			

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND .....–0.5V to +4.6V

Supply Voltage on V_{DDQ} Relative to GND..... –0.5V to +V_{DD}

DC to Outputs in Tri-State.....–0.5V to V_{DDQ} + 0.5V

DC Input Voltage .....–0.5V to V_{DD} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch up Current..... > 200 mA

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical Single-Bit Upsets	25°C	320	368	FIT/ Mb
LMBU	Logical Multi-Bit Upsets	25°C	0	0.01	FIT/ Mb
SEL	Single Event Latch up	85°C	0	0.1	FIT/ Dev

** No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN 54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V –5%/+10%	2.5V – 5% to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics Over the Operating Range[14, 15]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power Supply Voltage		3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3V I/O	3.135	V_{DD}	V
		for 2.5V I/O	2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3V I/O, I_{OH} = –4.0 mA	2.4		V
		for 2.5V I/O, I_{OH} = –1.0 mA	2.0		V
V_{OL}	Output LOW Voltage	for 3.3V I/O, I_{OL}= 8.0 mA		0.4	V
		for 2.5V I/O, I_{OL}= 1.0 mA		0.4	V
V_{IH}	Input HIGH Voltage	for 3.3V I/O	2.0	V_{DD} + 0.3V	V
		for 2.5V I/O	1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[16]	for 3.3V I/O	–0.3	0.8	V
		for 2.5V I/O	–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA
	Input Current of MODE	Input = V_{SS}	–30		µA
		Input = V_{DD}		5	µA
	Input Current of ZZ	Input = V_{SS}	–5		µA
		Input = V_{DD}		30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled	–5	5	µA

Notes

14. Overshoot: $V_{IH}(AC) < V_{DD} + 1.5V$ (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > -2V$ (Pulse width less than $t_{CYC}/2$).
15. $T_{Power\text{-}up}$: Assumes a linear ramp from 0V to V_{DD} (min.) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
16. Tested initially and after any design or process changes that may affect these parameters.

Electrical Characteristics Over the Operating Range[14, 15] (continued)

Parameter	Description	Test Conditions		Min	Max	Unit
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz		250	mA
			5 ns cycle, 200 MHz		220	mA
			6 ns cycle, 166 MHz		180	mA
I_{SB1}	Automatic CE Power down Current—TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz		130	mA
			5 ns cycle, 200 MHz		120	mA
			6 ns cycle, 166 MHz		110	mA
I_{SB2}	Automatic CE Power down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \leq 0.3V$ or $V_{IN} \geq V_{DDQ} - 0.3V$, f = 0	All speed grades		40	mA
I_{SB3}	Automatic CE Power down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \leq 0.3V$ or $V_{IN} \geq V_{DDQ} - 0.3V$, f = f_{MAX} = $1/t_{CYC}$	4 ns cycle, 250 MHz		120	mA
			5 ns cycle, 200 MHz		110	mA
			6 ns cycle, 166 MHz		100	mA
I_{SB4}	Automatic CE Power down Current—TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	All speed grades		40	mA

Capacitance[16]

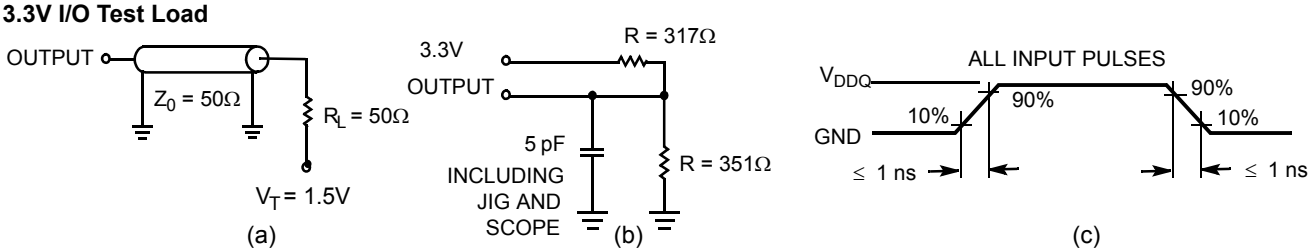
Parameter	Description	Test Conditions	100 TQFP Max	119 BGA Max	165 FBGA Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V V_{DDQ} = 2.5V	5	5	5	pF
C_{CLK}	Clock Input Capacitance		5	5	5	pF
$C_{I/O}$	Input/Output Capacitance		5	7	7	pF

Thermal Resistance[16]

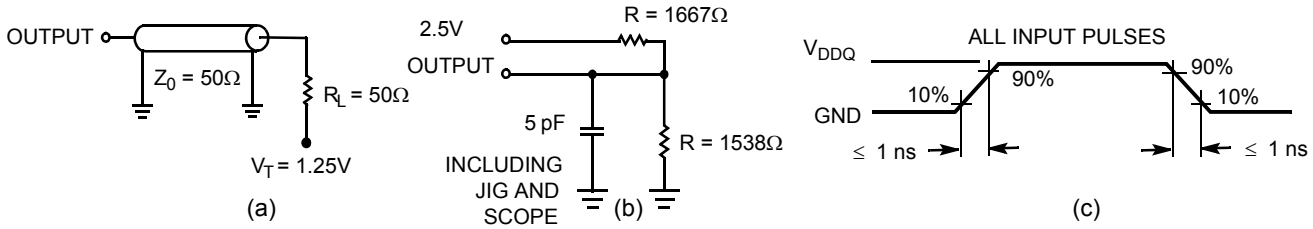
Parameter	Description	Test Conditions	100 TQFP Max	119 BGA Max	165 FBGA Max	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	29.41	34.1	16.8	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		6.13	14.0	3.0	°C/W

Figure 4. AC Test Loads and Waveforms

3.3V I/O Test Load



2.5V I/O Test Load



Switching Characteristics Over the Operating Range [18, 19]

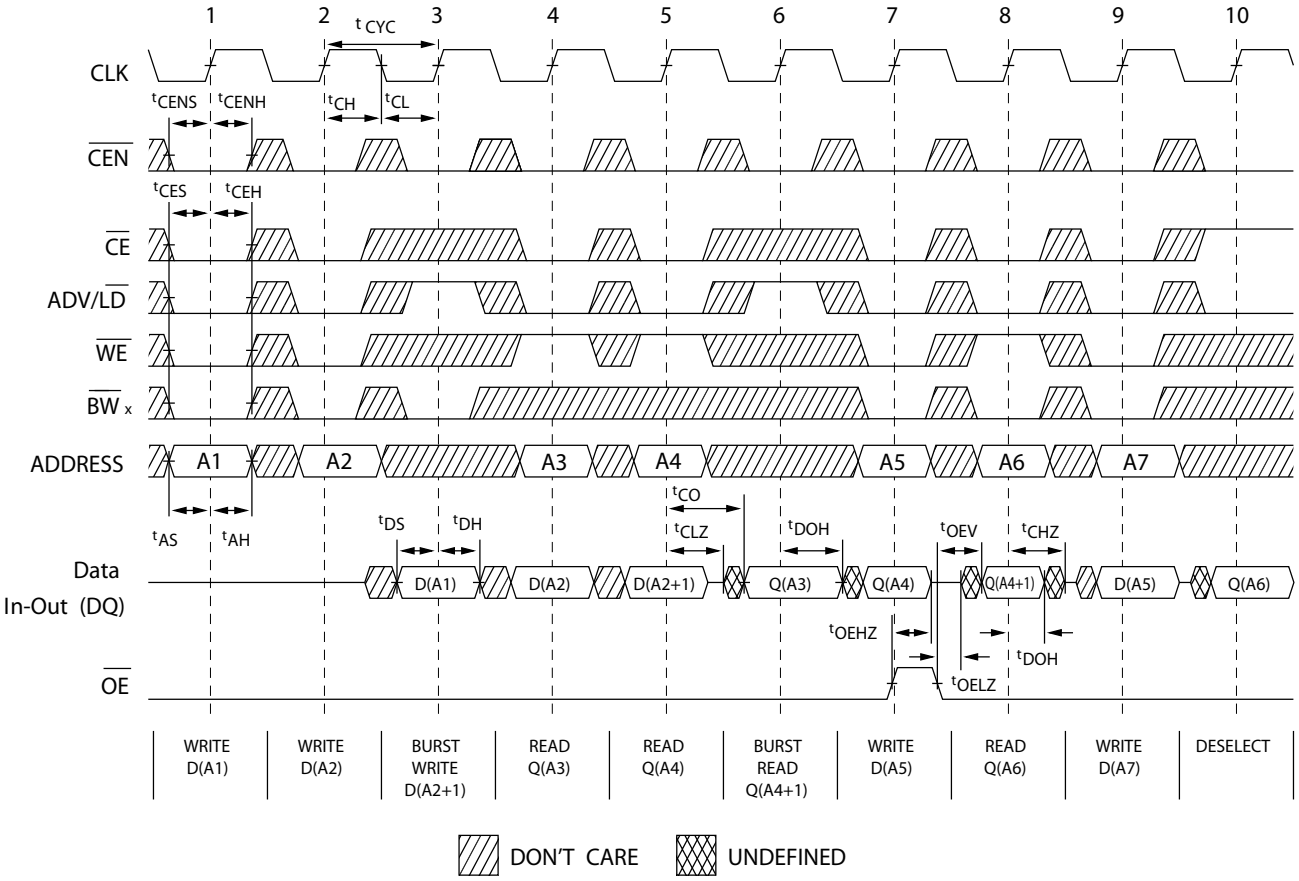
Parameter	Description	–250		–200		–166		Unit
		Min	Max	Min	Max	Min	Max	
t_{Power}[17]	V_{CC} (typical) to the First Access Read or Write	1		1		1		ms
Clock								
t_{CYC}	Clock Cycle Time	4.0		5		6		ns
F_{MAX}	Maximum Operating Frequency		250		200		166	MHz
t_{CH}	Clock HIGH	1.8		2.0		2.4		ns
t_{CL}	Clock LOW	1.8		2.0		2.4		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		2.8		3.2		3.5	ns
t_{CLZ}	Clock to Low-Z[20, 21, 22]	1.25		1.5		1.5		ns
Output Times								
t_{CO}	Data Output Valid after CLK Rise		2.8		3.2		3.5	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		2.8		3.2		3.5	ns
t_{DOH}	Data Output Hold after CLK Rise	1.25		1.5		1.5		ns
t_{CHZ}	Clock to High-Z[20, 21, 22]	1.25	2.8	1.5	3.2	1.5	3.5	ns
t_{CLZ}	Clock to Low-Z[20, 21, 22]	1.25		1.5		1.5		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[20, 21, 22]		2.8		3.2		3.5	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[20, 21, 22]	0		0		0		ns
Setup Times								
t_{AS}	Address Setup before CLK Rise	1.4		1.5		1.5		ns
t_{DS}	Data Input Setup before CLK Rise	1.4		1.5		1.5		ns
t_{CENS}	$\overline{CEN}$ Setup before CLK Rise	1.4		1.5		1.5		ns
t_{WES}	$\overline{WE}$, $\overline{BW_x}$ Setup before CLK Rise	1.4		1.5		1.5		ns
t_{ALS}	ADV/$\overline{LD}$ Setup before CLK Rise	1.4		1.5		1.5		ns
t_{CES}	Chip Select Setup	1.4		1.5		1.5		ns
Hold Times								
t_{AH}	Address Hold after CLK Rise	0.4		0.5		0.5		ns
t_{DH}	Data Input Hold after CLK Rise	0.4		0.5		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold after CLK Rise	0.4		0.5		0.5		ns
t_{WEH}	$\overline{WE}$, $\overline{BW_x}$ Hold after CLK Rise	0.4		0.5		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.4		0.5		0.5		ns
t_{CEH}	Chip Select Hold after CLK Rise	0.4		0.5		0.5		ns

Notes

17. This part has a voltage regulator internally; t_{power} is the time power needs to be supplied above V_{DD} minimum initially, before a Read or Write operation can be initiated.
18. Timing reference level is 1.5V when V_{DDQ} = 3.3V and is 1.25V when V_{DDQ} = 2.5V.
19. Test conditions shown in (a) of AC Test Loads unless otherwise noted.
20. t_{CHZ}, t_{CLZ}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
21. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
22. This parameter is sampled and not 100% tested.

Switching Waveforms

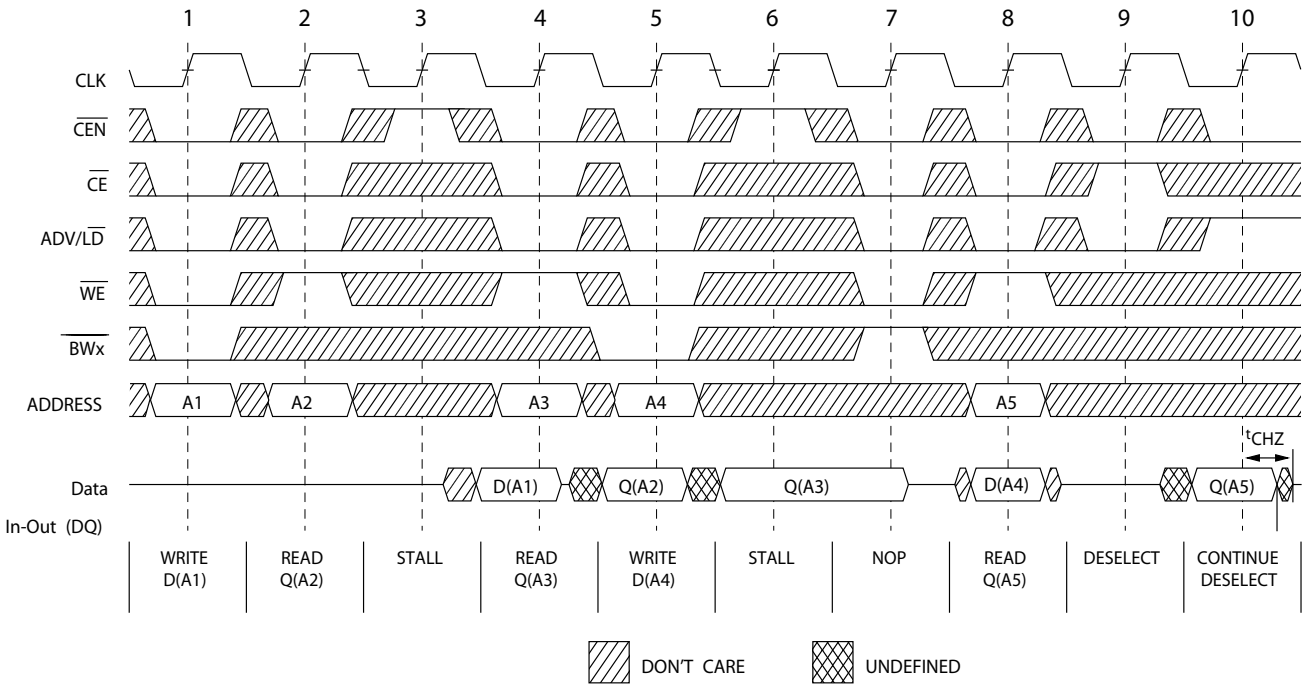
Figure 5. Read/Write Timing[23, 24, 25]



Notes
23. For this waveform ZZ is tied low.
24. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
25. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

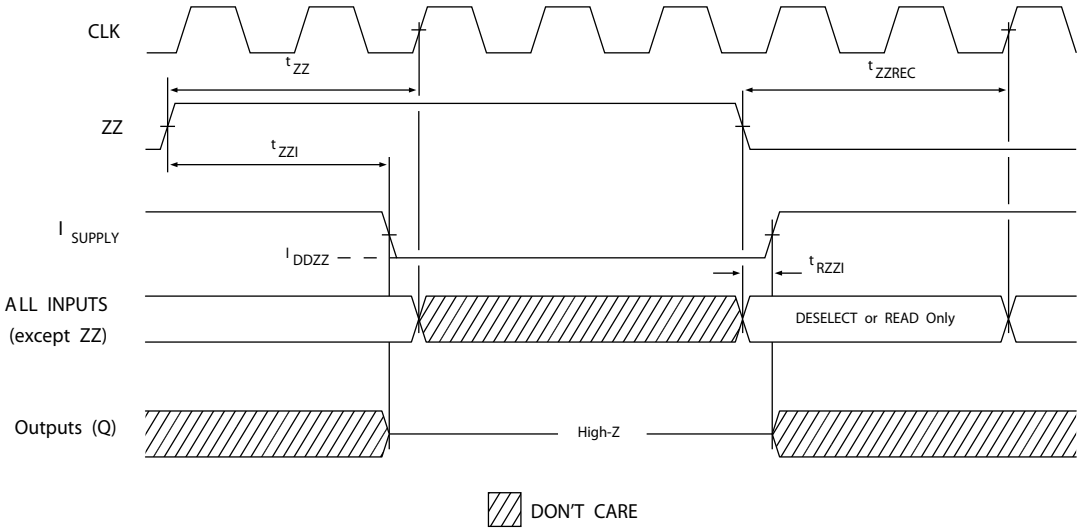
Figure 6. NOP, STALL, and DESELECT Cycles[23, 24, 26]



Note
26. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated CEN being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

Figure 7. ZZ Mode Timing[27, 28]



Notes
27. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
28. I/Os are in High-Z when exiting ZZ sleep mode.

Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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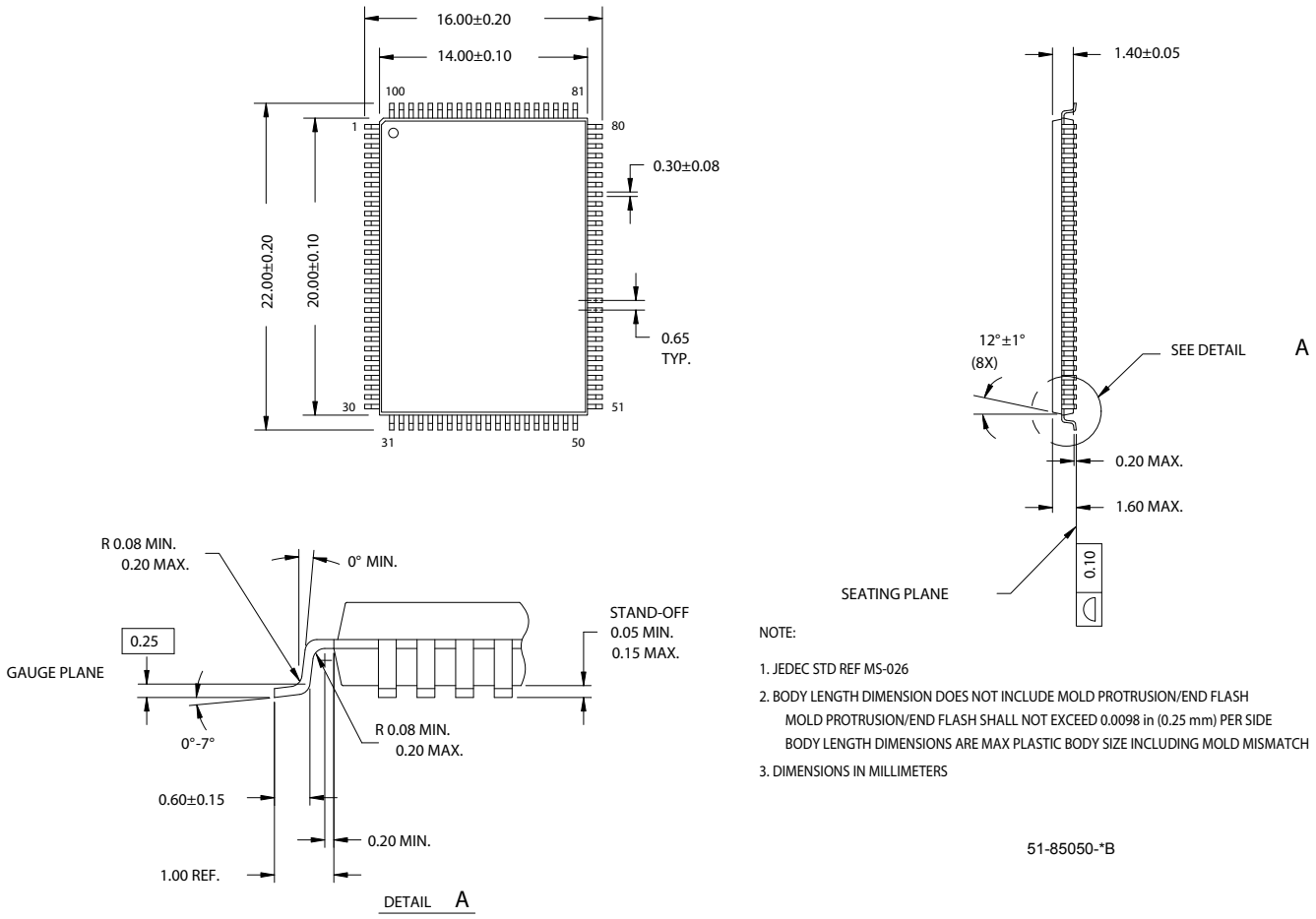
Table 4. Ordering Information

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
166	CY7C1354C-166AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1356C-166AXC			
	CY7C1354C-166BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1356C-166BGC			
	CY7C1354C-166BZC	51-85180	165-ball Fine-Pitch Ball Grid Array (13 x 15 x 1.4 mm)	
	CY7C1354C-166AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1356C-166AXI			
200	CY7C1354C-200AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1354C-200BGC	51-85115	119-ball Ball Grid Array (14 x 22 x 2.4 mm)	
	CY7C1354C-200AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
250	CY7C1356C-250AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial

Package Diagrams

Figure 8. 100-Pin Thin Plastic Quad Flatpack (14X20X1.4 mm)



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050-*B

Figure 9. 119-Ball BGA (14X22X2.4 mm)

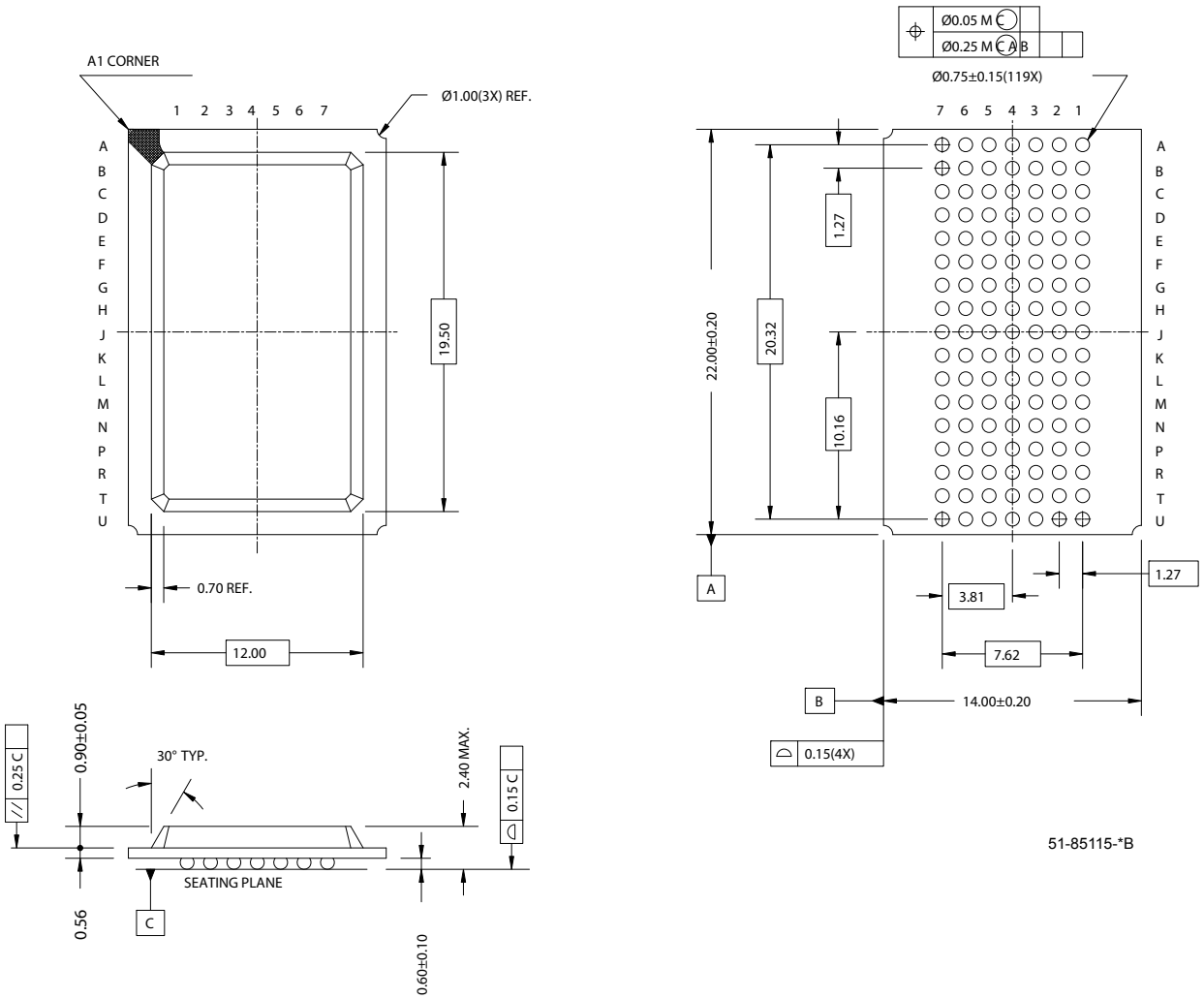
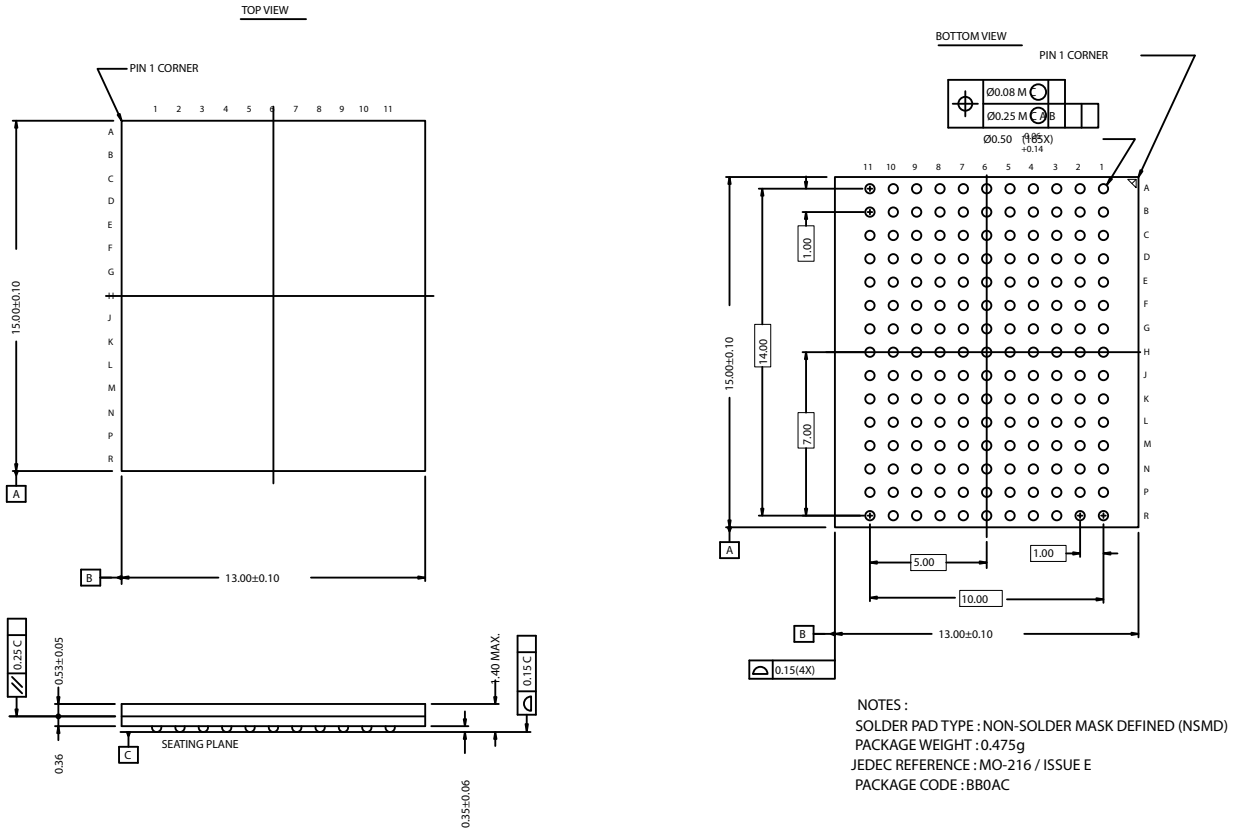


Figure 10. 165-Ball FBGA (13X15X1.4 mm)



Document History Page

Document Title: CY7C1354C/CY7C1356C 9-Mbit (256K x 36/512K x 18) Pipelined SRAM with NoBL™ Architecture Document Number: 38-05538				
REV.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	242032	See ECN	RKF	New data sheet
*A	278130	See ECN	RKF	Changed Boundary Scan order to match the B Rev of these devices Changed TQFP pkg to Lead-free TQFP in Ordering Information section Added comment of Lead-free BG and BZ packages availability
*B	284431	See ECN	VBL	Changed ISB1 and ISB3 from DC Characteristic table as follows ISB1: 225 mA-> 130 mA, 200 MHz -> 120 mA, 167 MHz -> 110 mA ISB3: 225 MHz -> 120 mA, 200 MHz -> 110 mA, 167 MHz -> 100 mA Add BG and BZ pkg lead-free part numbers to ordering info section
*C	320834	See ECN	PCI	Changed 225 MHz to 250 MHz Address expansion pins/balls in the pinouts for all packages are modified as per JEDEC standard Unshaded frequencies of 250, 200, 166 MHz in AC/DC Tables and Selection Guide Changed Θ_{JA} and Θ_{JC} for TQFP Package from 25 and 9 °C/W to 29.41 and 6.13 °C/W respectively Changed Θ_{JA} and Θ_{JC} for BGA Package from 25 and 6 °C/W to 34.1 and 14.0 °C/W respectively Changed Θ_{JA} and Θ_{JC} for FBGA Package from 27 and 6 °C/W to 16.8 and 3.0 °C/W respectively Modified V_{OL}, V_{OH} test conditions Added Lead-Free product information Updated Ordering Information Table Changed from Preliminary to Final
*D	351895	See ECN	PCI	Changed I_{SB2} from 35 to 40 mA Updated Ordering Information Table
*E	377095	See ECN	PCI	Modified test condition in note# 15 from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$
*F	408298	See ECN	RXU	Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Changed three-state to tri-state. Modified “Input Load” to “Input Leakage Current except ZZ and MODE” in the Electrical Characteristics Table. Replaced Package Name column with Package Diagram in the Ordering Information table.
*G	501793	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND Changed t_{TH}, t_{TL} from 25 ns to 20 ns and t_{TDOV} from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.
*H	2756340	08/26/2009	VKN/AESA	Updated template Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information.

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