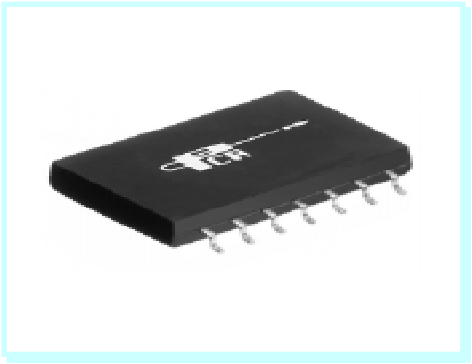
PCA ELECTRONICS INC.

10/100 LAN Interface Module for PC Card Applications

EPF8074G



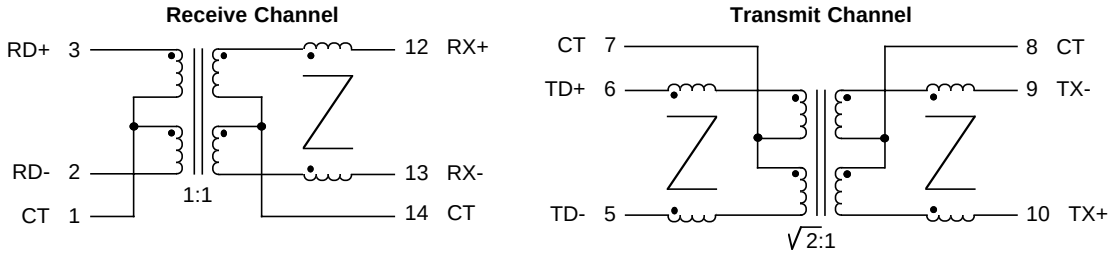
- Optimized for QSI6611/6612 PHY/MAC
- Guaranteed to operate with 8 mA DC bias at 70°C on cable side
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards

Electrical Parameters @ 25° C

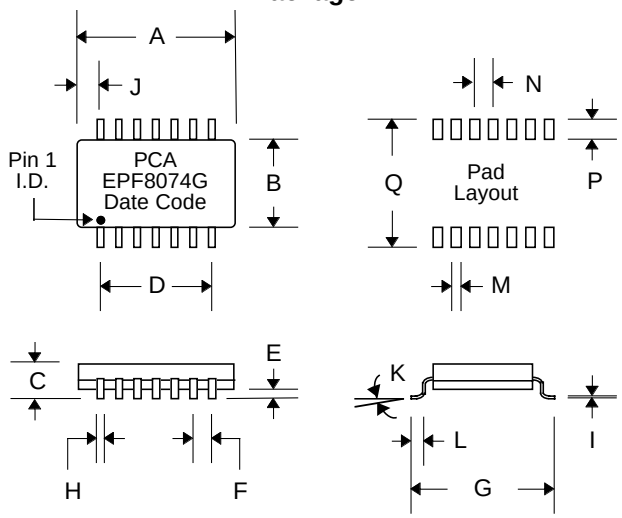
OCL @ 70°C	**Insertion Loss** (dB Max.)						**Return Loss** (dB Min.)						**Common Mode Rejection** (dB Min.)						**Crosstalk** (dB Min.) [Between Channels]	
100 KHz, 0.1 Vrms 8 mA DC Bias	1-80 MHz		100 MHz		150 MHz		1-30 MHz		60 MHz		100 MHz		30-100 MHz		200 MHz		500 MHz		5-10 MHz	10-100 MHz
Cable Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv		
350µH	-1	-1	-2	-2	-3.5	-3	-18	-18	-12	-12	-10	-10	-38	-38	-30	-25	-20	-15	-40	-40

- **Isolation** : 1500 Vrms
- Cable **Impedance** : 100 Ω
- **Rise Time** : 3.0 nS Max.

Schematic



Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	.790	.810		20.06	20.57	
B	.510	.530		12.95	13.46	
C	.074	.084		1.88	2.13	
D	.600	Typ.		15.24	Typ.	
E	.003	.020		0.076	.508	
F	.100	Typ.		2.54	Typ.	
G	.660	.680		16.76	17.27	
H	.016	.022		.406	.559	
I	.008	.012		.203	.305	
J	.090	Typ.		2.28	Typ.	
K	0°	8°		0°	8°	
L	.025	.045		.635	1.14	
M			.040			1.02
N			.100			2.54
P			.085			2.16
Q			.700			17.78

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CSF8074Ga Rev. 8/6/97

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EPF8074G

The circuit below is a guideline for interconnecting PCA's EPF8074G with QSI6611 and QSI6612 chip set for 10/100 Mb/s applications. Further details can be obtained from the chip manufacturer application notes.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 10/100 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the chip's supporting resistor to get at least 2.12V pk-pk across the transmit pins.

It is recommended that system designers do not use the receiver side center tap to ground, via a capacitor. This may worsen EMI, specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

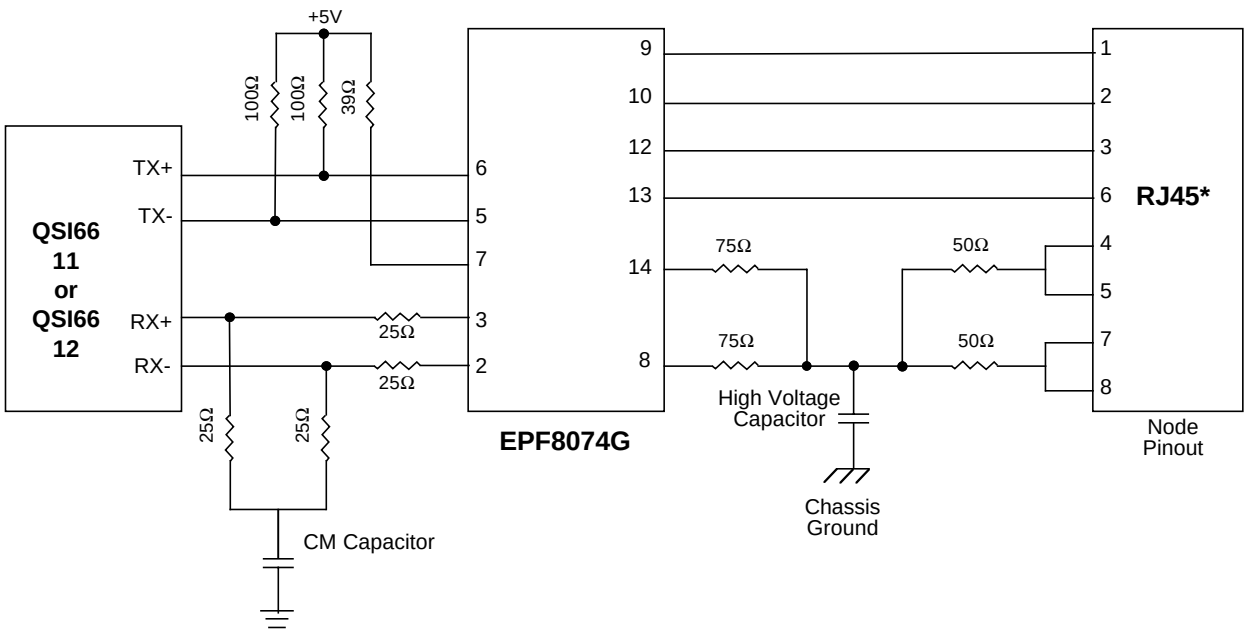
The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75 Ω shown from the center taps of the secondary may be taken to chassis ground via a cap of suitable value. This depends upon user's design, EMI margin etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8074G. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50 Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP



Notes : * NIC Side is shown. Hub side connection will have crossover swapping pins 3-6 & 1-2.

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