



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV5807MX — Step-down Switching Regulator

Overview

LV5807MX is a 1ch step-down switching regulator. 0.12Ω FET is incorporated on the upper side to achieve high-efficiency operation for large output current. Low-heat resistance and compact-package MFP8 (200mil) employed. Current mode control type, with superior load current response and easy phase compensation ON/OFF pin, allowing the standby mode with the current drain of 40μA or less Pulse-by-pulse over-current protection and overheat protection available for protection of load devices Soft start pin to be provided with a capacitance for soft start.

Functions

- 3A 1ch step-down switching regulator
- Wide input dynamic range (8 to 18V)
- High efficiency (90% $I_{OUT} = 1A$, $V_{IN} = 12V$, $V_O = 5V$)
- Standby mode
- Over-current protection
- Thermal shutdown
- Reference voltage: 0.79V
- Fixed frequency: 385kHz
- Soft start
- Compact package: MFP8 (200mil) with Exposed Pad

Specifications

Maximum Ratings at $T_a = 25^\circ C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input V_{IN} voltage	V_{IN} max		20	V
BOOT pin maximum voltage	V_{BT} max		25	V
SW pin maximum voltage	V_{SW} max		V_{IN} max	V
BOOT pin-SW pin maximum voltage	V_{BS-SW} max		7	V
EN pin maximum voltage	V_{EN} max		20	V
FB, COMP, SS pin maximum voltage	V_{fs} max		7	V
Allowable power dissipation	P_d max	Mount on a specified board *	2.05	W
Junction temperature	T_j max		150	°C
Operating temperature	T_{opr}		-20 to 80	°C
Storage temperature	T_{stg}		-40 to 150	°C

* Specified board: 46.4mm × 31.8mm × 1.7mm, glass epoxy both side.

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

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LV5807MX

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
V_{IN} pin voltage	V_{IN}		8 to 18	V
BOOT pin voltage	V_{BT}		-0.3 to 23	V
SW pin voltage	V_{SW}		-0.4 to V_{IN}	V
BOOT pin-SW pin maximum voltage	V_{BS-SW}		6.5	V
EN pin maximum voltage	V_{EN}		18	V
FB, COMP, SS pin voltage	V_{FSO}		6	V

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
IC current drain at standby	I_{CC1}	$EN=0\text{V}$		40		μA
IC current drain in operation	I_{CC2}	$EN=5\text{V}$, $FB=1\text{V}$		3		mA
Efficiency	Effcy	$V_{IN}=12\text{V}$, $I_{OUT}=1\text{A}$, $V_o=5\text{V}$, Design target *1		90		%
Reference voltage	V_{ref}	$V_{IN}=8\text{V}$ to 18V ($\pm 2\%$)	0.7742	0.79	0.8058	V
FB pin bias current	I_{ref}	$FB=0.79\text{V}$ application		10	100	nA
High-side ON resistance	R_{onH}	$BOOT=5\text{V}$, $I_{OUT}=1\text{A}$		0.12		Ω
Low-side ON resistance	R_{onL}			5		Ω
Oscillation frequency	f_{OSC}		310	385	460	kHz
Oscillation frequency during short-circuit protection	f_{OSCS}		29	38	47	kHz
EN high-threshold voltage	V_{enh}		1.05	1.57	2.1	V
EN low-threshold voltage	V_{enl}		0.8	1.23	1.65	V
Maximum ON DUTY	D_{max}			80		%
Current limit peak value	I_{cl1}	SW pin output current, $V_{IN}=12\text{V}$, $V_{OUT}=5\text{V}$, $L=10\mu\text{H}$	3.8	5		A
Thermal shutdown temperature	T_{tsd}	*Design guarantee *2		160		$^\circ\text{C}$
Thermal shutdown temperature hysteresis	D_{tsd}	*Design guarantee *2		40		$^\circ\text{C}$
Soft start current	I_{SS}	$SS=0\text{V}$	6	10	14	μA

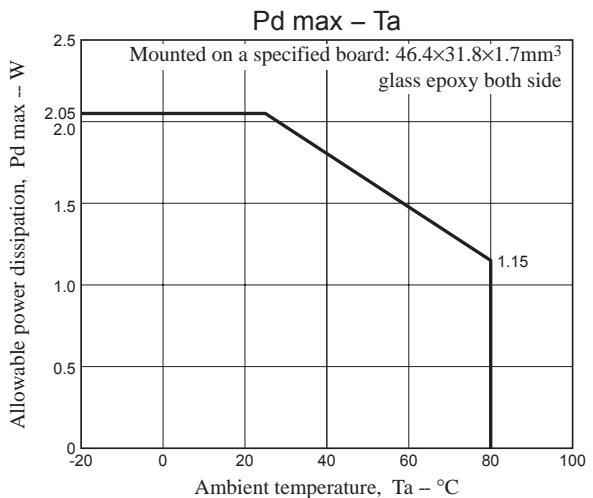
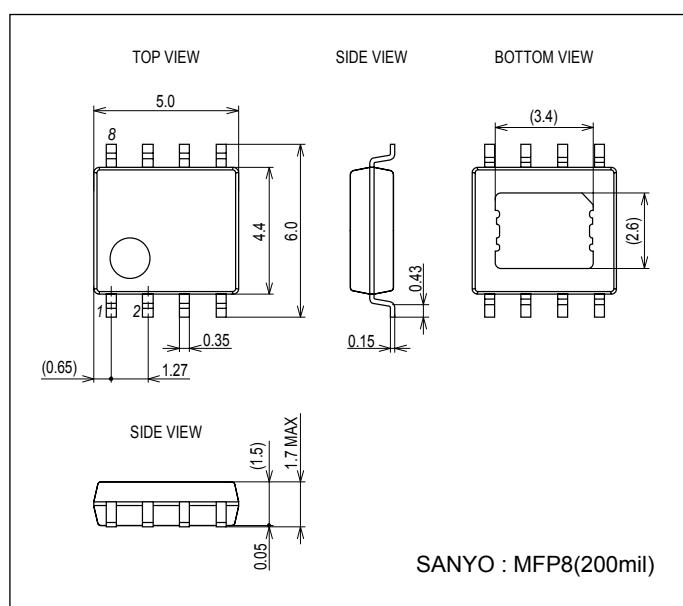
*1: Reference value (not tested before shipment)

*2: Design guarantee (value guaranteed by design and not tested before shipment)

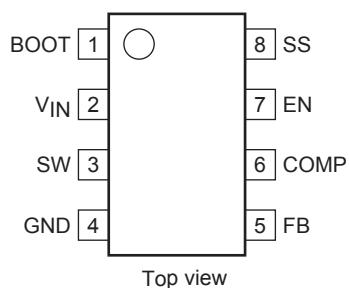
Package Dimensions

unit : mm (typ)

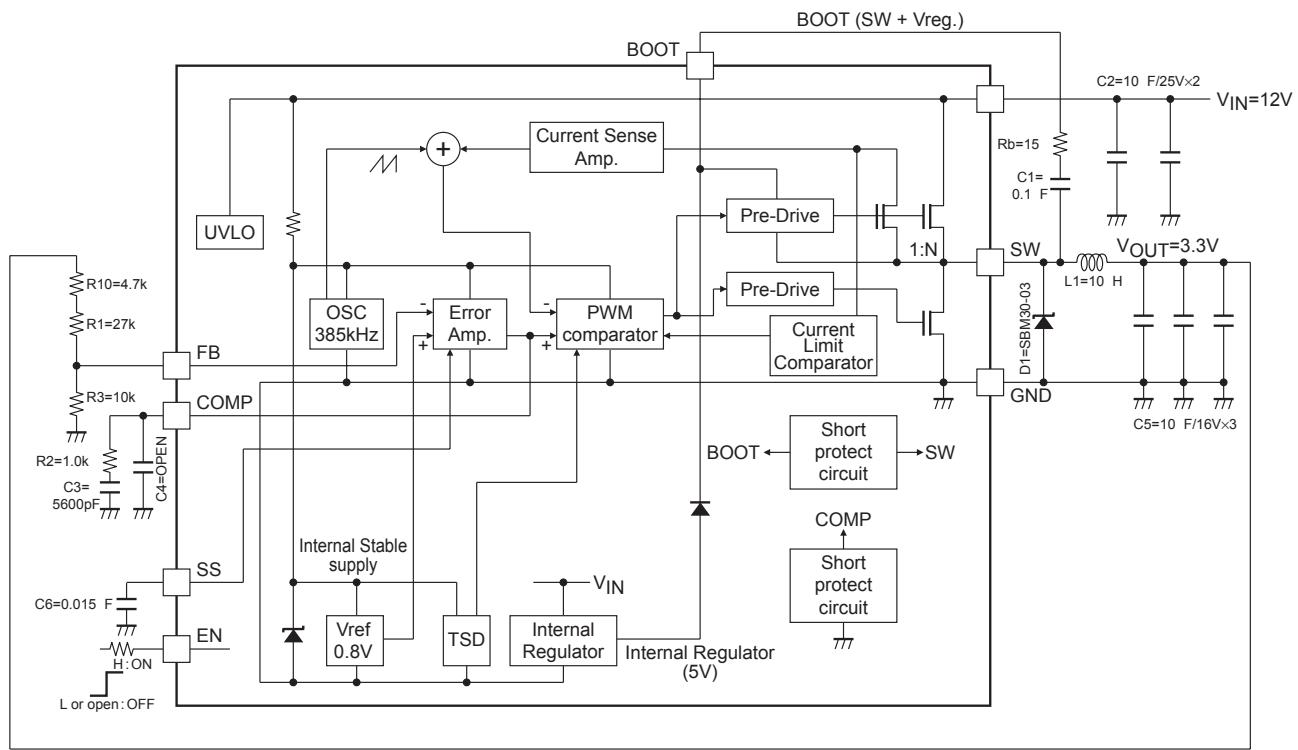
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Pin Assignment

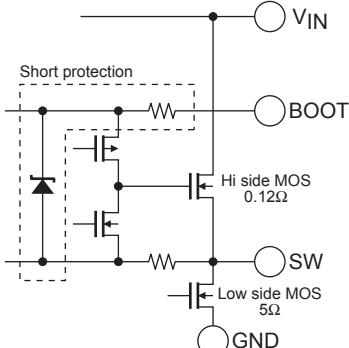
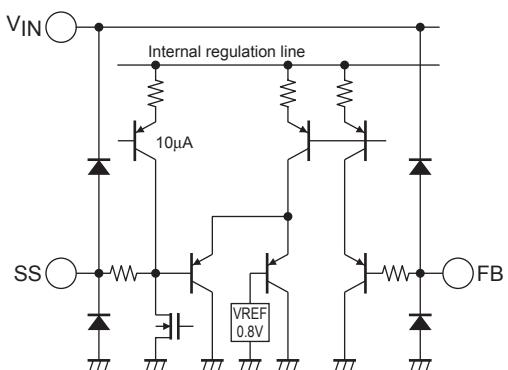
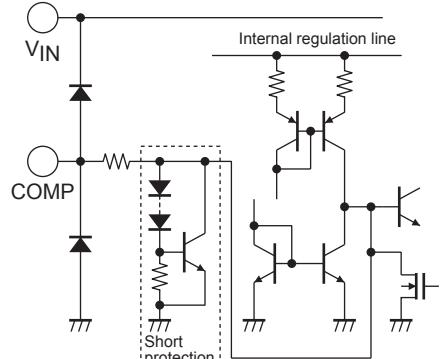
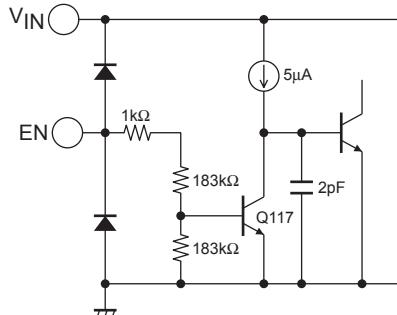


Block Diagram and Sample Application Circuit (3.3V output)



*C1,C2,C5 = Ceramic capacitor
*L1 = CDRH105RNP-100NC (sumida)

Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	BOOT	Upper MOS transistor boot strap capacitance connection pin. Connect the boot capacitance of about $0.1\mu\text{F}$ between SW pins. To protect the SW pin's absolute maximum rating, to ensure stable operation, and to eliminate noise, the boot capacitance serial resistance (about 15Ω) R_b proves effective.	
2	V _{IN}	Input voltage pin. Connect substantially large ($10\mu\text{F}$ 2 parallel or more) capacitance between this pin and GND.	
3	SW	Power switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin.	
4	GND	Ground pin.	
5	FB	Feedback pin. Sets the output voltage by means of split resistor in the section of the output voltage $V_{\text{OUT}} - \text{FB} - \text{GND}$. V_{OUT} setting is made as calculated below: $V_{\text{OUT}} = V_{\text{ref}} \times \left\{ 1 + \frac{(R_1 + R_{10})}{R_3} \right\}$ $V_{\text{ref}} = 0.79\text{V}$ Example: 3.3V output voltage (See Block Diagram and Sample Application Circuit) $V_{\text{OUT}} = 0.79 \times \left\{ 1 + \frac{(27\text{k} + 4.7\text{k})}{10\text{k}} \right\}$ $=3.294\text{V}$	
8	SS	Soft start pin. Sets the soft start time by means of the built-in $10\mu\text{A}$ source voltage and external soft start capacity. The soft start capacity C_6 can be set as follows: $C_6 = 10\mu\text{A} \times \frac{T_{\text{ss}}}{V_{\text{ref}}}$ Where, T_{ss} is the soft start time and V_{ref} is the reference voltage. Example: 1.2ms soft start time achieved $C_6 = 10\mu\text{A} \times \frac{1.2\text{ms}}{0.79\text{ V}} = 0.015\mu\text{F}$	
6	COMP	Phase compensation pin. Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	
7	EN	Enable pin. Converter enabled when set to the HIGH voltage and disabled when LOW voltage or OPEN state.	

Considerations for the design

Insertion of serial beads in the Schottky diode for removal of noise may cause generation of the negative voltage deviating from the absolute maximum rating at the SW pin, resulting in failure of normal operation. In such an event, do not insert beads as above described and, instead, remove noise by means of the BOOT resistance R_b.

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