



W24129A

16K × 8 HIGH SPEED CMOS STATIC RAM

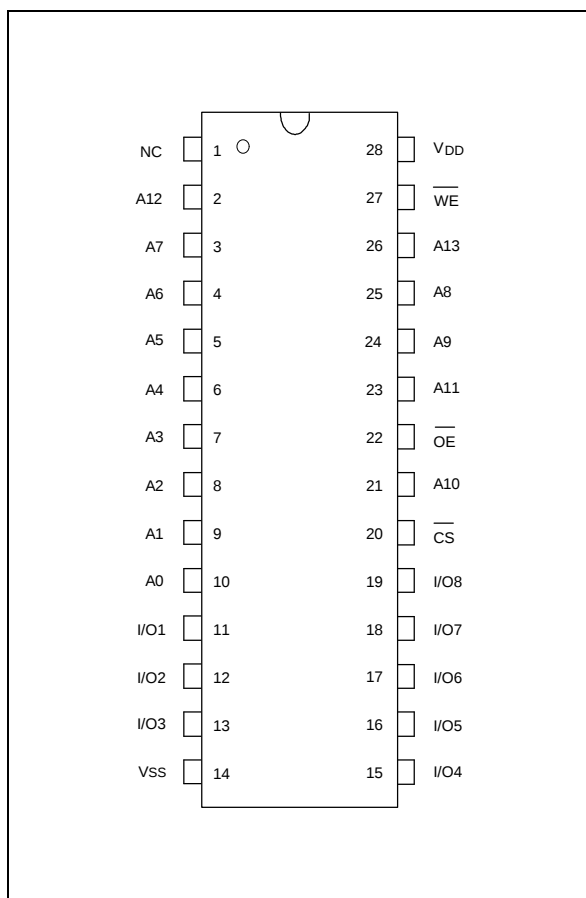
GENERAL DESCRIPTION

The W24129A is a high speed, low power CMOS static RAM organized as 16384 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

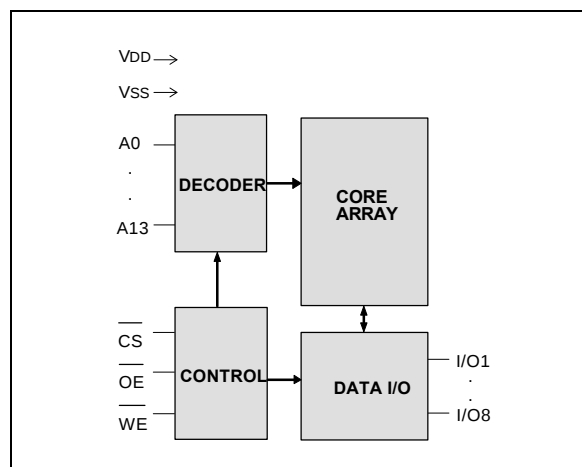
FEATURES

- High speed access time: 35 nS (max.)
- Low power consumption:
 - Active: 600 mW (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 28-pin 600 mil DIP and 330 mil SOP

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A13	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1–I/O8	V _{DD} CURRENT
H	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
L	H	H	Output Disable	High Z	I _{DD}
L	L	H	Read	Data Out	I _{DD}
L	X	L	Write	Data In	I _{DD}

DC CHARACTERISTICS**Absolute Maximum Ratings**

PARAMETER	RATING	UNIT
Supply Voltage to V _{SS} Potential	-0.5 to +7.0	V
Input/Output to V _{SS} Potential	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V
Input High Voltage	V _{IH}	-	+2.2	-	V _{DD} +0.5	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , $\overline{CS}$ = V _{IH} (min.) or $\overline{OE}$ = V _{IH} (min.) or $\overline{WE}$ = V _{IL} (max.)	-10	-	+10	μA
Output Low Voltage	V _{OL}	I _{OL} = +8.0 mA	-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA	2.4	-	-	V
Operating Power Supply Current	I _{DD}	$\overline{CS}$ = V _{IL} (max.), I/O = 0 mA Cycle = min., Duty = 100%	-	-	120	mA
Standby Power Supply Current	I _{SB}	$\overline{CS}$ = (min.) Cycle = min., Duty = 100%	-	-	30	mA
	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	-	5	mA

Note: Typical characteristics are at V_{DD} = 5V, T_A = 25° C.



CAPACITANCE

($V_{DD} = 5V$, $T_A = 25^\circ C$, $f = 1\text{ MHz}$)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	$V_{IN} = 0V$	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0V$	10	pF

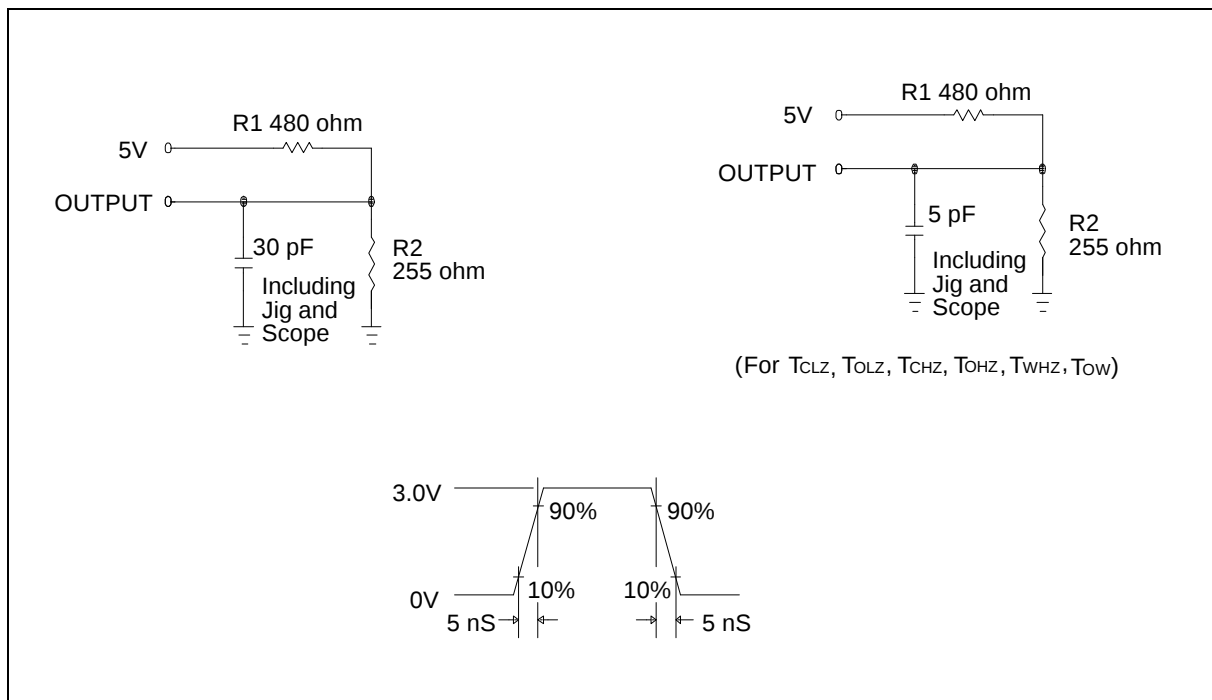
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	$C_L = 30\text{ pF}$, $I_{OH}/I_{OL} = -4\text{ mA}/8\text{ mA}$

AC Test Loads and Waveform





AC Characteristics, continued
(V_{DD} = 5V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER	SYM.	W24129A-35		UNIT
		MIN.	MAX.	
Read Cycle Time	T _{RC}	35	-	nS
Address Access Time	T _{AA}	-	35	nS
Chip Select Access Time	T _{ACS}	-	35	nS
Output Enable to Output Valid	T _{AOE}	-	17	nS
Chip Selection to Output in Low Z	T _{CLZ} *	3	-	nS
Output Enable to Output in Low Z	T _{OLZ} *	0	-	nS
Chip Deselection to Output in High Z	T _{CHZ} *	-	17	nS
Output Disable to Output in High Z	T _{OHZ} *	-	17	nS
Output Hold from Address Change	T _{OH}	3	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

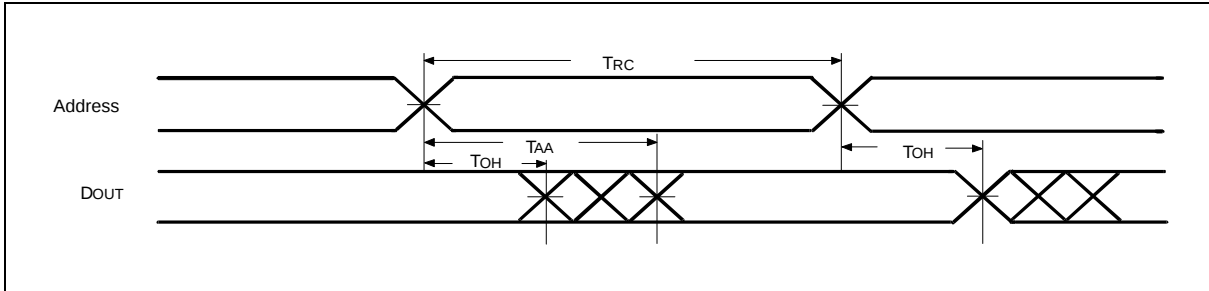
PARAMETER		SYM.	W24129A-35		UNIT
			MIN.	MAX.	
Write Cycle Time		T _{WC}	35	-	nS
Chip Selection to End of Write		T _{CW}	20	-	nS
Address Valid to End of Write		T _{AW}	20	-	nS
Address Setup Time		T _{AS}	0	-	nS
Write Pulse Width		T _{WP}	18	-	nS
Write Recovery Time	CS, WE	T _{WR}	0	-	nS
Data Valid to End of Write		T _{DW}	15	-	nS
Data Hold from End of Write		T _{DH}	0	-	nS
Write to Output in High Z		T _{WHZ} *	-	15	nS
Output Disable to Output in High Z		T _{OHZ} *	-	15	nS
Output Active from End of Write		T _{OW}	0	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

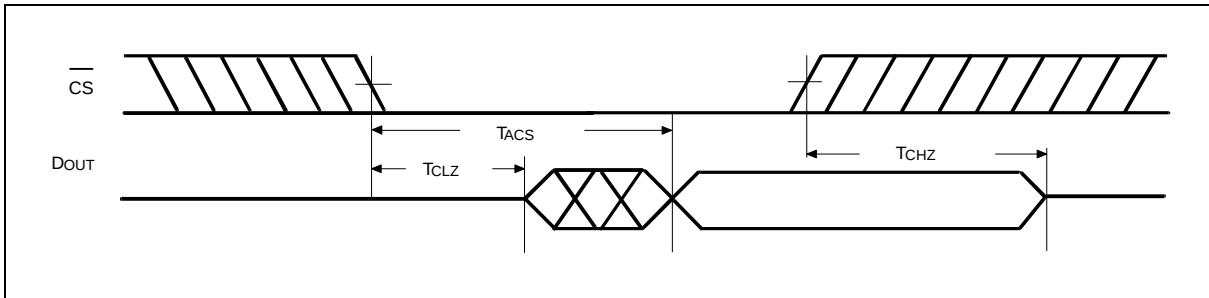
Read Cycle 1

(Address Controlled)



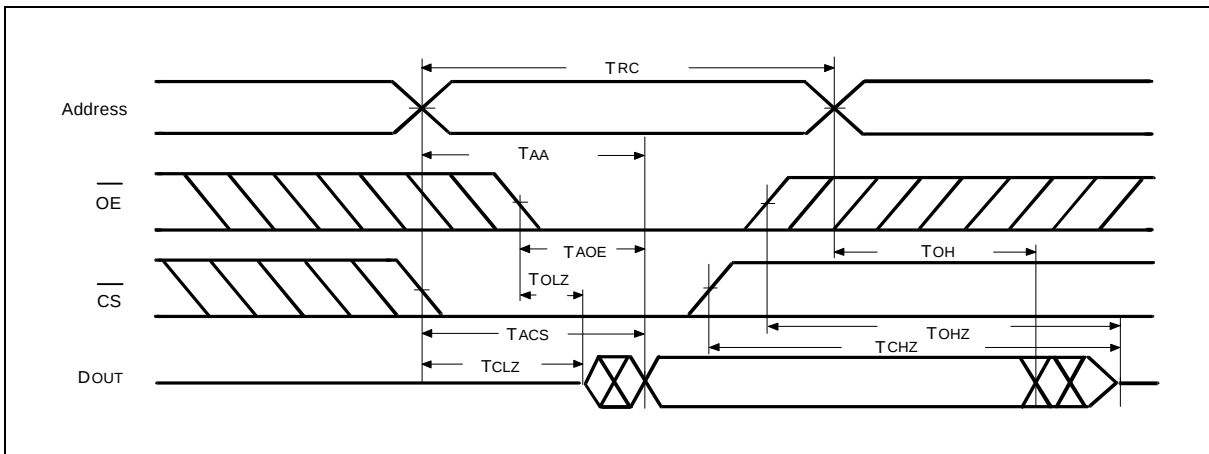
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

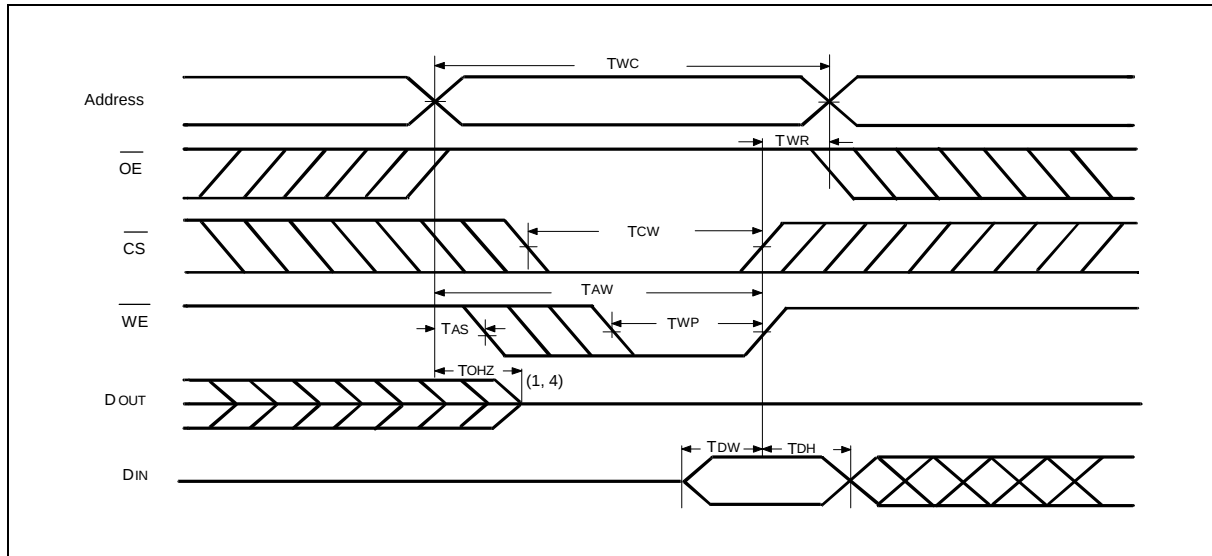
(Output Enable Controlled)



Timing Waveforms, continued

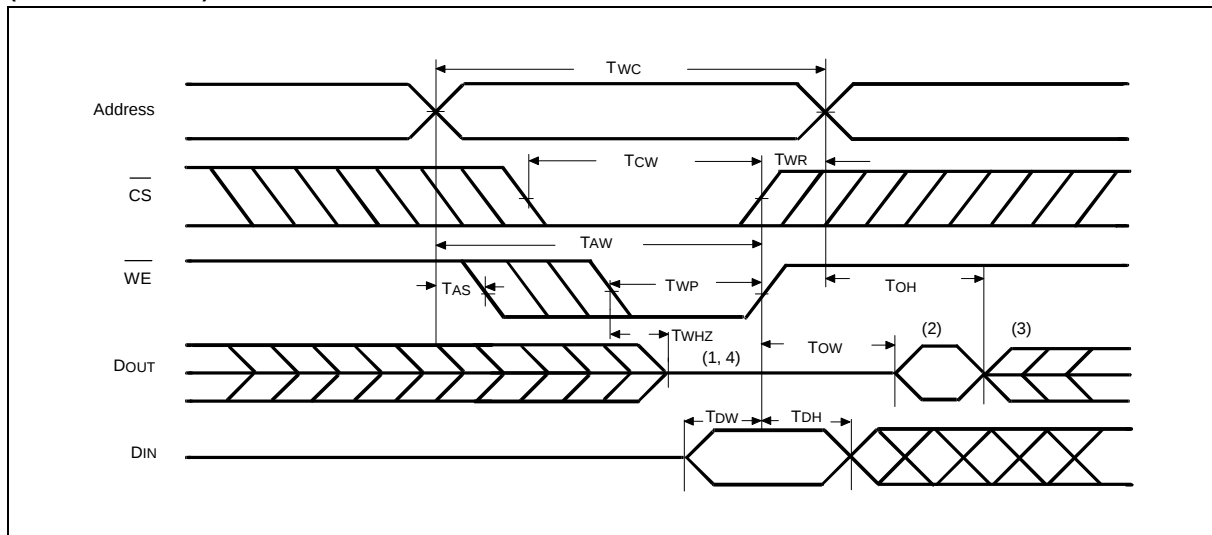
Write Cycle 1

($\overline{\text{OE}}$ Clock)



Write Cycle 2

($\overline{\text{OE}} = \text{VIL Fixed}$)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.



ORDERING INFORMATION

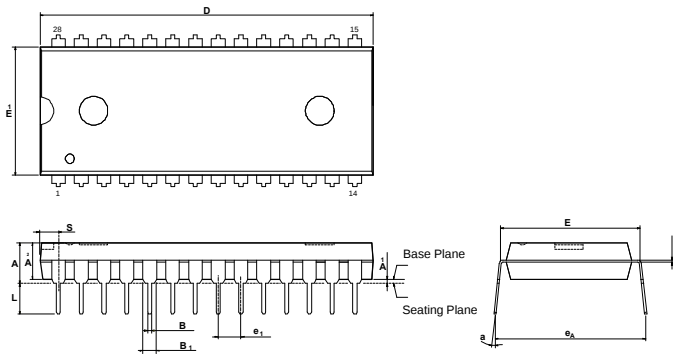
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24129A-35	35	120	5	600 mil DIP
W24129AS-35	35	120	5	330 mil SOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

28-pin P-DIP

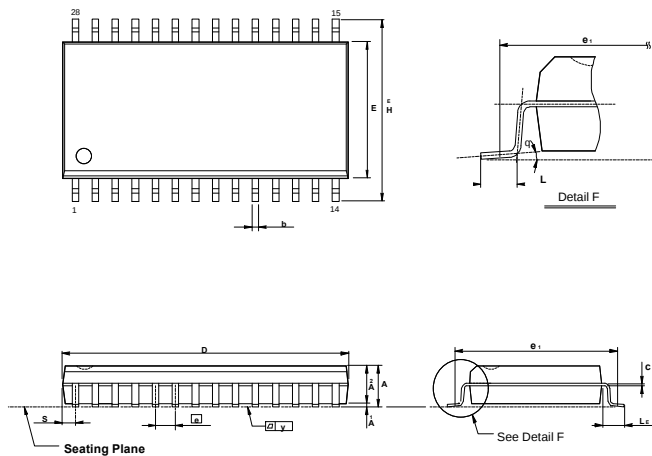


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A ₁	0.010	—	—	0.25	—	—
A ₂	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B ₁	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.460	1.470	—	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E ₁	0.540	0.545	0.550	13.72	13.84	13.97
e ₁	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e _A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

28-pin SO Wide Body



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.112	—	—	2.85
A ₁	0.004	—	—	0.10	—	—
A ₂	0.093	0.098	0.103	2.36	2.49	2.62
b	0.014	0.016	0.020	0.36	0.41	0.51
C	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.713	0.733	—	18.11	18.62
E	0.326	0.331	0.336	8.28	8.41	8.53
E ₁	0.044	0.050	0.056	1.12	1.27	1.42
H _e	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L _E	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
Q	0°	—	10°	0°	—	10°

Notes:

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.

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Note: All data and specifications are subject to change without notice.