

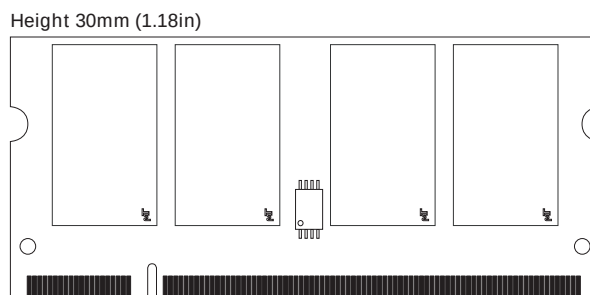
# DDR2 SDRAM SODIMM

**MT8HTF3264H(I) – 256MB**
**MT8HTF6464H(I) – 512MB**
**MT8HTF12864H(I) – 1GB**

For component data sheets, refer to Micron's Web site: [www.micron.com/products/dram/ddr2](http://www.micron.com/products/dram/ddr2)

## Features

- 200-pin, small outline, dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 256MB (32 Meg x 64), 512MB (64 Meg x 64), 1GB (128 Meg x 64)
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$  to  $+3.6V$
- JEDEC standard 1.8V I/O (SSTL\_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1  $t_{CK}$
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Single rank

**Figure 1: 200-pin SODIMM (MO-224 R/C "B")**


## Options

- Operating temperature
- Commercial ( $0^{\circ}C \leq T_C \leq +85^{\circ}C$ )
- Industrial ( $-40^{\circ}C \leq T_C \leq +95^{\circ}C$ )<sup>1,2</sup>
- Package
  - 200-pin SODIMM (Pb-free)
- Frequency/CAS latency<sup>3</sup>
  - 2.5ns @ CL = 5 (DDR2-800)<sup>4</sup>
  - 2.5ns @ CL = 6 (DDR2-800)<sup>4</sup>
  - 3ns @ CL = 5 (DDR2-667)
  - 3.75ns @ CL = 4 (DDR2-533)
  - 5.0ns @ CL = 3 (DDR2-400)
- PCB Height
  - 30mm (1.18in)

## Marking

I  
Y  
-80E  
-800  
-667  
-53E  
-40E

- Notes: 1. Industrial temperatures apply to DRAM only.  
 2. Contact Micron for product availability.  
 3. CL = CAS (READ) latency  
 4. Not available in 256MB density

**Table 1: Key Timing Parameters**

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) |        |        |        | $t_{RCD}$ (ns) | $t_{RP}$ (ns) | $t_{RC}$ (ns) |
|-------------|-----------------------|------------------|--------|--------|--------|----------------|---------------|---------------|
|             |                       | CL = 6           | CL = 5 | CL = 4 | CL = 3 |                |               |               |
| -80E        | PC2-6400              | –                | 800    | 533    | –      | 12.5           | 12.5          | 55            |
| -800        | PC2-6400              | 800              | 667    | 533    | –      | 15             | 15            | 55            |
| -667        | PC2-5300              | –                | 667    | 533    | 400    | 15             | 15            | 55            |
| -53E        | PC2-4200              | –                | –      | 533    | 400    | 15             | 15            | 55            |
| -40E        | PC2-3200              | –                | –      | 400    | 400    | 15             | 15            | 55            |



## 256MB, 512MB, 1GB: (x64, SR) 200-Pin DDR2 SDRAM SODIMM Features

**Table 2: Addressing**

|                           | 256MB              | 512MB              | 1GB               |
|---------------------------|--------------------|--------------------|-------------------|
| Refresh count             | 8K                 | 8K                 | 8K                |
| Row address               | 8K A[12:0]         | 16K A[13:0]        | 16K A[13:0]       |
| Device bank address       | 4 BA[1:0]          | 4 BA[1:0]          | 8 BA[2:0]         |
| Device page size per bank | 1KB                | 1KB                | 1KB               |
| Device configuration      | 256Mb (32 Meg x 8) | 512Mb (64 Meg x 8) | 1Gb (128 Meg x 8) |
| Column address            | 1K A[9:0]          | 1K A[9:0]          | 1K A[9:0]         |
| Module rank address       | 1 S0#              | 1 S0#              | 1 S0#             |

**Table 3: Part Numbers and Timing Parameters – 256MB Modules**

Base device: MT47H32M8, 256Mb DDR2 SDRAM

| Part Number <sup>1</sup> | Module Density | Configuration | Module Bandwidth | Memory Clock/<br>Data Rate | Latency<br>(CL - t <sub>RCD</sub> - t <sub>RP</sub> ) |
|--------------------------|----------------|---------------|------------------|----------------------------|-------------------------------------------------------|
| MT8HTF3264HY-667__       | 256MB          | 32 Meg x 64   | 5.3 GB/s         | 3.0ns/667 MT/s             | 5-5-5                                                 |
| MT8HTF3264HY-53E__       | 256MB          | 32 Meg x 64   | 4.3 GB/s         | 3.75ns/533 MT/s            | 4-4-4                                                 |
| MT8HTF3264HY-40E__       | 256MB          | 32 Meg x 64   | 3.2 GB/s         | 5.0ns/400 MT/s             | 3-3-3                                                 |

**Table 4: Part Numbers and Timing Parameters – 512MB Modules**

Base device: MT47H64M8, 512Mb DDR2 SDRAM

| Part Number <sup>1</sup> | Module Density | Configuration | Module Bandwidth | Memory Clock/<br>Data Rate | Latency<br>(CL - t <sub>RCD</sub> - t <sub>RP</sub> ) |
|--------------------------|----------------|---------------|------------------|----------------------------|-------------------------------------------------------|
| MT8HTF6464HY-80E__       | 512MB          | 64 Meg x 64   | 6.4 GB/s         | 2.5ns/800 MT/s             | 5-5-5                                                 |
| MT8HTF6464HY-800__       | 512MB          | 64 Meg x 64   | 6.4 GB/s         | 2.5ns/800 MT/s             | 6-6-6                                                 |
| MT8HTF6464HY-667__       | 512MB          | 64 Meg x 64   | 5.3 GB/s         | 3.0ns/667 MT/s             | 5-5-5                                                 |
| MT8HTF6464HY-53E__       | 512MB          | 64 Meg x 64   | 4.3 GB/s         | 3.75ns/533 MT/s            | 4-4-4                                                 |
| MT8HTF6464HY-40E__       | 512MB          | 64 Meg x 64   | 3.2 GB/s         | 5.0ns/400 MT/s             | 3-3-3                                                 |

**Table 5: Part Numbers and Timing Parameters – 1GB Modules**

Base device: MT47H128M8, 1Gb DDR2 SDRAM

| Part Number <sup>1</sup> | Module Density | Configuration | Module Bandwidth | Memory Clock/<br>Data Rate | Latency<br>(CL - t <sub>RCD</sub> - t <sub>RP</sub> ) |
|--------------------------|----------------|---------------|------------------|----------------------------|-------------------------------------------------------|
| MT8HTF12864HY-80E__      | 1GB            | 128 Meg x 64  | 6.4 GB/s         | 2.5ns/800 MT/s             | 5-5-5                                                 |
| MT8HTF12864HY-800__      | 1GB            | 128 Meg x 64  | 6.4 GB/s         | 2.5ns/800 MT/s             | 6-6-6                                                 |
| MT8HTF12864HY-667__      | 1GB            | 128 Meg x 64  | 5.3 GB/s         | 3.0ns/667 MT/s             | 5-5-5                                                 |
| MT8HTF12864HY-53E__      | 1GB            | 128 Meg x 64  | 4.3 GB/s         | 3.75ns/533 MT/s            | 4-4-4                                                 |
| MT8HTF12864HY-40E__      | 1GB            | 128 Meg x 64  | 3.2 GB/s         | 5.0ns/400 MT/s             | 3-3-3                                                 |

- Notes:
1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8HTF6464HY-667A3.
  2. For the latest component data sheets, see Micron's Web site:  
[www.micron.com/products/dram/ddr2](http://www.micron.com/products/dram/ddr2)



## 256MB, 512MB, 1GB: (x64, SR) 200-Pin DDR2 SDRAM SODIMM Module Pin Assignments and Descriptions

### Module Pin Assignments and Descriptions

**Table 6: Pin Assignments**

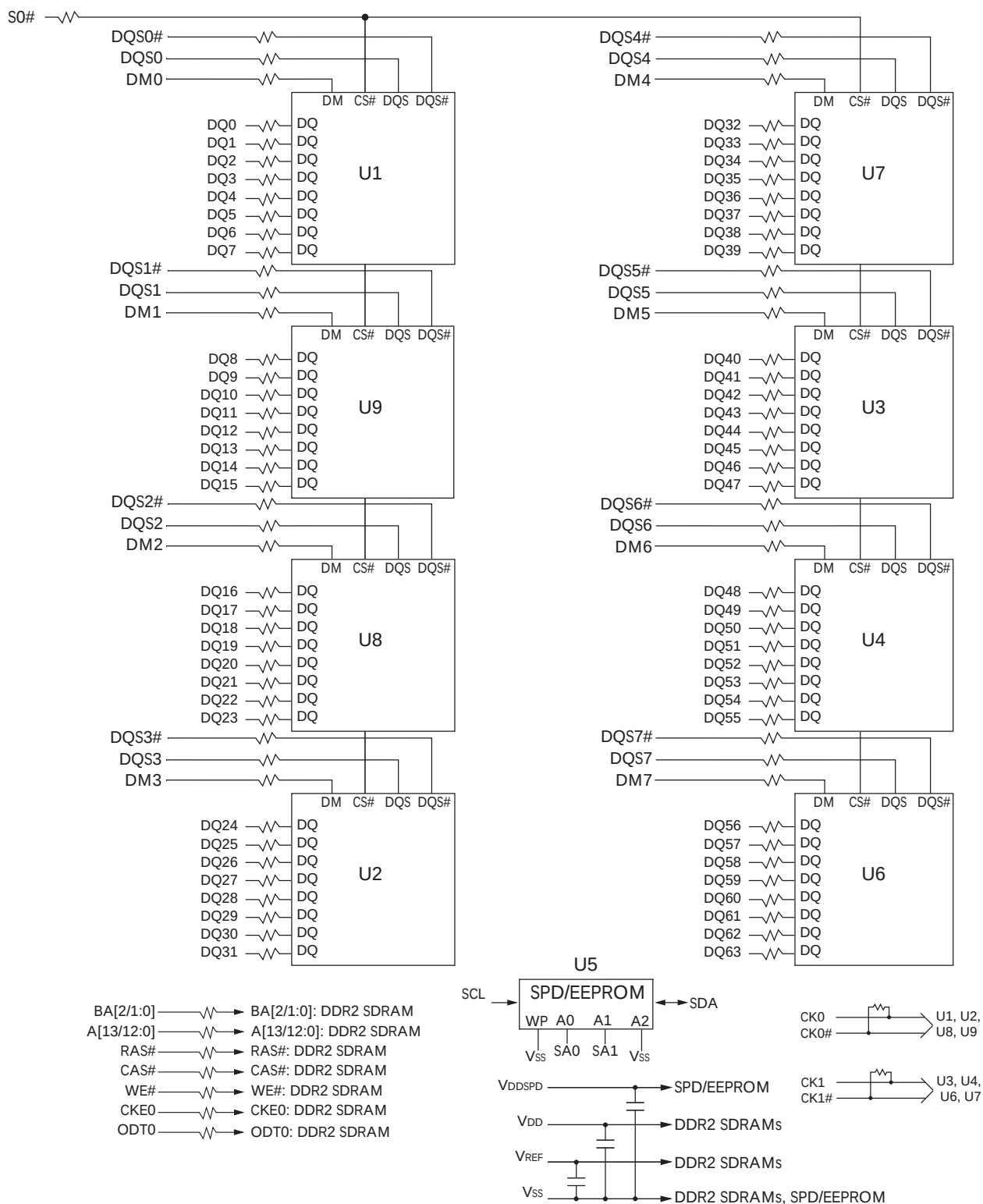
| 200-Pin SODIMM Front |        |     |        |     |        |     |        | 200-Pin SODIMM Back |        |     |        |     |        |     |        |
|----------------------|--------|-----|--------|-----|--------|-----|--------|---------------------|--------|-----|--------|-----|--------|-----|--------|
| Pin                  | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin                 | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1                    | VREF   | 51  | DQS2   | 101 | A1     | 151 | DQ42   | 2                   | Vss    | 52  | DM2    | 102 | A0     | 152 | DQ46   |
| 3                    | Vss    | 53  | Vss    | 103 | VDD    | 153 | DQ43   | 4                   | DQ4    | 54  | Vss    | 104 | VDD    | 154 | DQ47   |
| 5                    | DQ0    | 55  | DQ18   | 105 | A10/AP | 155 | Vss    | 6                   | DQ5    | 56  | DQ22   | 106 | BA1    | 156 | Vss    |
| 7                    | DQ1    | 57  | DQ19   | 107 | BA0    | 157 | DQ48   | 8                   | Vss    | 58  | DQ23   | 108 | RAS#   | 158 | DQ52   |
| 9                    | Vss    | 59  | Vss    | 109 | WE#    | 159 | DQ49   | 10                  | DM0    | 60  | Vss    | 110 | SO#    | 160 | DQ53   |
| 11                   | DQS0#  | 61  | DQ24   | 111 | VDD    | 161 | Vss    | 12                  | Vss    | 62  | DQ28   | 112 | VDD    | 162 | Vss    |
| 13                   | DQS0   | 63  | DQ25   | 113 | CAS#   | 163 | NC     | 14                  | DQ6    | 64  | DQ29   | 114 | ODT0   | 164 | CK1    |
| 15                   | Vss    | 65  | Vss    | 115 | NC#    | 165 | Vss    | 16                  | DQ7    | 66  | Vss    | 116 | NC/A13 | 166 | CK1#   |
| 17                   | DQ2    | 67  | DM3    | 117 | VDD    | 167 | DQS6#  | 18                  | Vss    | 68  | DQS3#  | 118 | VDD    | 168 | Vss    |
| 19                   | DQ3    | 69  | NC     | 119 | NC     | 169 | DQS6   | 20                  | DQ12   | 70  | DQS3   | 120 | NC     | 170 | DM6    |
| 21                   | Vss    | 71  | Vss    | 121 | Vss    | 171 | Vss    | 22                  | DQ13   | 72  | Vss    | 122 | Vss    | 172 | Vss    |
| 23                   | DQ8    | 73  | DQ26   | 123 | DQ32   | 173 | DQ50   | 24                  | Vss    | 74  | DQ30   | 124 | DQ36   | 174 | DQ54   |
| 25                   | DQ9    | 75  | DQ27   | 125 | DQ33   | 175 | DQ51   | 26                  | DM1    | 76  | DQ31   | 126 | DQ37   | 176 | DQ55   |
| 27                   | Vss    | 77  | Vss    | 127 | Vss    | 177 | Vss    | 28                  | Vss    | 78  | Vss    | 128 | Vss    | 178 | Vss    |
| 29                   | DQS1#  | 79  | CKE0   | 129 | DQS4#  | 179 | DQ56   | 30                  | CK0    | 80  | NC     | 130 | DM4    | 180 | DQ60   |
| 31                   | DQS1   | 81  | VDD    | 131 | DQS4   | 181 | DQ57   | 32                  | CK0#   | 82  | VDD    | 132 | Vss    | 182 | DQ61   |
| 33                   | Vss    | 83  | NC     | 133 | Vss    | 183 | Vss    | 34                  | Vss    | 84  | NC     | 134 | DQ38   | 184 | Vss    |
| 35                   | DQ10   | 85  | NC/BA2 | 135 | DQ34   | 185 | DM7    | 36                  | DQ14   | 86  | NC     | 136 | DQ39   | 186 | DQS7#  |
| 37                   | DQ11   | 87  | VDD    | 137 | DQ35   | 187 | Vss    | 38                  | DQ15   | 88  | VDD    | 138 | Vss    | 188 | DQS7   |
| 39                   | Vss    | 89  | A12    | 139 | Vss    | 189 | DQ58   | 40                  | Vss    | 90  | A11    | 140 | DQ44   | 190 | Vss    |
| 41                   | Vss    | 91  | A9     | 141 | DQ40   | 191 | DQ59   | 42                  | Vss    | 92  | A7     | 142 | DQ45   | 192 | DQ62   |
| 43                   | DQ16   | 93  | A8     | 143 | DQ41   | 193 | Vss    | 44                  | DQ20   | 94  | A6     | 144 | Vss    | 194 | DQ63   |
| 45                   | DQ17   | 95  | VDD    | 145 | Vss    | 195 | SDA    | 46                  | DQ21   | 96  | VDD    | 146 | DQS5#  | 196 | Vss    |
| 47                   | Vss    | 97  | A5     | 147 | DM5    | 197 | SCL    | 48                  | Vss    | 98  | A4     | 148 | DQS5   | 198 | SA0    |
| 49                   | DQS2#  | 99  | A3     | 149 | Vss    | 199 | VDDSPD | 50                  | NC     | 100 | A2     | 150 | Vss    | 200 | SA1    |

- Notes: 1. Pin 85 is NC for 256MB and 512MB, BA2 for 1GB.  
2. Pin 116 is NC for 256MB, A13 for 512MB and 1GB.

**Table 7: Pin Descriptions**

| Symbol                 | Type   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A[15:0]                | Input  | <b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[2/1:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A[12:0] (512MB) and A[13:0] (1GB, 2GB). A[15:14] are connected for parity. |
| BA[2:0]                | Input  | <b>Bank address inputs:</b> BA[2/1:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2/1:0] define which mode register (MR, EMR1, EMR2, and EMR3) is loaded during the LOAD MODE command. BA[1:0] (512MB, 1GB) and BA[2:0] (2GB).                                                                                                                                                                                                                                                                       |
| CK[1:0]<br>CK#[1:0]    | Input  | <b>Clock:</b> CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ, DQS, and DQS#) is referenced to the crossings of CK and CK#.                                                                                                                                                                                                                                                                                 |
| CKE0                   | Input  | <b>Clock enable:</b> CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| DM[8:0]                | Input  | <b>Input data mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although the DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.                                                                                                                                                                                                                                                   |
| ODT0                   | Input  | <b>On-die termination:</b> ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.                                                                                                                                                                                                                                     |
| RAS#, CAS#,<br>WE#     | Input  | <b>Command inputs:</b> RAS#, CAS#, and WE# (along with S#) define the command being entered.                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| RESET#                 | Input  | <b>Reset:</b> Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.                                                                                                                                                                                                                                                                                                                                                                                    |
| S0#                    | Input  | <b>Chip select:</b> S# enables (registered LOW) and disables (registered HIGH) the command decoder.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| SA[1:0]                | Input  | <b>Serial address inputs:</b> These pins are used to configure the SPD EEPROM address range on the I <sup>2</sup> C bus.                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| SCL                    | Input  | <b>Serial clock for SPD EEPROM:</b> SCL is used to synchronize communication to and from the SPD EEPROM.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| DQ[63:0]               | I/O    | <b>Data input/output:</b> Bidirectional data bus.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| DQS[8:0],<br>DQS#[8:0] | I/O    | <b>Data strobe:</b> DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.                                                                                                                                                                                                                                                                                                                                  |
| SDA                    | I/O    | <b>Serial data:</b> SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module on the I <sup>2</sup> C bus.                                                                                                                                                                                                                                                                                                                                                                                               |
| VDD                    | Supply | <b>Power supply:</b> 1.8V ±0.1V. The component VDD are connected to the module VDD.                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| VDDSPD                 | Supply | <b>SPD EEPROM power supply:</b> +1.7V to +3.6V.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| VREF                   | Supply | <b>Reference voltage:</b> VDD/2.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| VSS                    | Supply | Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| NC                     | –      | <b>No connect:</b> These pins are not connected on the module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

**Figure 2: Functional Block Diagram**



## General Description

The MT8HTF3264H, MT8HTF6464H, and MT8HTF12864H DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 256MB, 512MB, and 1GB memory modules organized in x64 configuration. DDR2 SDRAM modules use internally configured quad-bank (256Mb, 512Mb) or eight-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single  $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during reads and by the memory controller during writes. DQS is edge-aligned with data for reads and center-aligned with data for writes.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

## Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I<sup>2</sup>C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[1:0], which provide four unique DIMM/EEPROM addresses. Write protect (WP) is connected to VSS, permanently disabling hardware write protect.

## Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 8: Absolute Maximum Ratings**

| Symbol            | Parameter                                                                                                                                     |                                               | Min  | Max  | Units |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|------|------|-------|
| VDD               | VDD supply voltage relative to Vss                                                                                                            |                                               | −1.0 | +2.3 | V     |
| VDDQ              | VDDQ supply voltage relative to Vss                                                                                                           |                                               | −0.5 | +2.3 | V     |
| VDDL              | VDDL supply voltage relative to Vss                                                                                                           |                                               | −0.5 | +2.3 | V     |
| VIN, VOUT         | Voltage on any pin relative to Vss                                                                                                            |                                               | −0.5 | +2.3 | V     |
| I <sub>I</sub>    | Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$ ; VREF input $0V \leq V_{IN} \leq 0.95V$ ; (all other pins not under test = 0V) | Command/Address, RAS#, CAS#, WE# S#, CE#, ODT | −40  | +40  | μA    |
|                   |                                                                                                                                               | CK, CK#                                       | −20  | +20  |       |
|                   |                                                                                                                                               | DM                                            | −5   | +5   |       |
| I <sub>OZ</sub>   | Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$ ; DQs and ODT are disabled                                                             | DQ, DQS, DQS#                                 | −5   | +5   | μA    |
| I <sub>VREF</sub> | VREF leakage current; VREF = Valid VREF level                                                                                                 |                                               | −16  | +16  | μA    |
| T <sub>CASE</sub> | DDR2 SDRAM device operating temperature <sup>1</sup>                                                                                          | Commercial                                    | 0    | +85  | °C    |
|                   |                                                                                                                                               | Industrial <sup>2</sup>                       | −40  | +95  | °C    |

- Notes: 1. For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site at [www.micron.com/technotes](http://www.micron.com/technotes).  
2. Refresh rate must double when T<sub>CASE</sub> exceeds 85°C.



## DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9.

**Table 9: Module and Component Speed Grades**  
DDR2 components may exceed the listed module speed grades

| Module Speed Grade | Component Speed Grade |
|--------------------|-----------------------|
| -80E               | -25E                  |
| -800               | -25                   |
| -667               | -3                    |
| -53E               | -37E                  |
| -40E               | -5E                   |

## Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.





## 256MB, 512MB, 1GB: (x64, SR) 200-Pin DDR2 SDRAM SODIMM Electrical Specifications

**Table 10: DDR2 I<sub>DD</sub> Specifications and Conditions – 256MB**

Values are for the MT47H32M8 DDR2 SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

| Parameter/Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Symbol            | -667  | -53E  | -40E  | Units |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------|-------|-------|-------|
| <b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                                  | I <sub>DD0</sub>  | 720   | 640   | 600   | mA    |
| <b>Operating one bank active-read-precharge current;</b> I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$ , $t_{RCD} = t_{RCD} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I <sub>DD4W</sub>                                                                                                              | I <sub>DD1</sub>  | 800   | 720   | 680   | mA    |
| <b>Precharge power-down current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                        | I <sub>DD2P</sub> | 40    | 40    | 40    | mA    |
| <b>Precharge quiet standby current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                                        | I <sub>DD2Q</sub> | 320   | 280   | 200   | mA    |
| <b>Precharge standby current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                                                                                                          | I <sub>DD2N</sub> | 320   | 280   | 240   | mA    |
| <b>Active power-down current;</b> All device banks open; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                           | I <sub>DD3P</sub> | 240   | 200   | 160   | mA    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                   | 48    | 48    | 48    | mA    |
| <b>Active standby current;</b> All device banks open; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                              | I <sub>DD3N</sub> | 400   | 320   | 240   | mA    |
| <b>Operating burst write current;</b> All device banks open, continuous burst writes; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                                                    | I <sub>DD4W</sub> | 1,520 | 1,280 | 1,000 | mA    |
| <b>Operating burst read current;</b> All device banks open, continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                              | I <sub>DD4R</sub> | 1,440 | 1,200 | 920   | mA    |
| <b>Burst refresh current;</b> $t_{CK} = t_{CK} (I_{DD})$ ; Refresh the command at every $t_{RFC} (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                                                    | I <sub>DD5</sub>  | 1,440 | 1,360 | 1,320 | mA    |
| <b>Self refresh current;</b> CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                                                                | I <sub>DD6</sub>  | 40    | 40    | 40    | mA    |
| <b>Operating bank interleave read current;</b> All device banks interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = $t_{RCD} (I_{DD}) - 1 \times t_{CK} (I_{DD})$ ; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RRD} = t_{RRD} (I_{DD})$ , $t_{RCD} = t_{RCD} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselections; Data bus inputs are switching; See I <sub>DD7</sub> conditions for detail | I <sub>DD7</sub>  | 2,080 | 1,920 | 1,840 | mA    |

**Table 11: DDR2 I<sub>DD</sub> Specifications and Conditions – 512MB**

Values are for the MT47H64M8 DDR2 SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

| Parameter/Condition                                                                                                                                                                                                                                                                                                                                                                                                                                               |                             | Symbol | -80E/-800 | -667 | -53E | -40E | Units |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|--------|-----------|------|------|------|-------|
| <b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                          |                             | IDD0   | 800       | 720  | 640  | 640  | mA    |
| <b>Operating one bank active-read-precharge current;</b> IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$ , $t_{RCD} = t_{RCD} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W                                                                                                           |                             | IDD1   | 920       | 840  | 760  | 720  | mA    |
| <b>Precharge power-down current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                |                             | IDD2P  | 56        | 56   | 56   | 56   | mA    |
| <b>Precharge quiet standby current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                |                             | IDD2Q  | 400       | 360  | 320  | 280  | mA    |
| <b>Precharge standby current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                                                                  |                             | IDD2N  | 440       | 400  | 360  | 320  | mA    |
| <b>Active power-down current;</b> All device banks open; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                   | Fast PDN Exit<br>MR[12] = 0 | IDD3P  | 320       | 280  | 240  | 200  | mA    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Slow PDN Exit<br>MR[12] = 1 |        | 96        | 96   | 96   | 96   | mA    |
| <b>Active standby current;</b> All device banks open; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                      |                             | IDD3N  | 560       | 520  | 440  | 360  | mA    |
| <b>Operating burst write current;</b> All device banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                         |                             | IDD4W  | 1560      | 1360 | 1120 | 920  | mA    |
| <b>Operating burst read current;</b> All device banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                               |                             | IDD4R  | 1640      | 1440 | 1160 | 920  | mA    |
| <b>Burst refresh current;</b> $t_{CK} = t_{CK} (I_{DD})$ ; Refresh the command at every $t_{RFC} (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                            |                             | IDD5   | 1840      | 1440 | 1360 | 1320 | mA    |
| <b>Self refresh current;</b> CK and CK# at 0V; CKE $\leq 0.2V$ ; Other control and address bus inputs are floating; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                  |                             | IDD6   | 56        | 56   | 56   | 56   | mA    |
| <b>Operating bank interleave read current;</b> All device banks interleaving reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = $t_{RCD} (I_{DD}) - 1 \times t_{CK} (I_{DD})$ ; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RRD} = t_{RRD} (I_{DD})$ , $t_{RCD} = t_{RCD} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See IDD7 conditions for detail |                             | IDD7   | 2400      | 1920 | 1800 | 1760 | mA    |

**Table 12: DDR2 I<sub>DD</sub> Specifications and Conditions – 1GB (die revision A)**

Values are for the MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

| Parameter/Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                             | Symbol            | -80E/-800 | -667 | -53E  | -40E | Units |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|-------------------|-----------|------|-------|------|-------|
| <b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                               |                             | I <sub>DD0</sub>  | 800       | 720  | 640   | 560  | mA    |
| <b>Operating one bank active-read-precharge current;</b> I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$ , $t_{RCD} = t_{RCD} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I <sub>DD4W</sub>                                                                                                           |                             | I <sub>DD1</sub>  | 880       | 800  | 760   | 640  | mA    |
| <b>Precharge power-down current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                     |                             | I <sub>DD2P</sub> | 56        | 56   | 56    | 56   | mA    |
| <b>Precharge quiet standby current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                                     |                             | I <sub>DD2Q</sub> | 520       | 440  | 328   | 280  | mA    |
| <b>Precharge standby current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                                                                                                       |                             | I <sub>DD2N</sub> | 560       | 480  | 360   | 320  | mA    |
| <b>Active power-down current;</b> All device banks open; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                        | Fast PDN Exit<br>MR[12] = 0 | I <sub>DD3P</sub> | 360       | 320  | 280   | 280  | mA    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Slow PDN Exit<br>MR[12] = 1 |                   | 112       | 112  | 112   | 112  | mA    |
| <b>Active standby current;</b> All device banks open; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                           |                             | I <sub>DD3N</sub> | 600       | 560  | 440   | 360  | mA    |
| <b>Operating burst write current;</b> All device banks open, continuous burst writes; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                                                 |                             | I <sub>DD4W</sub> | 1480      | 1280 | 1,040 | 880  | mA    |
| <b>Operating burst read current;</b> All device banks open, continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                           |                             | I <sub>DD4R</sub> | 1520      | 1280 | 1040  | 880  | mA    |
| <b>Burst refresh current;</b> $t_{CK} = t_{CK} (I_{DD})$ ; Refresh the command at every $t_{RFC} (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                                                 |                             | I <sub>DD5</sub>  | 2240      | 2080 | 2000  | 1760 | mA    |
| <b>Self refresh current;</b> CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                                                             |                             | I <sub>DD6</sub>  | 56        | 56   | 56    | 56   | mA    |
| <b>Operating bank interleave read current;</b> All device banks interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = $t_{RCD} (I_{DD}) - 1 \times t_{CK} (I_{DD})$ ; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RRD} = t_{RRD} (I_{DD})$ , $t_{RCD} = t_{RCD} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See I <sub>DD7</sub> conditions for detail |                             | I <sub>DD7</sub>  | 2680      | 2400 | 2320  | 2080 | mA    |

**Table 13: DDR2 I<sub>DD</sub> Specifications and Conditions – 1GB (die revision E)**

Values are for the MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

| Parameter/Condition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Symbol            | -80E/-800                   | -667 | -53E | -40E | Units |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----------------------------|------|------|------|-------|
| <b>Operating one bank active-precharge current;</b> $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                               | I <sub>DD0</sub>  | 720                         | 680  | 560  | 560  | mA    |
| <b>Operating one bank active-read-precharge current;</b> I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$ , $t_{RCD} = t_{RCD} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I <sub>DD4W</sub>                                                                                                           | I <sub>DD1</sub>  | 880                         | 800  | 760  | 720  | mA    |
| <b>Precharge power-down current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                     | I <sub>DD2P</sub> | 56                          | 56   | 56   | 56   | mA    |
| <b>Precharge quiet standby current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                                     | I <sub>DD2Q</sub> | 400                         | 320  | 320  | 280  | mA    |
| <b>Precharge standby current;</b> All device banks idle; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                                                                                                       | I <sub>DD2N</sub> | 400                         | 320  | 320  | 280  | mA    |
| <b>Active power-down current;</b> All device banks open; $t_{CK} = t_{CK} (I_{DD})$ ; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                        | I <sub>DD3P</sub> | Fast PDN Exit<br>MR[12] = 0 | 320  | 240  | 240  | mA    |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                   | Slow PDN Exit<br>MR[12] = 1 | 80   | 80   | 80   | mA    |
| <b>Active standby current;</b> All device banks open; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                           | I <sub>DD3N</sub> | 480                         | 440  | 360  | 320  | mA    |
| <b>Operating burst write current;</b> All device banks open, continuous burst writes; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                                                 | I <sub>DD4W</sub> | 1280                        | 1080 | 1000 | 840  | mA    |
| <b>Operating burst read current;</b> All device banks open, continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching                                                                                                                           | I <sub>DD4R</sub> | 1280                        | 1080 | 1000 | 840  | mA    |
| <b>Burst refresh current;</b> $t_{CK} = t_{CK} (I_{DD})$ ; Refresh the command at every $t_{RFC} (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching                                                                                                                                                                                                                                                 | I <sub>DD5</sub>  | 1880                        | 1720 | 1680 | 1640 | mA    |
| <b>Self refresh current;</b> CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating                                                                                                                                                                                                                                                                                                                                                             | I <sub>DD6</sub>  | 56                          | 56   | 56   | 56   | mA    |
| <b>Operating bank interleave read current;</b> All device banks interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = $t_{RCD} (I_{DD}) - 1 \times t_{CK} (I_{DD})$ ; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RRD} = t_{RRD} (I_{DD})$ , $t_{RCD} = t_{RCD} (I_{DD})$ ; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See I <sub>DD7</sub> conditions for detail | I <sub>DD7</sub>  | 2680                        | 2240 | 2160 | 2080 | mA    |

## Serial Presence-Detect

**Table 14: Serial Presence-Detect EEPROM DC Operating Conditions**

| Parameter/Condition                                               | Symbol             | Min                      | Max                      | Units |
|-------------------------------------------------------------------|--------------------|--------------------------|--------------------------|-------|
| Supply voltage                                                    | V <sub>DDSPD</sub> | 1.7                      | 3.6                      | V     |
| Input high voltage: Logic 1; All inputs                           | V <sub>IH</sub>    | V <sub>DDSPD</sub> × 0.7 | V <sub>DDSPD</sub> + 0.5 | V     |
| Input low voltage: Logic 0; All inputs                            | V <sub>IL</sub>    | –0.6                     | V <sub>DDSPD</sub> × 0.3 | V     |
| Output low voltage: I <sub>OUT</sub> = 3mA                        | V <sub>OL</sub>    | –                        | 0.4                      | V     |
| Input leakage current: V <sub>IN</sub> = GND to V <sub>DD</sub>   | I <sub>LI</sub>    | 0.1                      | 3.0                      | μA    |
| Output leakage current: V <sub>OUT</sub> = GND to V <sub>DD</sub> | I <sub>LO</sub>    | 0.05                     | 3.0                      | μA    |
| Standby current                                                   | I <sub>SB</sub>    | 1.6                      | 4.0                      | μA    |
| Power supply current, READ: SCL clock frequency = 100 kHz         | I <sub>CCR</sub>   | 0.4                      | 1.0                      | mA    |
| Power supply current, WRITE: SCL clock frequency = 100 kHz        | I <sub>CCW</sub>   | 2.0                      | 3.0                      | mA    |

**Table 15: Serial Presence-Detect EEPROM AC Operating Conditions**

| Parameter/Condition                                         | Symbol              | Min | Max | Units | Notes |
|-------------------------------------------------------------|---------------------|-----|-----|-------|-------|
| SCL LOW to SDA data-out valid                               | t <sub>AA</sub>     | 0.2 | 0.9 | μs    | 1     |
| Time the bus must be free before a new transition can start | t <sub>BUF</sub>    | 1.3 | –   | μs    |       |
| Data-out hold time                                          | t <sub>DH</sub>     | 200 | –   | ns    |       |
| SDA fall time                                               | t <sub>F</sub>      | –   | 300 | ns    | 2     |
| SDA rise time                                               | t <sub>R</sub>      | –   | 300 | ns    | 2     |
| Data-in hold time                                           | t <sub>HD:DAT</sub> | 0   | –   | μs    |       |
| Start condition hold time                                   | t <sub>H:STA</sub>  | 0.6 | –   | μs    |       |
| Clock HIGH period                                           | t <sub>HIGH</sub>   | 0.6 | –   | μs    |       |
| Noise suppression time constant at SCL, SDA inputs          | t <sub>I</sub>      | –   | 50  | ns    |       |
| Clock LOW period                                            | t <sub>LOW</sub>    | 1.3 | –   | μs    |       |
| SCL clock frequency                                         | f <sub>SCL</sub>    | –   | 400 | kHz   |       |
| Data-in setup time                                          | t <sub>SU:DAT</sub> | 100 | –   | ns    |       |
| Start condition setup time                                  | t <sub>SU:STA</sub> | 0.6 | –   | μs    | 3     |
| Stop condition setup time                                   | t <sub>SU:STO</sub> | 0.6 | –   | μs    |       |
| WRITE cycle time                                            | t <sub>WRC</sub>    | –   | 10  | ms    | 4     |

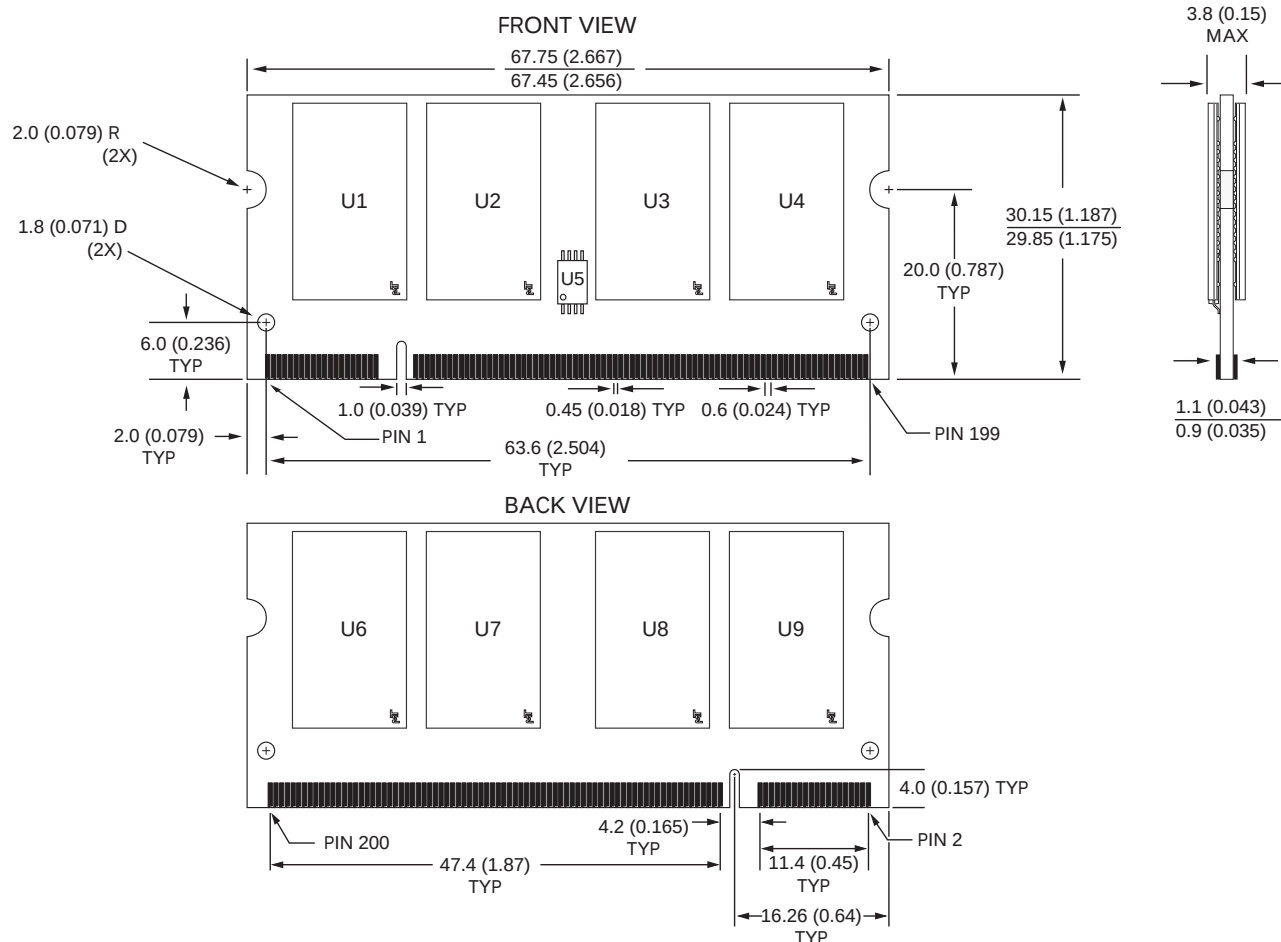
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
  2. This parameter is sampled.
  3. For a restart condition or following a WRITE cycle.
  4. The SPD EEPROM WRITE cycle time (t<sub>WRC</sub>) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

## Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:  
[www.micron.com/SPD](http://www.micron.com/SPD).

## Module Dimensions

**Figure 3: 200-pin DDR2 SODIMM Module Dimensions**



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
  2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.



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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.