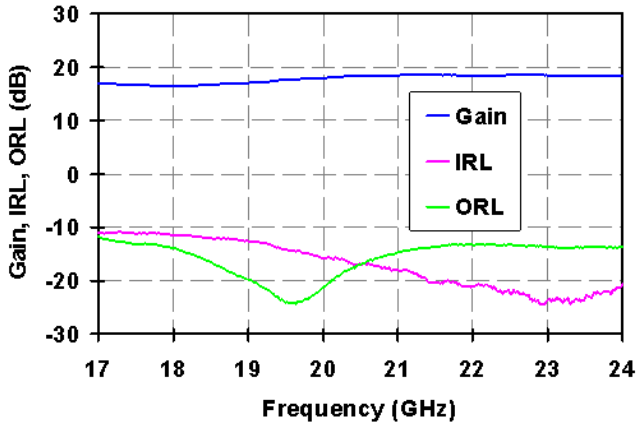
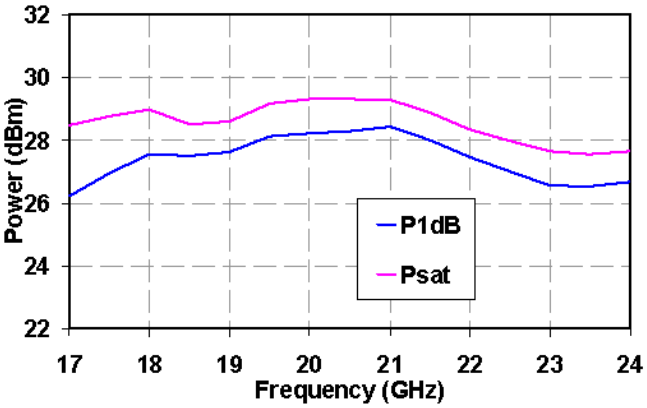
17- 24 GHz Power Amplifier

Measured Performance

Bias conditions: Vd = 5 V, Id = 712 mA , Vg = -0.5 V Typical





Key Features

- Frequency Range 17 GHz to 24 GHz.
- 28 dBm Output Psat, 26 dBm P1dB, typical.
- 35 dBm Output TOI.
- 17 dB Typical Gain.
- Integrated power detection with 30 dB dynamic range.
- High ESD tolerance.
- Dimensions: 4.0 x 4.0 x 0.85 mm
- Bias conditions: Vd = 5 V, Id = 712 mA, Vg = -0.5 V, typical.

Primary Applications

- Point-to-Point Radio
- Point-to-Multipoint Communications

Product Description

The TriQuint TGA2522-SM is a three stage HPA MMIC design using TriQuint's proven 0.25 um Power pHEMT process. The TGA2522-SM is designed to support a variety of millimeter wave applications including point-to-point digital radio and other K band linear gain applications.

The TGA2522-SM provides 26 dBm nominal output power at 1dB compression across 17-24 GHz. Typical small signal gain is 17 dB at 17 GHz and 18 dB at 24 GHz.

The TGA2522-SM requires minimum off-chip components. Each device is DC and RF tested for key parameters. The device is available in a 4 x 4 mm plastic QFN package.

RoHS and Lead-Free compliant. Evaluation boards available on request.

Datasheet subject to change without notice.

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Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd - Vg	Drain to Gate Voltage	11 V	
Vd1,2	Drain Voltage	8 V	2/
Vg1,2	Gate Voltage Range	-5 V to 0 V	
Vd3	Drain Voltage	8 V	2/
Vg3	Gate Voltage Range	-5 V to 0 V	
Id1, 2	Drain Current	1750 mA	2/
Id3	Drain Current	1575 mA	2/
Ig1,2	Gate Current Range	35 mA	
Ig3	Gate Current Range	31.5 mA	
Pin	Input Continuous Wave Power	26 dBm	2/
Tchannel	Channel Temperature	200 °C	

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

Table II
Recommended Operating Conditions

Symbol	Parameter 1/	Value
Vd1,2, Vd3	Drain Voltage	5 V
Id1,2, Id3	Drain Current	712 mA
Id_Drive	Drain Current under RF Drive	850 mA
Vg1,2, Vg3	Gate Voltage	-0.5 V

1/ See assembly diagram for bias instructions.

Table III
RF Characterization Table

Bias: Vd = 5 V, Id = 712 mA, Vg = - 0.5 V, Typical

SYMBOL	PARAMETER	TEST CONDITIONS	MINIMUM	NOMINAL	MAXIMUM	UNITS
Gain	Small Signal Gain	f = 17.7-23.6 GHz	15	18		dB
IRL	Input Return Loss	f = 17.7-23.6 GHz		12		dB
ORL	Output Return Loss	f = 17.7-23.6 GHz		13		dB
Psat	Saturated Output Power	f = 17.7-22 GHz f = 23.6 GHz	26.5 25.5	28		dBm
P1dB	Output Power @1dB Compression	f = 17.7-22 GHz f = 23.6 GHz	25 24	27		dBm
TOI	Output TOI	f = 17.7-23.6 GHz	33	36		dBm

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Table IV
Power Dissipation and Thermal Properties

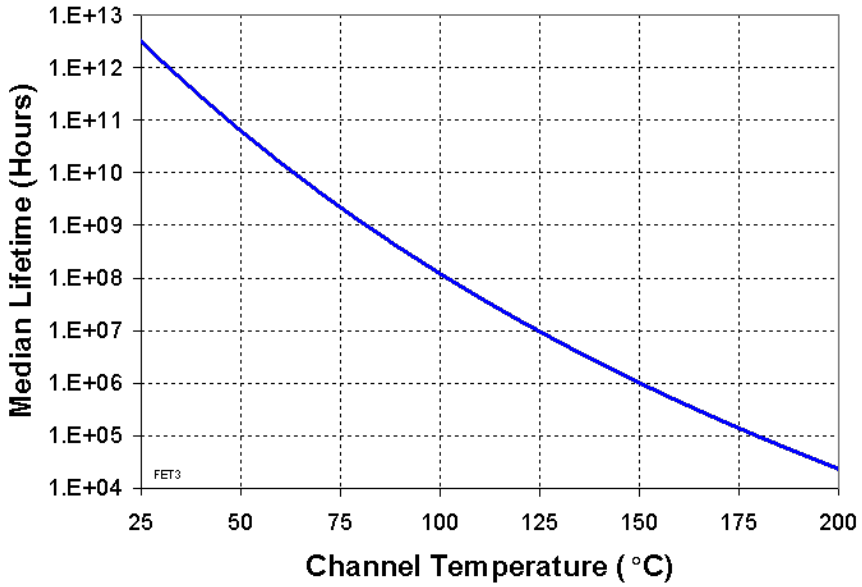
Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 85 °C	Pd = 8.52 W Tchannel = 200 °C	1/ 2/
Thermal Resistance, θ_{JC}	Vd = 5 V Id = 712 A Pd = 3.56 W Tbaseplate = 85 °C	θ_{JC} = 13.5 °C/W Tchannel = 133 °C Tm = 4.5E+6 Hrs	
Thermal Resistance, θ_{JC} Under RF Drive	Vd = 5 V Id = 850 mA Pout = 30 dBm Pd = 3.25 W	θ_{JC} = 13.5 °C/W Tchannel = 129 °C Tm = 6.2E+6 Hrs	
Mounting Temperature	30 Seconds	320 °C	
Storage Temperature		-65 to 150 °C	

1/ For a median life of 1E+6 hours, Power Dissipation is limited to

$Pd(max) = (150\ °C - Tbase\ °C)/\ \theta_{JC}$.

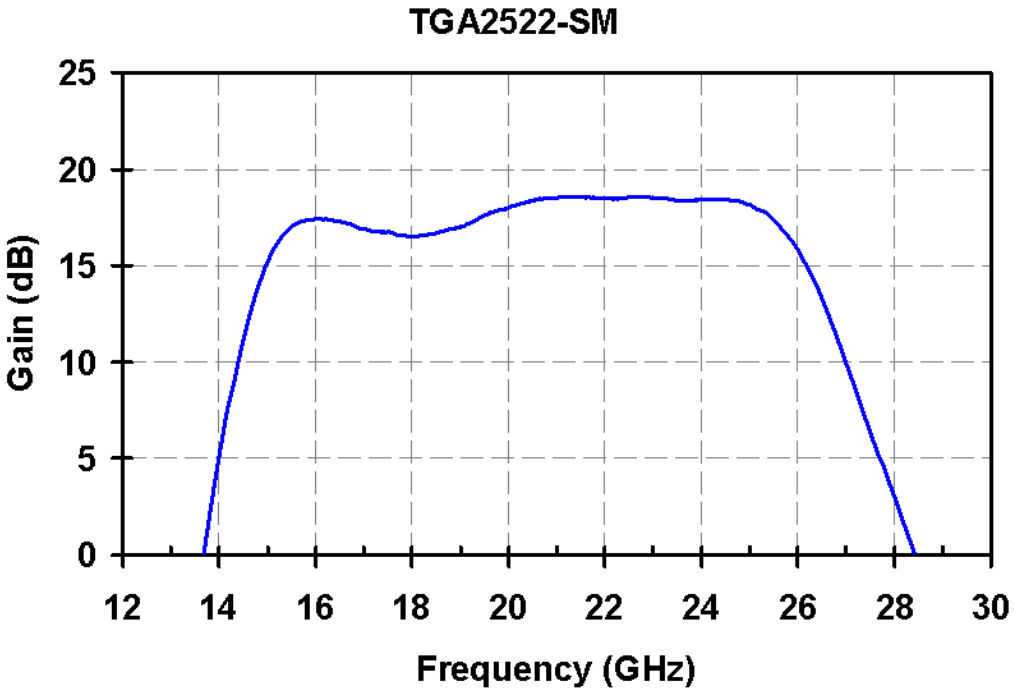
2/ Channel operating temperature will directly affect the device lifetime. For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

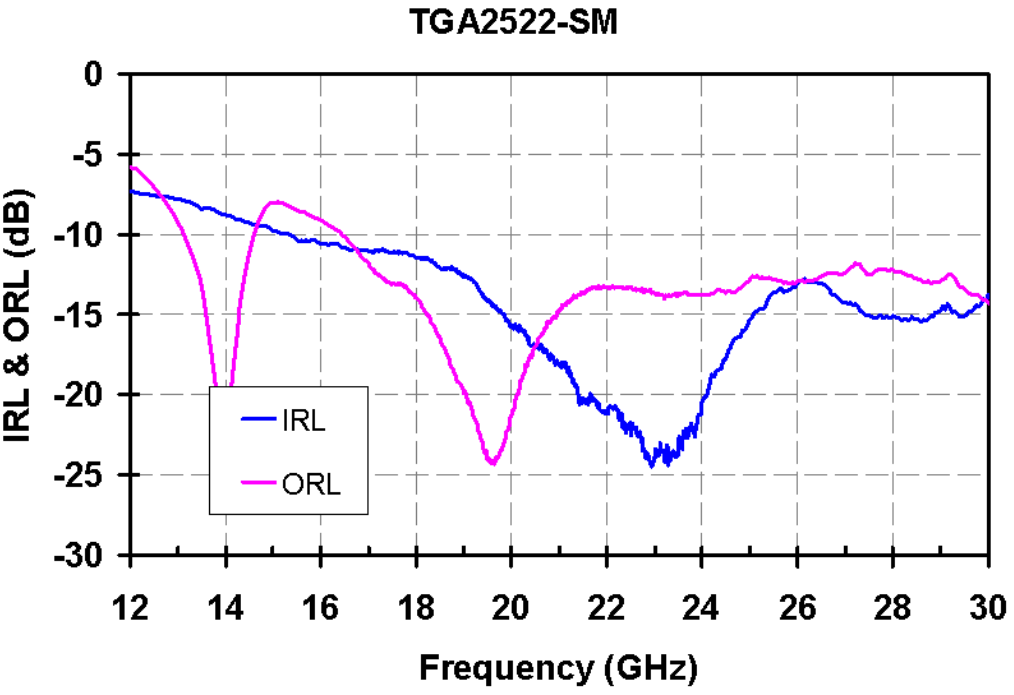
Median Lifetime (Tm) vs. Channel Temperature



Measured Data

Bias conditions: Vd = 5 V, Id = 712 mA, Vg = -0.5 V Typical





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Measured Data

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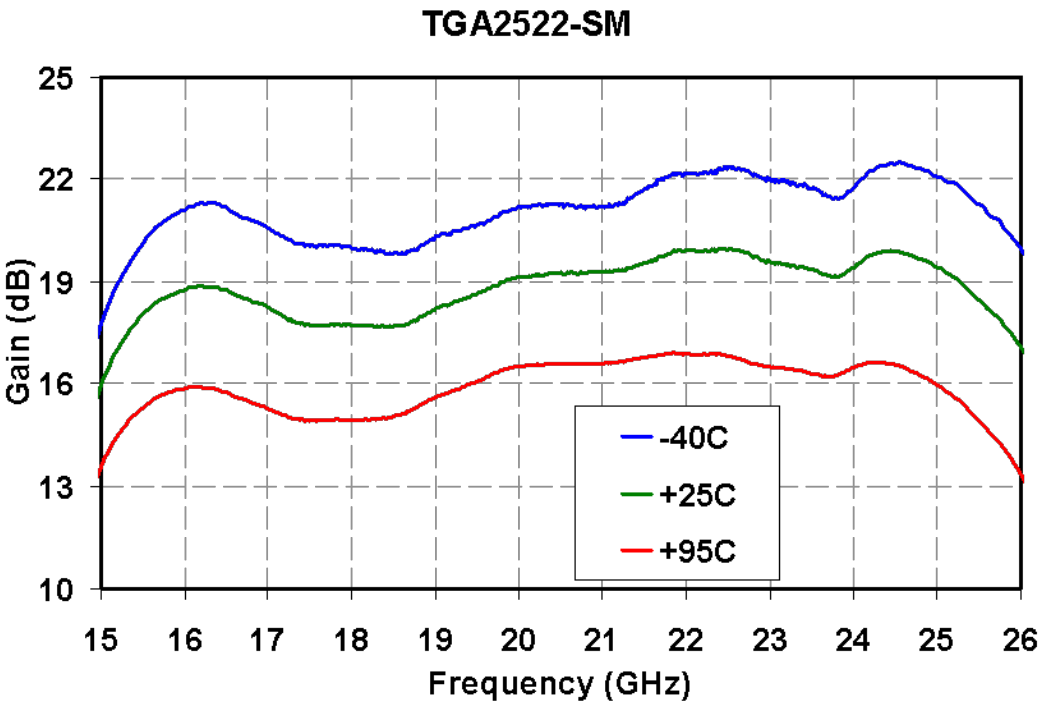

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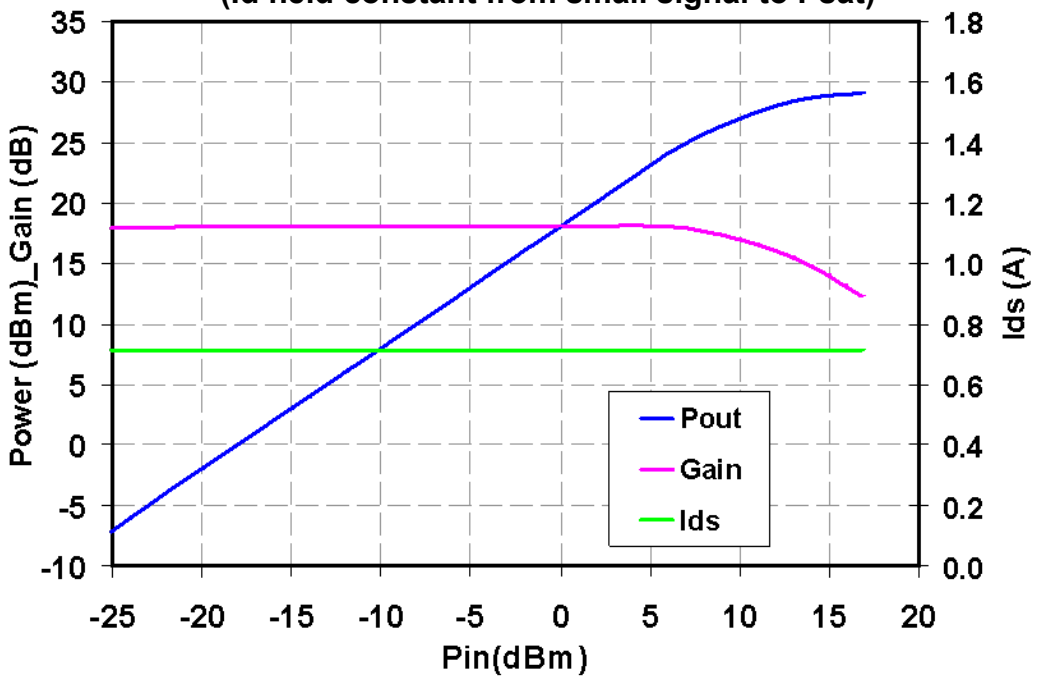
Measured Data

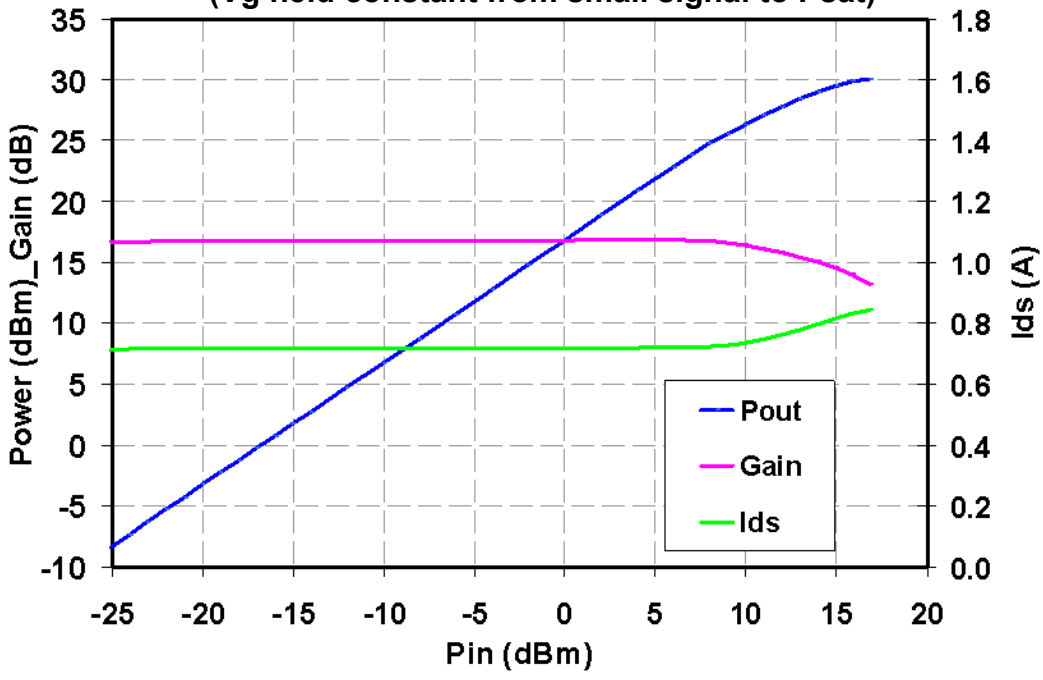
Bias conditions: Vd = 5 V, Id = 712 mA, Vg = -0.5 V. Frequency = 19 GHz

(Id held constant from small signal to Psat)



Bias conditions: Vd = 5 V, Id = 712 mA, Vg = -0.5 V. Frequency = 19 GHz

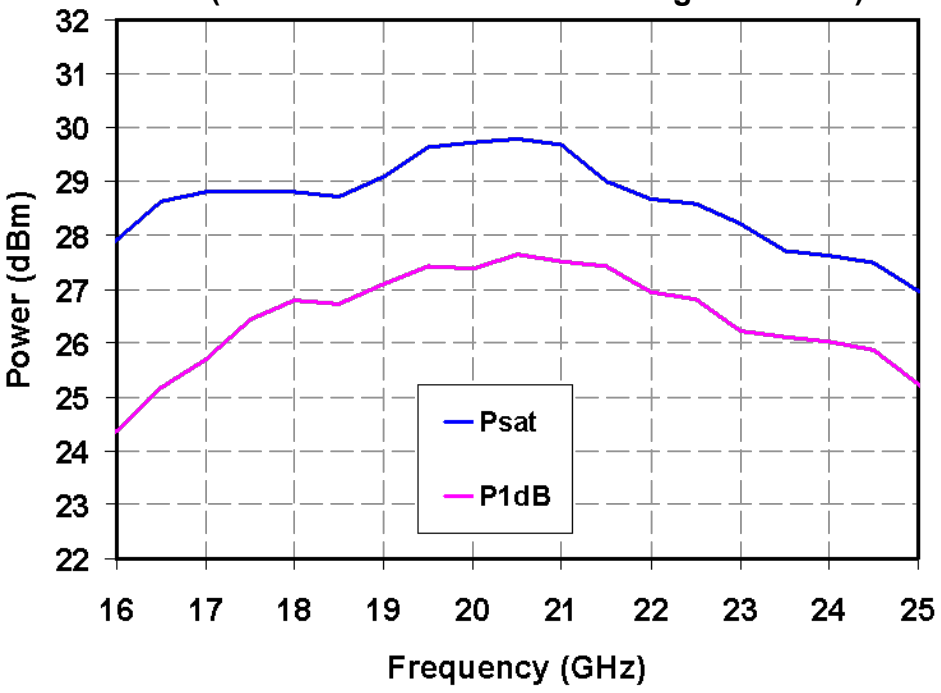
(Vg held constant from small signal to Psat)



Measured Data

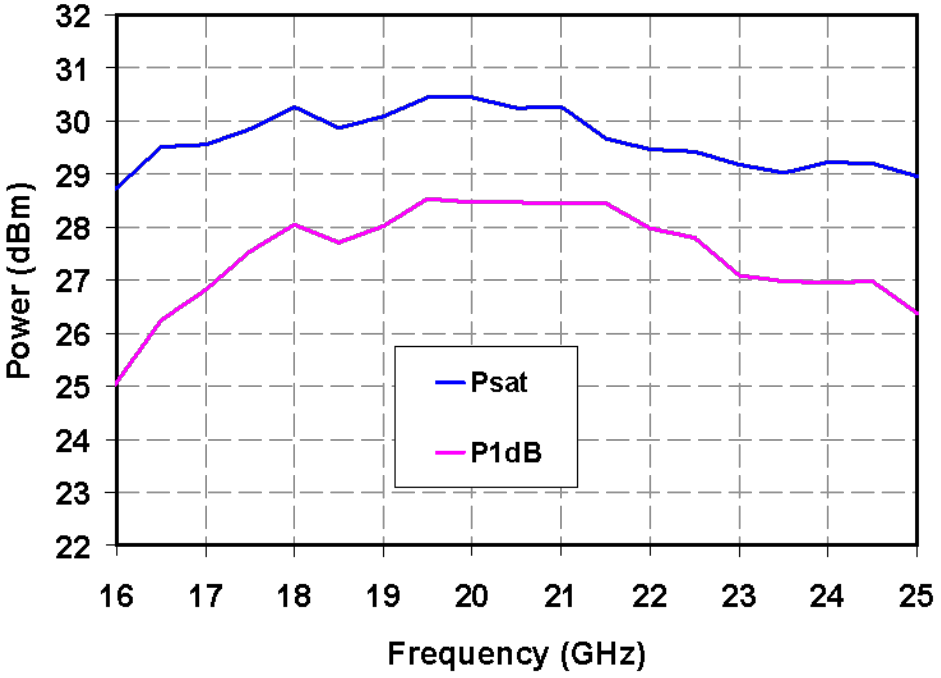
Bias conditions: Vd = 5 V, Id = 712 mA, Vg = -0.5 V

(Id held constant from small signal to Psat)



Bias conditions: Vd = 5 V, Id = 712 mA, Vg = -0.5 V

(Vg held constant from small signal to Psat)



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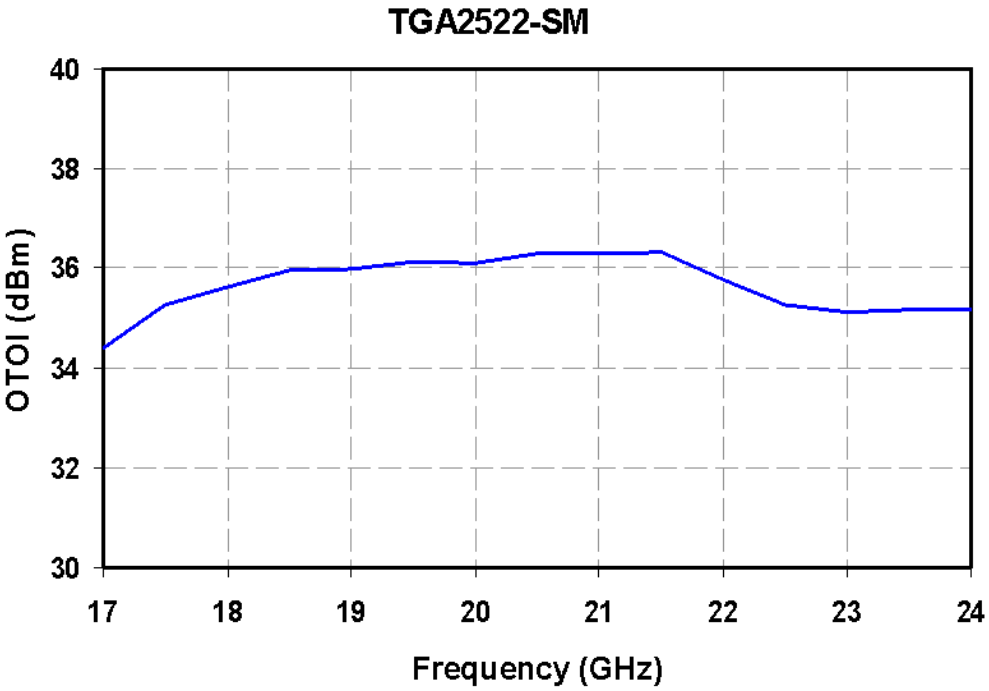
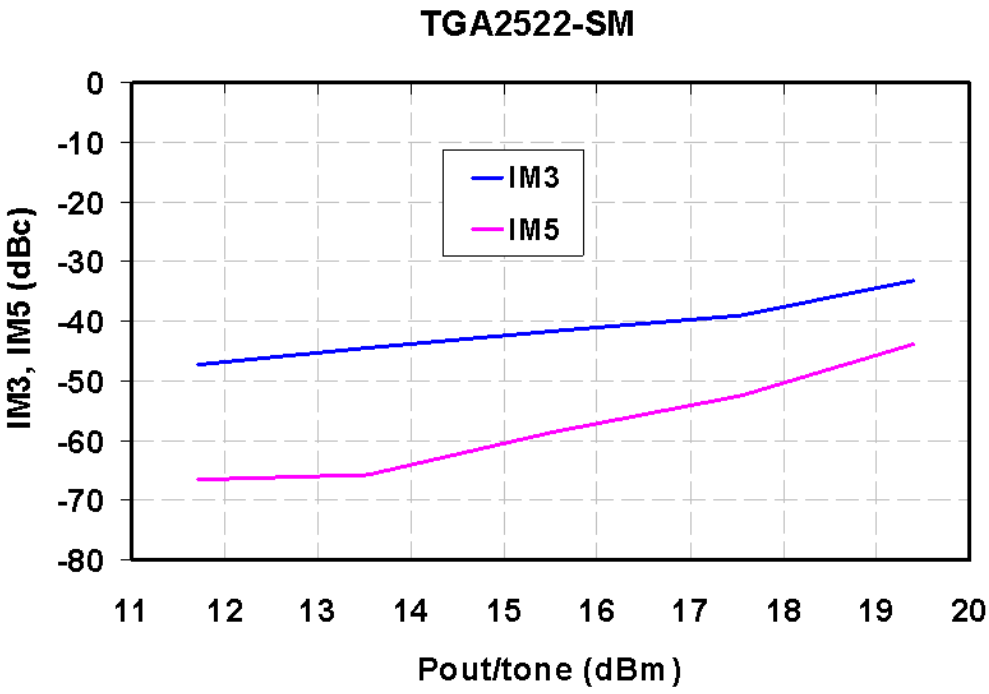
Measured Data

Bias conditions: Vd = 5 V, Id = 712 mA, Vg = -0.5 V Typical





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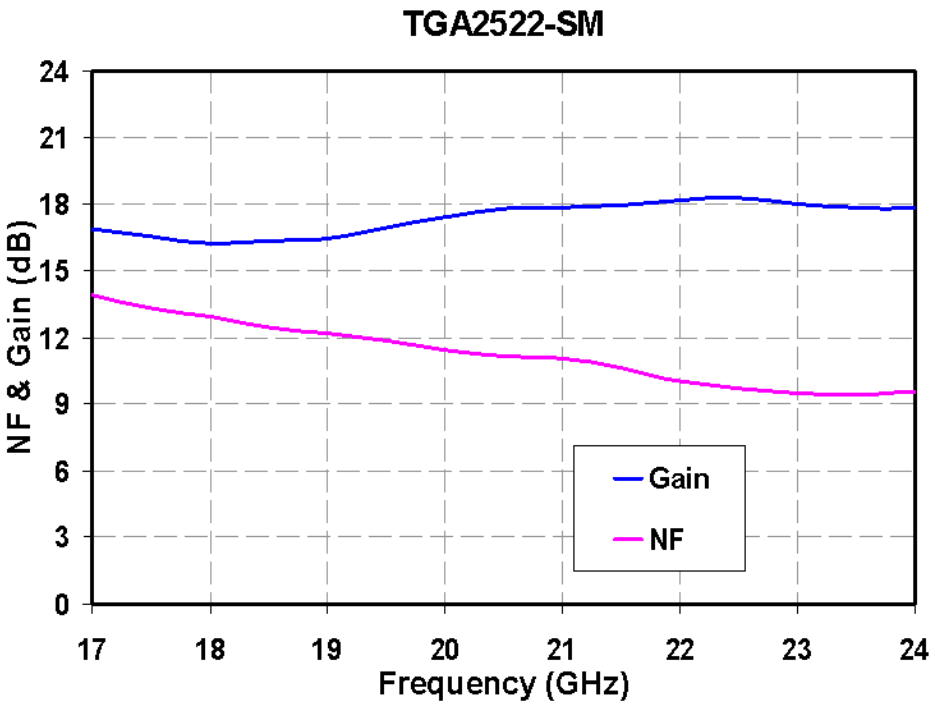
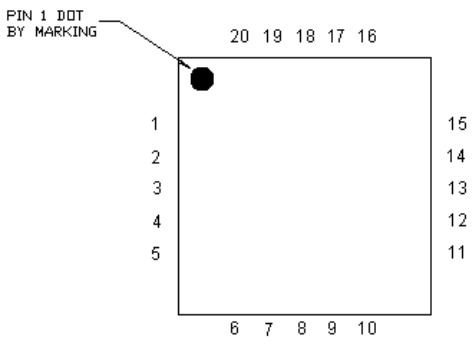
Measured Data

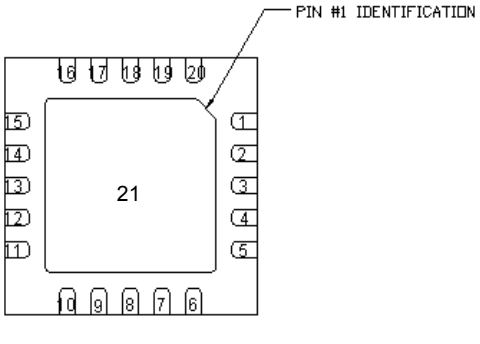
Bias conditions: Vd = 5 V, Id = 712 mA, Vg = -0.5 V Typical



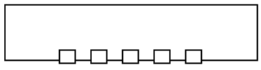
Package Pinout



TOP VIEW



BOTTOM VIEW

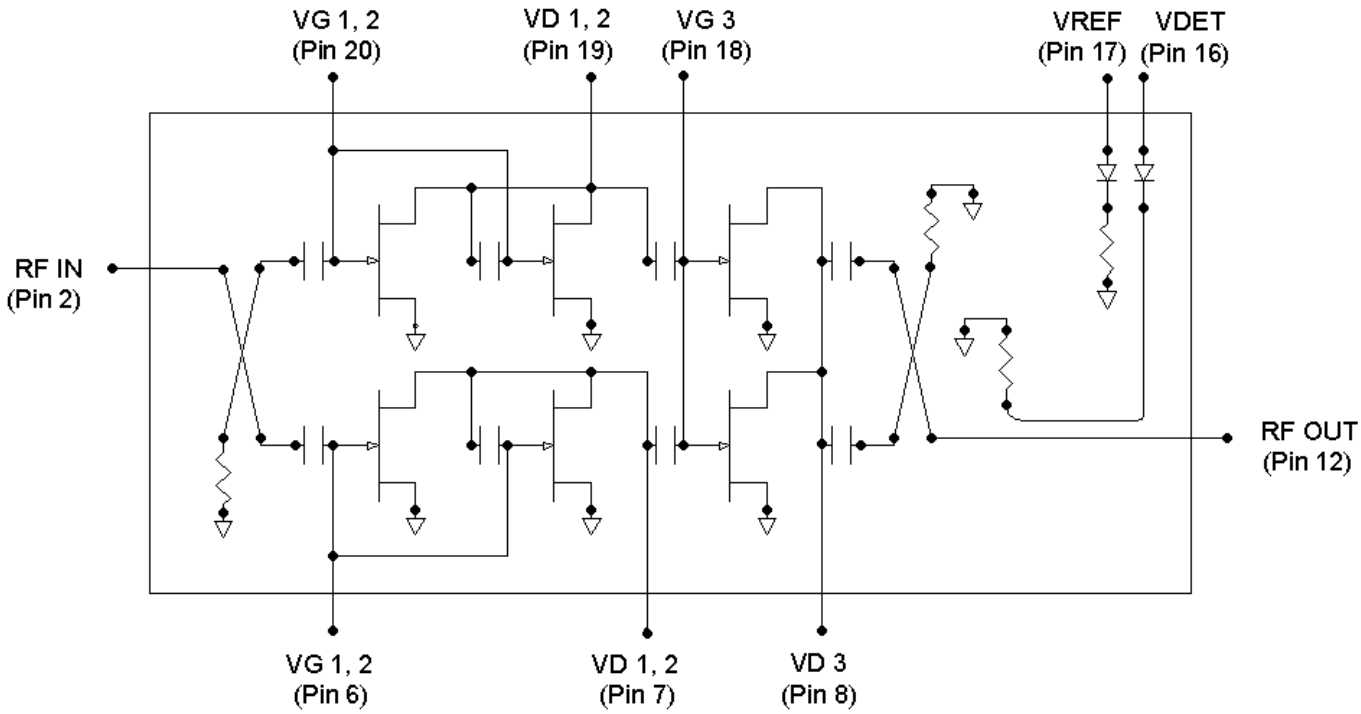


SIDE VIEW

Pin	Symbol	Description
2	RF In	Input, matched to 50 ohms.
12	RF Out	Output, matched to 50 ohms.
6,20	Vg1,2	Gate voltage for amplifier's input and 2nd stage. Must be biased from both sides. 1/
18	Vg3	Gate voltage for amplifier's final stage. 1/
7,19	Vd1,2	Drain voltage for amplifier's input and 2nd stage. Must be biased from both sides. 1/
8	Vd3	Drain voltage for amplifier's final stage. 1/
16	VDET	Reference diode output voltage.
17	VREF	Detector diode output voltage. Varies with RF output power.
5,13	GND	Connected to 21 internally. Must be grounded to the PCB. See 'Recommended Land Pattern'.
1, 3,4,11,14,15	NC	No internal connection. Must be grounded to the PCB. See 'Recommended Land Pattern'.
9,10	NC	No internal connection. Can be grounded or left open on the PCB.
21	GND	Backside paddle. Multiple vias on the PCB should be employed to minimize inductance and thermal resistance. See 'Recommended Land Pattern'.

1/ Bias network required. See 'Recommended Application Circuit'.

Electrical Schematic



Bias Procedures

Bias-up Procedure

VG 1, 2, VG 3 set to -1.5 V

VD 1, 2, VD 3 set to +5 V

Adjust VG 1, 2, VG 3 more positive until Id is 712 mA. This will be ~ -0.5 V

Apply RF signal

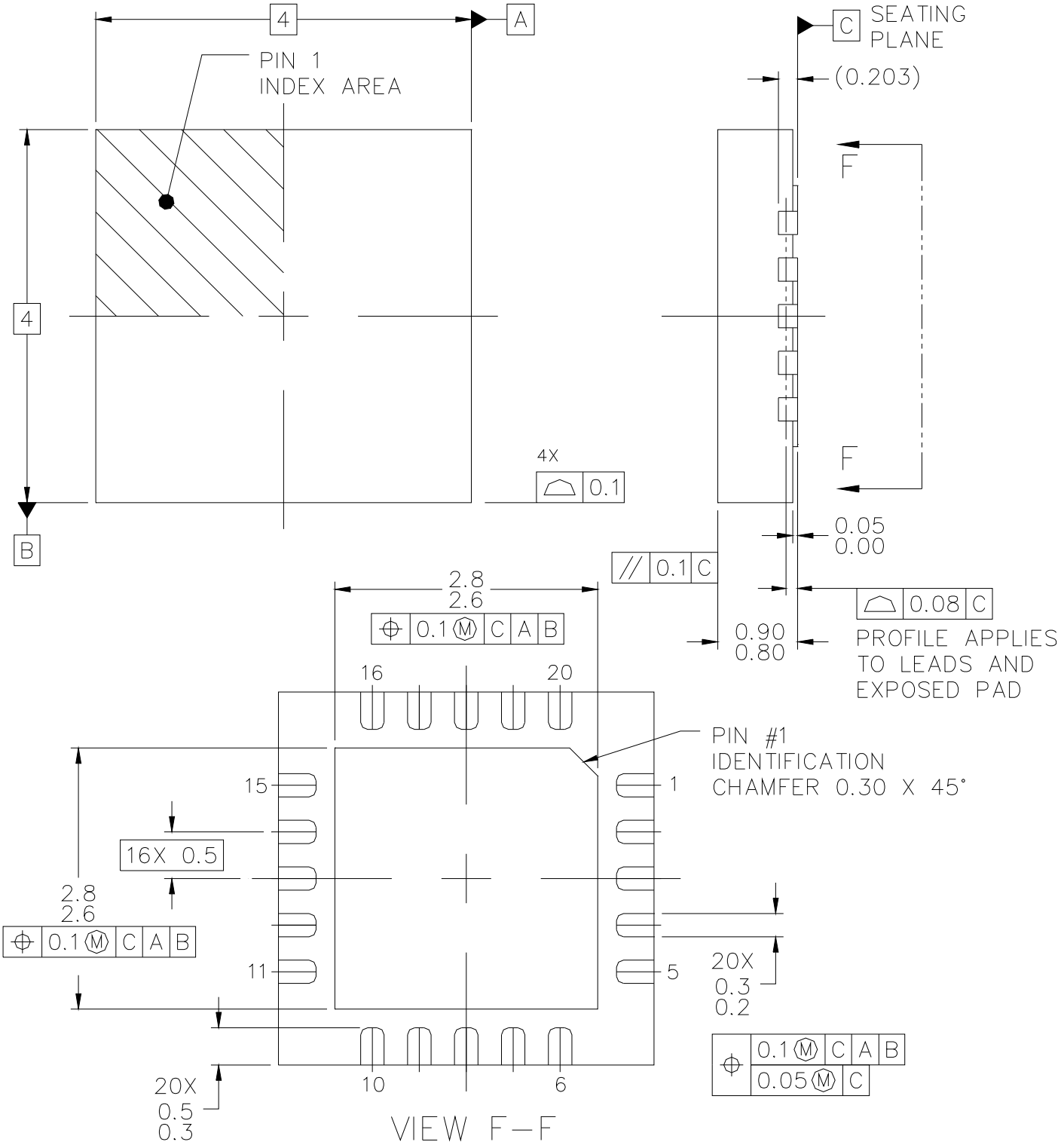
Bias-down Procedure

Turn off RF supply

Reduce VG 1, 2, VG3 to -1.5 V. Ensure Id ~ 0 mA

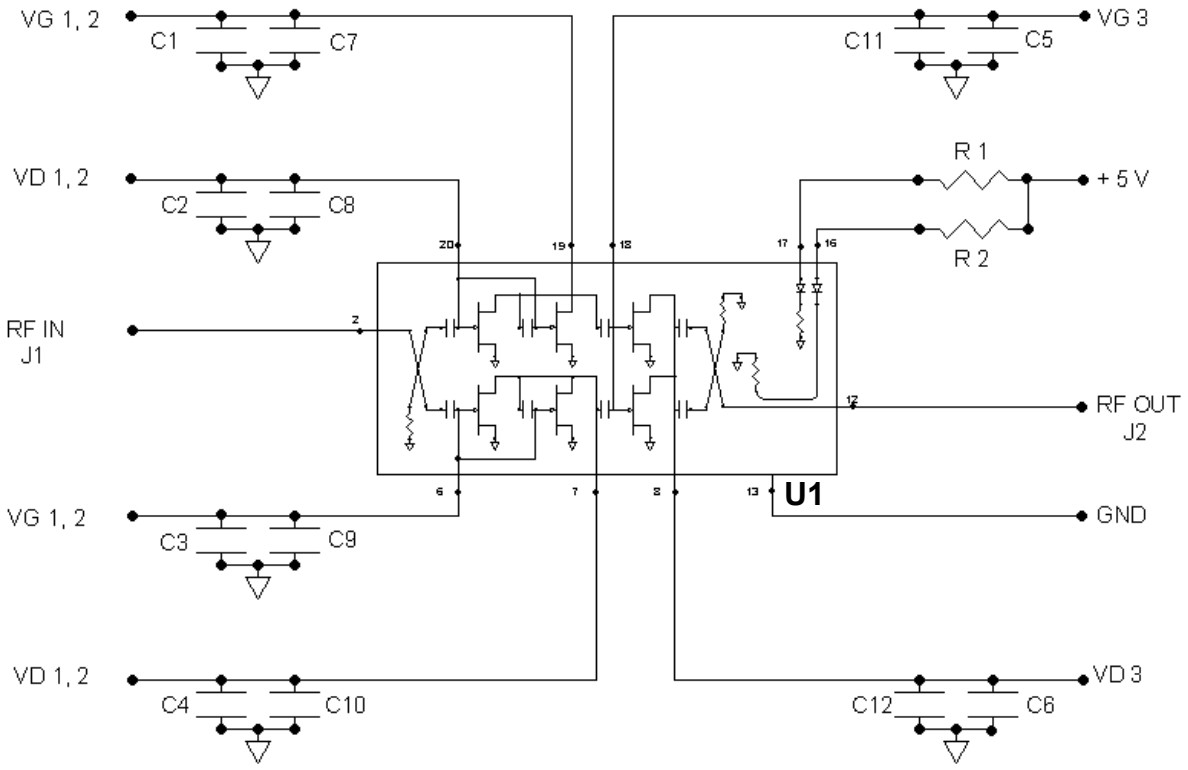
Turn VD 1, 2, VD 3 to 0 V

Turn VG 1, 2, VG 3 to 0 V



GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Recommended Application Circuit



Ref Designator	Value	Description
U1	--	TriQuint TGA2522-SM
C1, C2, C3, C4, C5, C6	1.0 μF	1206 SMT Ceramic Capacitor
C7, C8, C9, C10, C11, C12	0.01 μF	0603 SMT Ceramic Capacitor
J1, J2	1092-01A-5	Southwest Microwave End Launch Connector
R1, R2	240 KΩ	External Resistor

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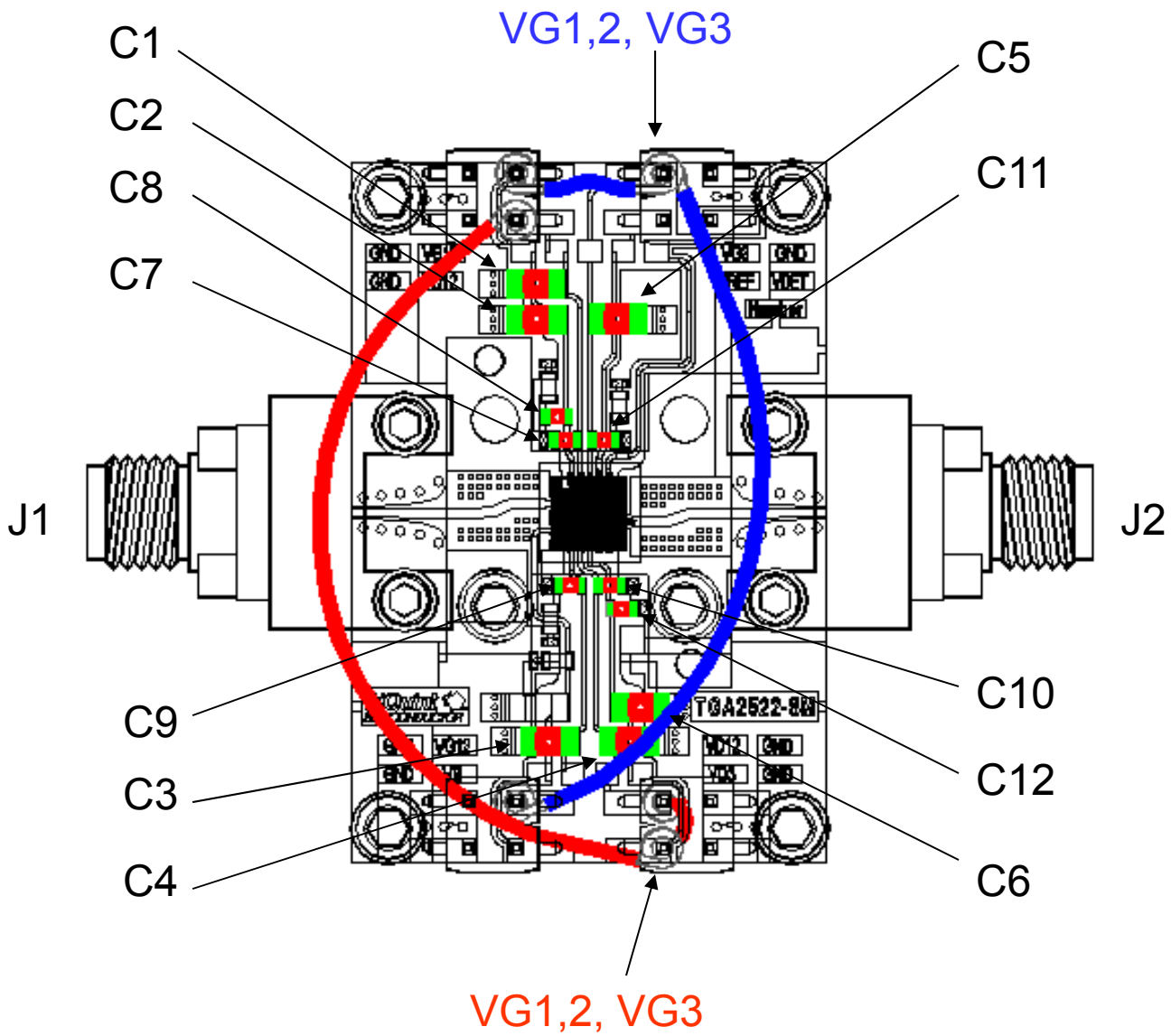
Recommended Evaluation Board



Board Material: 10 mil thick Rogers 4350, ε_r = 3.5

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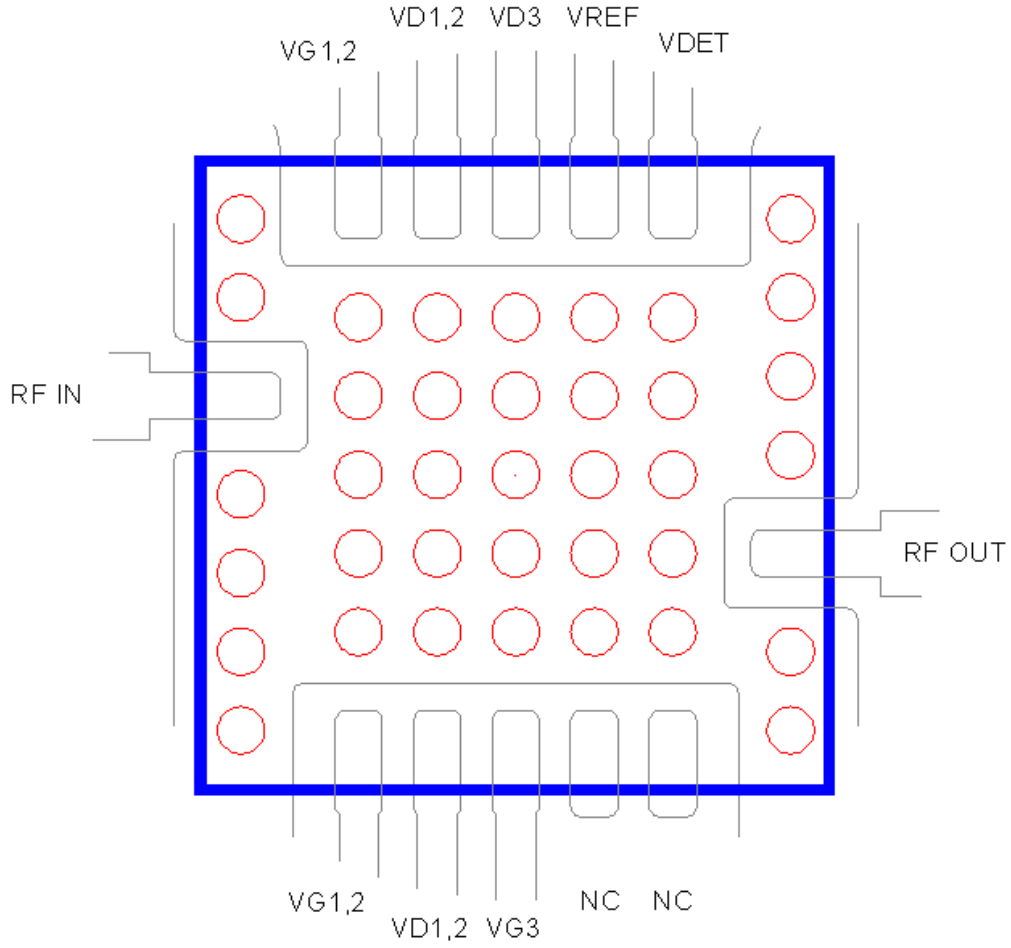
Recommended Land Pattern



Board Material: 10 mil thick Rogers 4350

Open Plated Vias in Center of Land pattern; Vias are 12 mil Diameter, 20 mil center-to-center spacing

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Assembly Notes

Recommended Surface Mount Package Assembly

- Proper ESD precautions must be followed while handling packages.
- Clean the board with acetone. Rinse with alcohol. Allow the circuit to fully dry.
- TriQuint recommends using a conductive solder paste for attachment. Follow solder paste and reflow oven vendors' recommendations when developing a solder reflow profile. Typical solder reflow profiles are listed in the table below.
- Hand soldering is not recommended. Solder paste can be applied using a stencil printer or dot placement. The volume of solder paste depends on PCB and component layout and should be well controlled to ensure consistent mechanical and electrical performance.
- Clean the assembly with alcohol.

Reflow Profile	SnPb	Pb Free
Ramp-up Rate	3 °C/sec	3 °C/sec
Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C	60 – 180 sec @ 150 – 200 °C
Time above Melting Point	60 – 150 sec	60 – 150 sec
Max Peak Temperature	240 °C	260 °C
Time within 5 °C of Peak Temperature	10 – 20 sec	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec	4 – 6 °C/sec

Ordering Information

Part	Package Style
TGA2522-SM, TAPE AND REEL	4 x 4 mm QFN Surface Mount, TAPE AND REEL

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Mouser Electronics

Authorized Distributor

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TGA2522-SM-T/R