FAIRCHILD
SEMICONDUCTOR®

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FSAL200
Wide Bandwidth Quad 2:1 Analog Multiplexer/Demultiplexer Switch

General Description

The Fairchild Switch FSAL200 is a rail-to-rail quad 2:1 high-speed CMOS TTL-compatible analog multiplexer/demultiplexer switch. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When $\overline{OE}$ is LOW, the select pin connects the A Port to the selected B Port output. When $\overline{OE}$ is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

■ Typical 6Ω switch connection between two ports
■ Minimal propagation delay through the switch
■ Low I_{CC}
■ Zero bounce in flow-through mode
■ Control inputs compatible with TTL level
■ Rail-to-rail signal handling
■ Low insertion loss
■ Route communications signals including:
   10/100 Ethernet
   USB1.1
   100VG-AnyLAN
   Token Ring 4/16 Mbps
   ATM25
   SONET OCI 51.8 Mbps
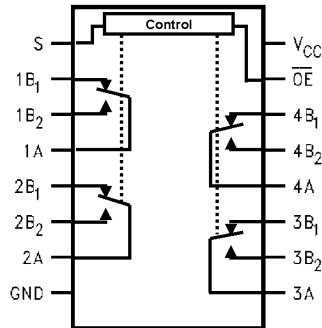   T1/E1

Ordering Code:

Order Number	Package Number	Package Description
FSAL200QSC	MQA16	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
FSAL200MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

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FSAL200

Analog Symbol

Connection Diagram

Pin Assignments for TSSOP and QSOP

Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	$A = B_1$
H	L	$A = B_2$
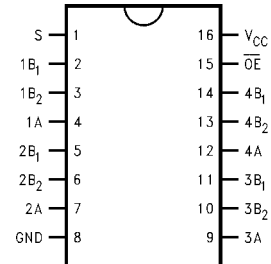
Pin Descriptions

Pin Name	Description
$\overline{OE}$	Switch Enable
S	Select Input
A, B_1, B_2	Data Port

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−0.5V to V_{CC} +0.5V
DC Input Voltage (V_{IN}) (Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
@ (I_{IK}) V_{IN} < 0V	−50 mA
DC Output Current (I_{OUT})	120 mA
DC V_{CC} or Ground Current (I_{CC}/I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) @ +85°C	0.5 W
Ambient Temperature with	
Power Applied	−40°C to +85°C

Recommended Operating Conditions (Note 3)

Supply Voltage Operating (V_{CC})	3.0V to 5.5V
Control Input Voltage (V_{IN})	0V to V_{CC}
Switch Input Voltage (V_{IN})	0V to V_{CC}
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
Control Input V_{CC} = 2.3V - 3.6V	0 ns/V to 10 ns/V
Control Input V_{CC} = 4.5V - 5.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	350°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Control input must be held HIGH or LOW, it must not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C			Units	Conditions
			Min	Typ	Max		
V_{IH}	HIGH Level Input Voltage	4.5 - 5.5	2.0			V	
		3.0 - 3.6	2.0				
V_{IL}	LOW Level Input Voltage	4.5 - 5.5	−0.5		0.8	V	
		3.0 - 3.6	−0.5		0.8		
I_{OZ}	OFF State Leakage Current	0 − 5.5			100	nA	$0 \le V_{IN} \le 5.5V$
R_{ON}	Switch On Resistance	4.5 - 5.5		6	12	Ω	I_{ON} = 10 - 30 mA
	(Note 4)	3.0 - 3.6		15	22		I_{ON} = 10 - 30 mA
I_{IN}	Control Input Leakage Current	5.5			±1	µA	$V_{IN} = V_{CC}$ or GND
		3.6			±1		$V_{IN} = V_{CC}$ or GND
I_{CC}	Quiescent Supply Current All Channels ON or OFF	5.5			1	µA	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0
	Analog Signal Range	V_{CC}	0		V_{CC}	V	
ΔR_{ON}	On Resistance Match Between	4.5 - 5.5		0.4	2	Ω	I_A = −30 mA, V_{Bn} = 3.15
	Channels (Note 4)(Note 5)	3.0 - 3.6		1	3		I_A = −10 mA, V_{Bn} 2.1
I_O	Output Current	4.5 - 5.5	100			mA	B_n, B_n, S = 0V to 5V
		3.0 - 3.6	80				
R_{flat}	On Resistance Flatness	4.5 - 5.5		3		Ω	A, B_1, B_2 = 0V to 5V
	(Note 4)(Note 6)	3.0 - 3.6		7			A, B_1, B_2 = 0V to 5V

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

Note 5: $\Delta R_{ON} = R_{ON}$ max − R_{ON} min measured at identical V_{CC}, temperature and voltage levels.

Note 6: Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

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FSAL200

AC Electrical Characteristics

Symbol	Parameter	V_CC (V)	$T_A = -40°C$ to $+85°C$ Min	Typ	Max	Units	Conditions	Figure Number
t_{ON}	Turn On Time	4.5 – 5.5		10	20	ns	$VB_n = 3V$	Figures 1, 2
	S to Output	3.0 - 3.6		28	40	ns	$VB_n = 1.5V$	
t_{OFF}	Turn Off Time	4.5 – 5.5		5	10	ns	$VB_n = 3V$	Figures 1, 2
	S to Output	3.0 - 3.6		4	20	ns	$VB_n = 1.5V$	
Q	Charge Injection	5.0		7		pC	$C_L = 0.1$ nF, $V_{GEN} = 0V$	Figure 3
	(Note 7)	3.3		3			$R_{GEN} = 0\ \Omega$	
OIRR	Off Isolation	4.5 - 5.5		−55		dB	$R_L = 100\ \Omega$ $f = 30$ MHz	Figure 4
	(Note 8)	3.0 - 3.6		−75		dB	$R_L = 50\ \Omega$ $f = 1$ MHz	Figure 4
Xtalk	Crosstalk	4.5 - 5.5		−70		dB	$R_L = 100\ \Omega$ $f = 30$ MHz	Figure 5
		3.0 - 3.6		−75		dB	$R_L = 50\ \Omega$ $f = 1$ MHz	Figure 5
BW	−3dB Bandwidth	4.5 - 5.5		137		MHz	$R_L = 100\ \Omega$	Figure 8
		3.0 - 3.6		110		MHz	$R_L = 50\ \Omega$	Figure 8
D	$\Delta R_{ON/RL}$ Distortion	4.5 - 5.5		2		%	$R_L = 100\ \Omega$	
	(Note 7)	3.0 - 3.6		3				

Note 7: Guaranteed by Design.

Note 8: Off Isolation = $20 \log_{10} [V_A / V_{Bn}]$

Capacitance (Note 9)

Symbol	Parameter	Typ	Max	Units	Conditions	Figure Number
C_{IN}	Control Pin Input Capacitance	2.3		pF	$V_{CC} = 0V$	
C_{IO-B}	B Port Off Capacitance	12		pF	$V_{CC} = 5.0V$ and 3.0V	Figure 6
	A Port Off Capacitance	20		pF	$V_{CC} = 5.0V$ and 3.0V	Figure 7
C_{ON}	Channel On Capacitance	15		pF	$V_{CC} = 5.0V$ and 3.0V	Figure 7

Note 9: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested in production.
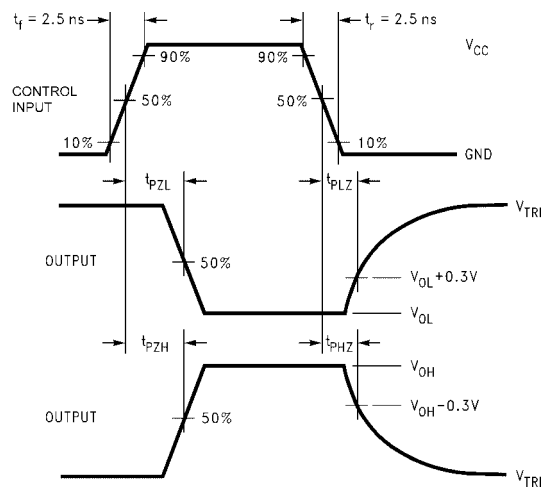
AC Loading and Waveforms

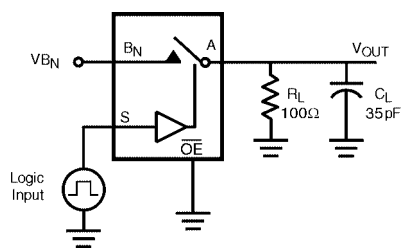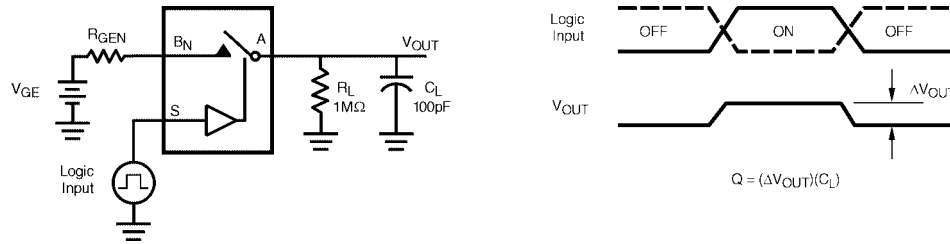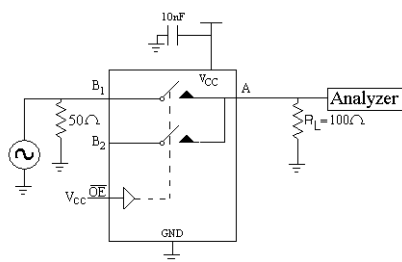**FIGURE 1. AC Waveforms**

FIGURE 2. t_{ON}, t_{OFF} Loading
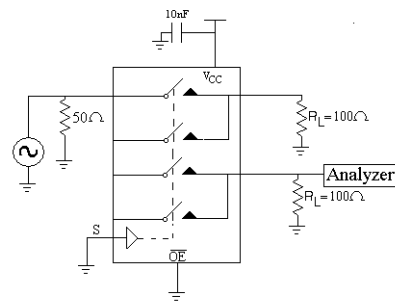
AC Loading and Waveforms (Continued)
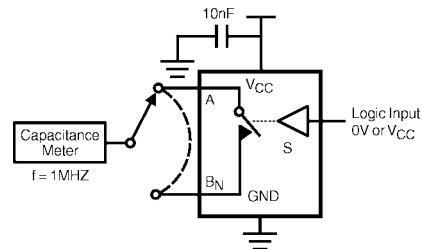

FIGURE 3. Charge Injection Test

Note: $R_L = 50\ \Omega$ when $V_{CC} = 3.3\pm10\%$ for the Off Isolation, Crosstalk and Bandwidth test.
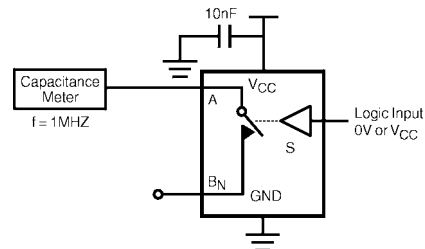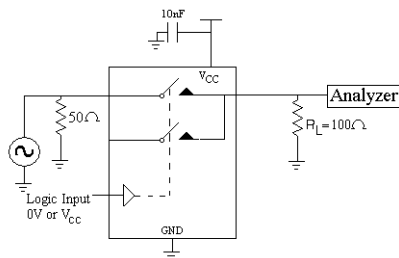

FIGURE 4. Off Isolation

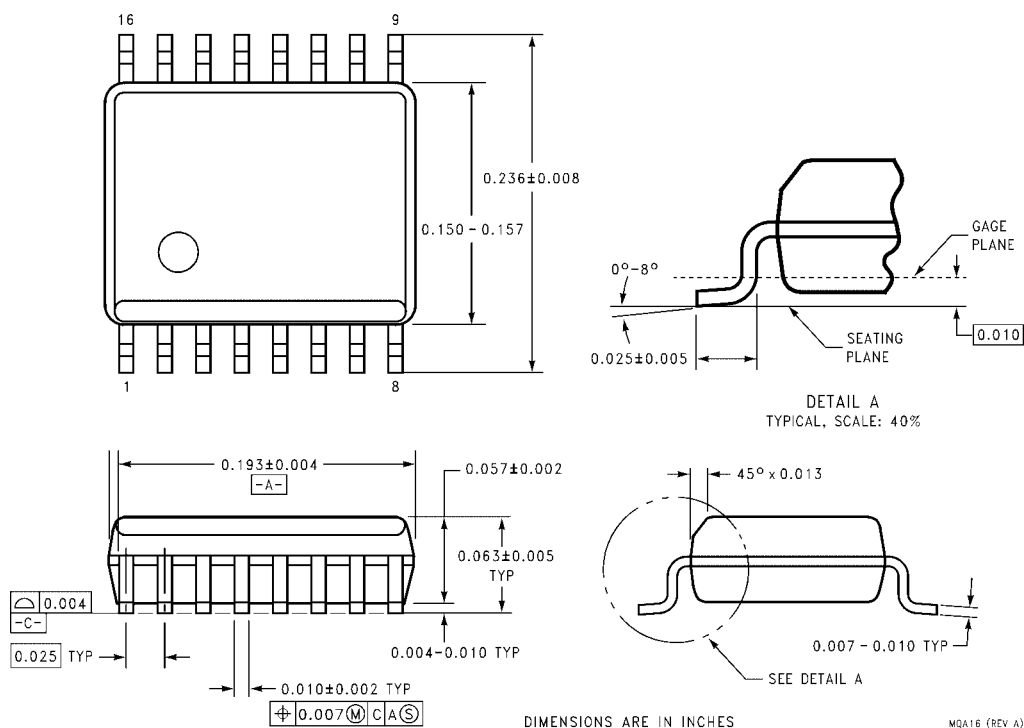**FIGURE 5. Crosstalk**

FIGURE 6. Channel Off Capacitance

FIGURE 7. Channel On Capacitance

FIGURE 8. Bandwidth

Physical Dimensions inches (millimeters) unless otherwise noted

16   9

0.236±0.008

0.150 - 0.157

1   8

0°-8°

GAGE
PLANE

0.025±0.005

SEATING
PLANE

0.010

DETAIL A
TYPICAL, SCALE: 40%

0.193±0.004
-A-

0.057±0.002

0.063±0.005
TYP

0.004

-C-

0.025 TYP

0.004-0.010 TYP

0.010±0.002 TYP

⊕ 0.007 Ⓜ C A Ⓢ

45° x 0.013

0.007 - 0.010 TYP

SEE DETAIL A

DIMENSIONS ARE IN INCHES

MQA16 (REV A)

**16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS METRIC ONLY

7.72 TYP.
4.16 TYP.
(1.78 TYP)
0.42 TYP
0.65 TYP

LAND PATTERN RECOMMENDATION

5.0 ± 0.1
-A-
16   9

6.4

4.4 ± 0.1
-B-

3.2

1   8   0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

GAGE PLANE
0.25

0°-8°   SEATING PLANE
0.6 ± 0.1

DETAIL A
TYPICAL, SCALE: 40X

0.1 C
ALL LEAD TIPS

SEE DETAIL A

(0.90)

-C-   1.1 MAX TYP

0.65 TYP

0.10 ± 0.05 TYP

0.09-0.20 TYP

0.19 - 0.30 TYP

0.13 M A B S C S

MTC16 (REV C)
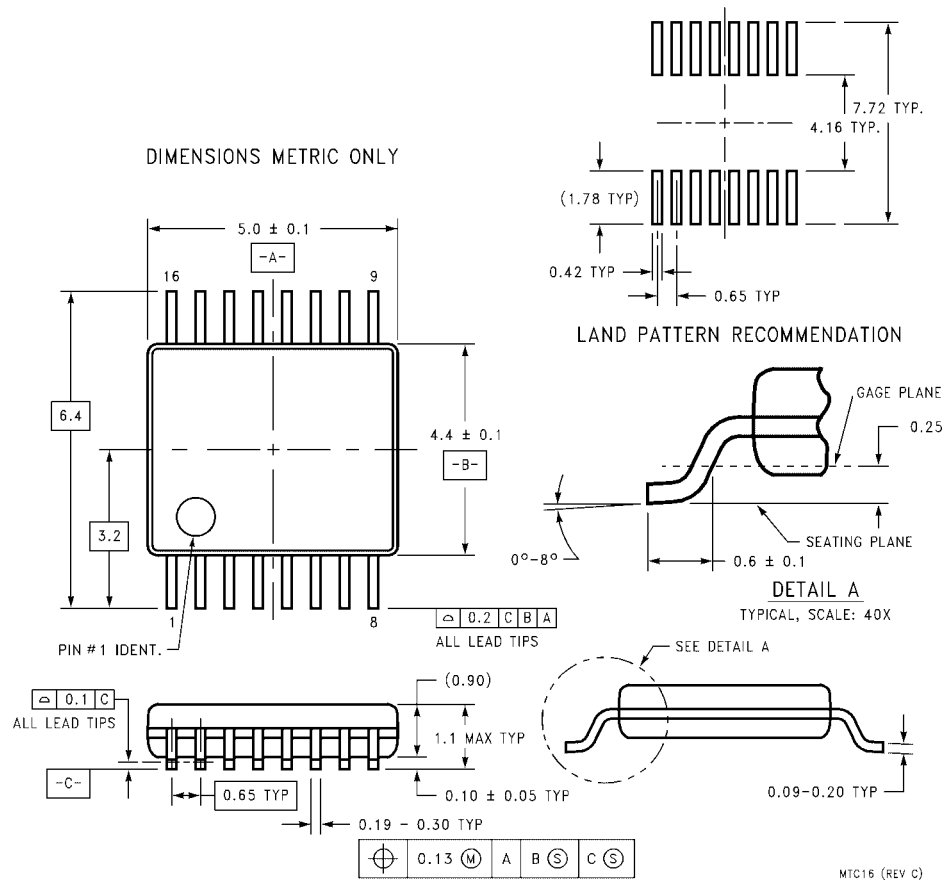
16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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