ACPL-32JT

Automotive 2.5 Amp Gate Drive Optocoupler with Integrated Flyback Controller for Isolated DC-DC Converter, Integrated IGBT Desat Overcurrent Sensing, Miller Current Clamping and UVLO Feedback

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

Avago's Automotive 2.5 Amp Gate Drive Optocoupler features integrated flyback controller for isolated DC-DC converter, IGBT desaturation sensing and fault feedback, Under-Voltage LockOut (UVLO) with soft-shutdown and fault feedback and active Miller current clamping. The fast propagation delay with excellent timing skew performance enables excellent timing control and efficiency. This full feature optocoupler comes in a compact, surface-mountable SO-16 package for space-savings, is suitable for traction power train inverter, power converter, battery charger, air-conditioner and oil pump motor drives in HEV and EV applications.

Avago R^{2}Coupler isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

Functional Diagram

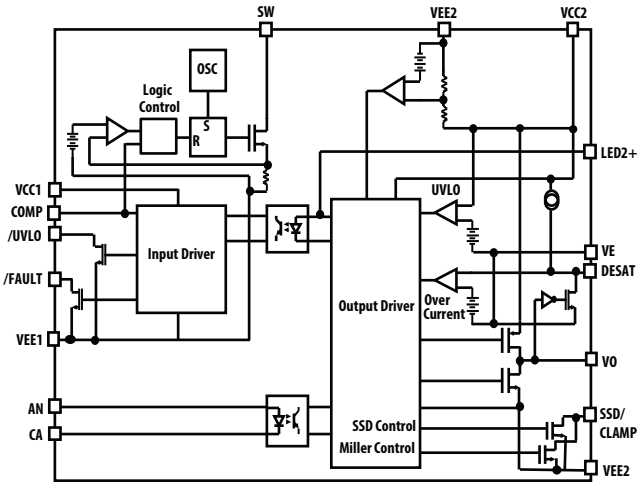


Figure 1. ACPL-32JT Functional Diagram

Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: -40 °C to +125 °C
- Integrated flyback controller for isolated DC-DC converter
- Regulated Output Voltage: 20 V
- Peak output current: 2.5 A max.
- Miller Clamp Sinking Current: 1.7 A max.
- Wide Input Voltage Range: 8 V to 18 V
- Common-Mode Rejection (CMR): > 30 kV/µs at V_{CM} = 1500 V
- Propagation delay: 250 ns max.
- Integrated fail-safe IGBT protection
  - Desat sensing, "Soft" IGBT turn-off and Fault Feedback
  - Under Voltage Lock-Out (UVLO) protection with Feedback
- High Noise Immunity
  - Miller Current Clamping
  - Direct LED input with low input impedance and low noise sensitivity
  - Negative Gate Bias
- SO-16 package with 8 mm clearance and creepage
- Regulatory approvals:
  - UL 1577, CSA
  - IEC/EN/DIN EN 60747-5-5

Applications

- Automotive Isolated IGBT/MOSFET Inverter gate drive
- Automotive DC-DC Converter
- AC and brushless DC motor drives
- Hybrid and Plug-in hybrid powertrain inverter
- Uninterruptible Power Supplies (UPS)

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.*

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-32JT	-000E	SO-16	X		X	45 per tube
ACPL-32JT	-500E		X	X	X	850 per reel

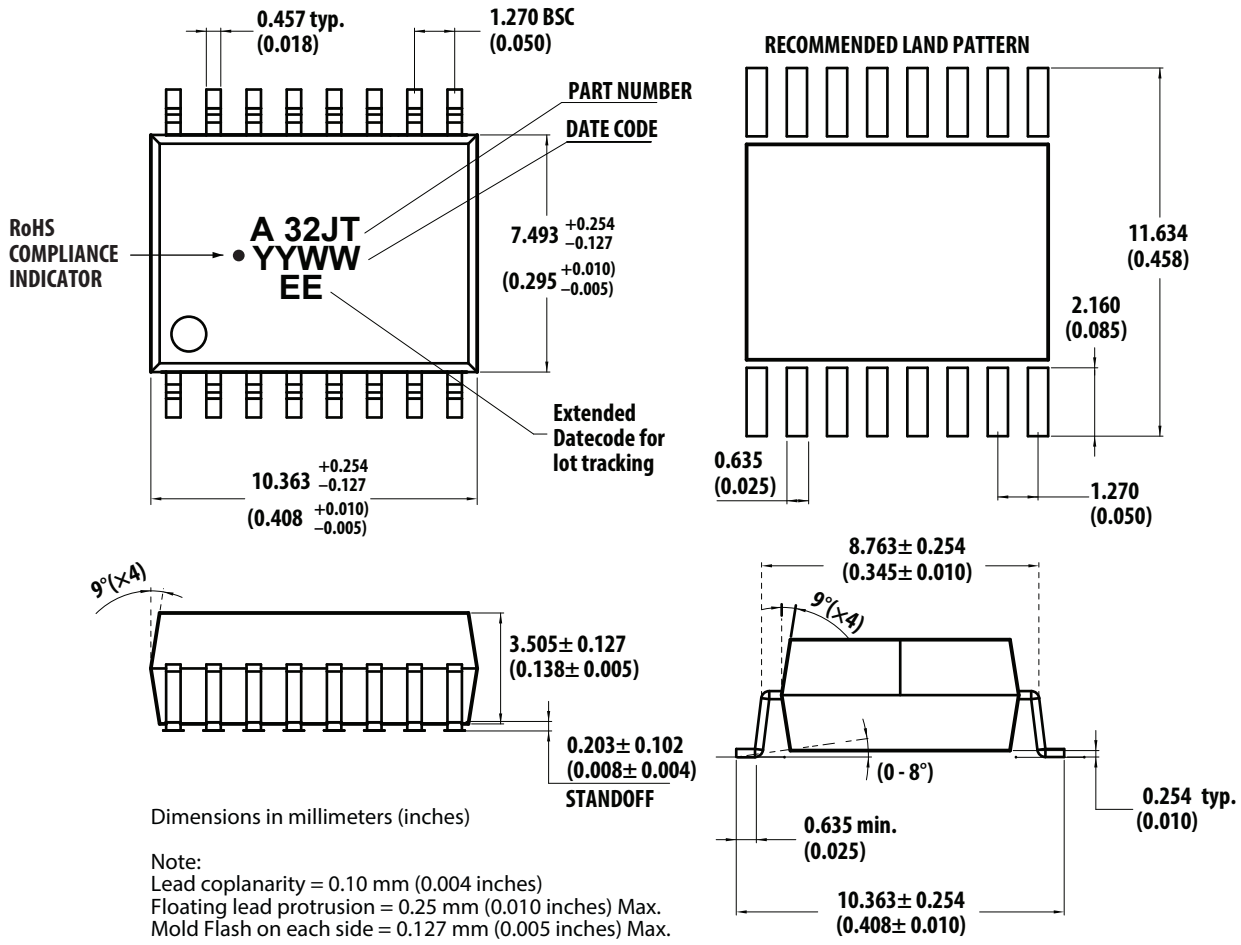
To order, choose a part number from the Part Number column and combine with the desired option from the Option column to form an order entry.

Example:

ACPL-32JT-500E to order product of SO-16 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval that is RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawing (16-Lead Surface Mount)



Dimensions in millimeters (inches)

Note:
Lead coplanarity = 0.10 mm (0.004 inches)
Floating lead protrusion = 0.25 mm (0.010 inches) Max.
Mold Flash on each side = 0.127 mm (0.005 inches) Max.

Recommended Lead-free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Non-halide flux should be used.

Product Overview Description

The ACPL-32JT (shown in Figure 1) is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit. It features a flyback controller for isolated DC-DC converter, a high current gate driver, Miller current clamping, IGBT desaturation, Under-Voltage Lock-Out (UVLO) protection, and feedback in a SO-16 package. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increases its noise immunity.

Package Pin Out

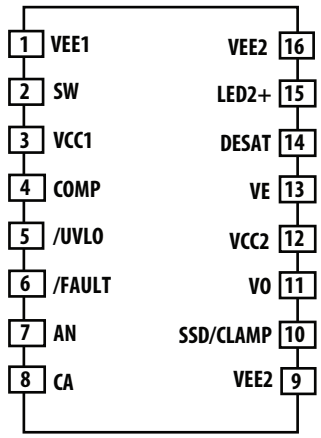


Figure 2. Pinout of ACPL-32JT

Pin Description

Pin Name	Function	Pin Name	Function
V_{EE1}	Input IC common	V_{EE2}	Output IC common and negative power supply reference to IGBT Emitter
SW	Switch Output to Primary Winding	LED2+	No connection, for testing only
V_{CC1}	Input power supply	DESAT	Desat overcurrent sensing
COMP	Compensation network for Flyback Controller	V_E	IGBT emitter reference
/UVLO	V_{CC2} under voltage lock out feedback	V_{CC2}	Positive power supply
/FAULT	Overcurrent fault feedback	V_O	Driver output to IGBT gate
AN	Input LED anode	SSD/CLAMP	Soft shutdown sensing/Miller current clamping output. (For proper functionality, this pin must be connected to the gate of the IGBT directly or through a current buffer.)
CA	Input LED cathode	V_{EE2}	Negative power supply

Typical Application/Operation

Introduction to Fault Detection and Protection

The power stage of a typical three-phase inverter is susceptible to several types of failures, most of which are potentially destructive to the power IGBTs. These failure modes can be grouped into four basic categories: phase or rail supply short circuits due to user misconnect or bad wiring; control signal failures due to noise or computational errors; overload conditions induced by the load; and component failures in the gate drive circuitry. Under any of these fault conditions, the current through the IGBTs can increase rapidly, causing excessive power dissipation and heating. The IGBTs become damaged when the current load approaches the saturation current of the device, and the collector-to-emitter voltage rises above the saturation voltage level. The drastically increased power dissipation very quickly overheats the power device and destroys it. To prevent damage to the drive, fault protection must be implemented to reduce or turn off the overcurrent during a fault condition.

A circuit providing fast local fault detection and shutdown is an ideal solution, but the number of required components, board space consumed, cost, and complexity have until now limited its use to high performance drives. The features that this circuit must have are high speed, low cost, low resolution, low power dissipation, and small size.

The ACPL-32JT satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shutdown, and optically isolated fault and UVLO status feedback signal into a single 16-pin surface mount package.

The fault detection method, which the ACPL-32JT has adopted, is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off-state of the IGBT, the fault detect circuitry is simply disabled to prevent false 'fault' signals.

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the ACPL-32JT limits the power dissipation in the IGBT, even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly- conservative overcurrent threshold is not needed to protect the IGBT.

Recommended Application Circuit

The ACPL-32JT has non-inverting gate control inputs, an open collector fault, and UVLO outputs suitable for wired 'OR' applications.

The recommended application circuit shown in Figure 3 illustrates a typical gate drive implementation using the ACPL-32JT.

The two supply bypass capacitors (1.0 μF or larger) provide the large transient currents necessary during a switching transition. The Desat diode and 220 pF blanking capacitor are the necessary external components for the fault detection circuitry. The gate resistor (10 Ω) serves to limit gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open collector fault and UVLO outputs have a passive 10 kΩ pull-up resistor and a 330 pF filtering capacitor.

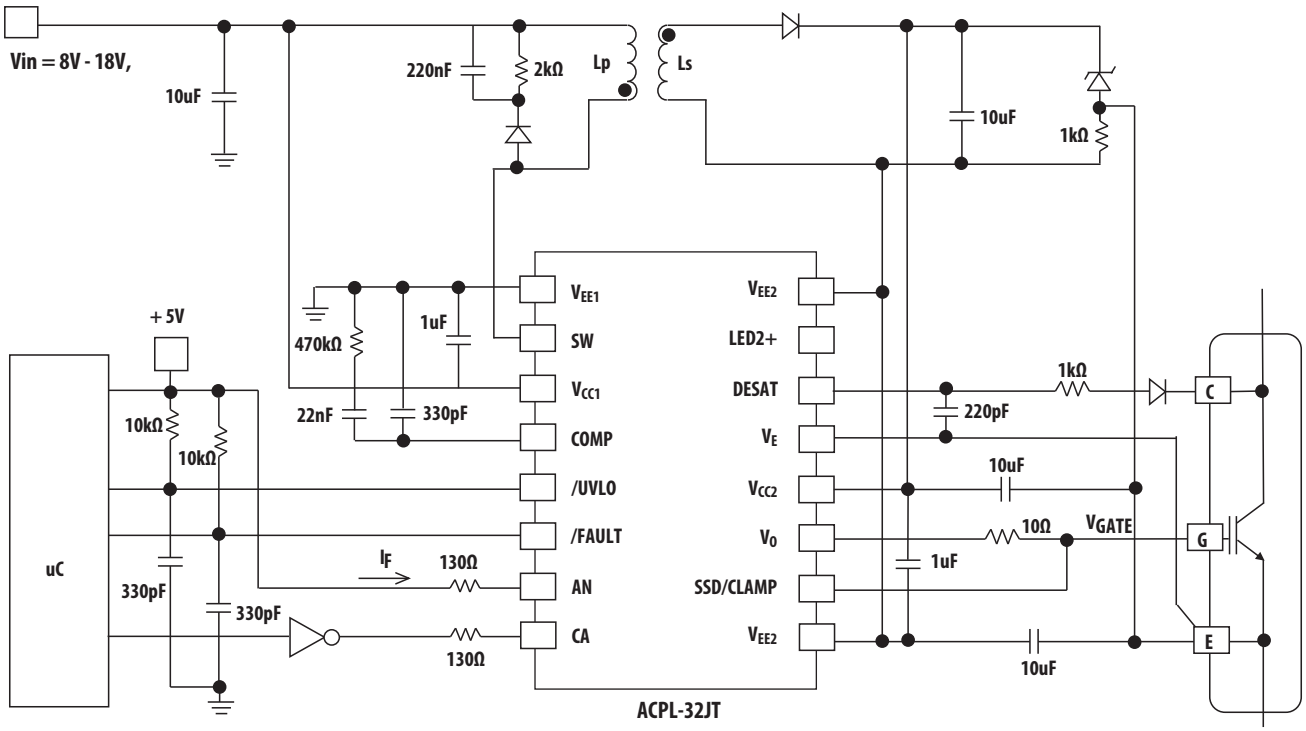


Figure 3. Typical gate drive circuits with Desat current sensing using ACPL-32JT

Note. Component value subject to change with varying application requirements

Operation of Integrated Flyback Controller

The primary control block implements direct duty cycle control logics for line and load regulation. Primary winding currents are sensed and limited to prevent transformer short circuit failure from damaging the primary switch. Secondary output voltage V_{CC2} is also sensed and fed back to the primary control circuits. V_{CC2} over voltage can be detected and the primary switch is turned off to protect secondary overvoltage failure. The maximum PWM duty cycle is designed to be around 55% to ensure discontinuous operation mode under a high load condition. For a complete isolated DC-DC converter, connect a discrete transformer to ACPL-32JT, as in Figure 3. Keep the LED off when you are powering up V_{CC1}. To ensure proper operation of the DC-DC converter, a fast V_{CC1} rise time (≤ 5 ms) is preferred for a soft start function to control the inrush current.

The average PWM switching frequency of the primary switch (SW) is dithered typically in a range of ±6%. This frequency dithering feature helps to achieve better EMI performance by spreading the switching and its harmonics over a wider band.

Reference DC/DC circuit

Figure 3 shows a reference circuit for DC/DC flyback conversion including the compensation network at pin 4, COMP.

This compensation network is referenced to a nominal transformer of L_p = 60 µH, L_s=260 µH.

For V_{CC1} = 8 V to 18 V, this circuit will nominally support a secondary-side load of up to 60 mA (including I_{CC2}) at the regulated V_{CC2} voltage. For V_{CC1} = 6 V to 8V, the supported load will be up to 40 mA.

Users must further characterize the DC/DC flyback conversion across their target operating conditions and chosen components to ensure that the required load can be supported.

DESAT Fault Detection Blanking Time

After the IGBT is turned on, the DESAT fault detection circuitry must remain disabled for a short time period to allow the collector voltage to fall below the DESAT threshold. This time period, called the total DESAT blanking time, is controlled by the both internal DESAT blanking time $t_{DESAT(BLANKING)}$ and external blanking time, determined by the internal charge current, the DESAT voltage threshold, and the external DESAT capacitor.

The total blanking time is calculated in terms of internal blanking time ($t_{DESAT(BLANKING)}$), external capacitance (C_{BLANK}), FAULT threshold voltage (V_{DESAT}), and DESAT charge current (I_{CHG}) as

$$t_{BLANK} = t_{DESAT(BLANKING)} + C_{BLANK} \times V_{DESAT} / I_{CHG}$$

Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the LED current. When the LED current is driven high, ACPL-32JT can then deliver a 2.5 A sourcing current to drive the IGBT's gate. When the LED is switched off, the gate driver can provide a 2.5 A sinking current to quickly switch off the gate. The additional Miller clamping pull-down transistor is activated when the output voltage reaches about 2 V with respect to V_{EE2} to provide a low impedance path to the Miller current, as shown in Figure 6.

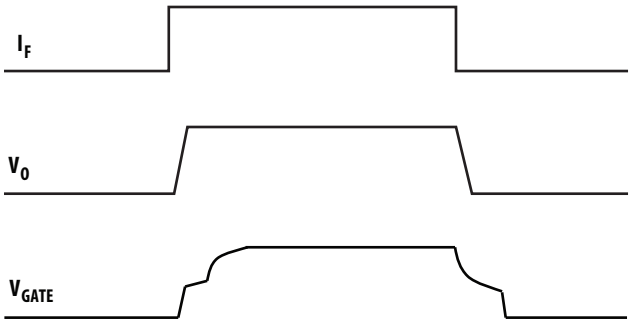


Figure 4. Gate Drive Signal Behavior

Description of Under Voltage Lock Out

Insufficient gate voltage to IGBT can increase turn on resistance of IGBT, resulting in large power loss and IGBT damage due to high heat dissipation. ACPL-32JT monitors the output power supply constantly. When output power supply is lower than under voltage lockout (UVLO) threshold gate driver output will shut off to protect IGBT from low voltage bias. During power up, the UVLO feature forces the ACPL-32JT's output low to prevent an unwanted turn-on at lower voltage.

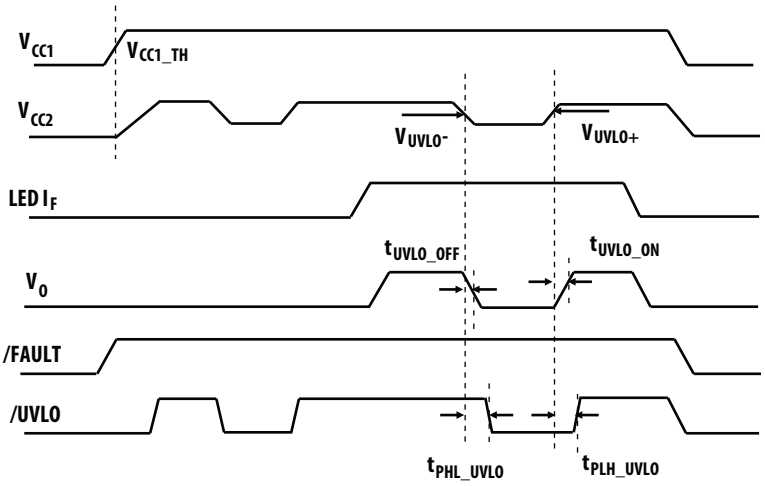


Figure 5. Circuit Behaviors at Power-up and Power down

Description of Over-Voltage Protection

If V_{CC2} is greater than the specified V_{CC2} OverVoltage Protection Threshold, then the transistor at the SW pin on the primary side will shut down and the DC/DC flyback conversion will stop.

During a Short Circuit:

1. DESAT terminal monitors IGBT's V_{CE} voltage.
2. When the voltage on the DESAT terminal exceeds 7 V, the IGBT gate voltage (V_{GATE}) is slowly lowered by soft shutdown pin SSD. Output driver V_O enters into high impedance state.
3. Output driver V_O ignores all PWM commands during mute time $t_{DESAT(MUTE)}$.
4. FAULT output goes Low, notifying the microcontroller of the fault condition.
5. Microcontroller takes appropriate action.
6. When $t_{DESAT(MUTE)}$ expires, the LED input needs to be kept Low for $t_{DESAT(RESET)}$ before fault condition can be cleared. FAULT status will return to High.
7. Output starts to respond to LED input after fault condition is cleared.

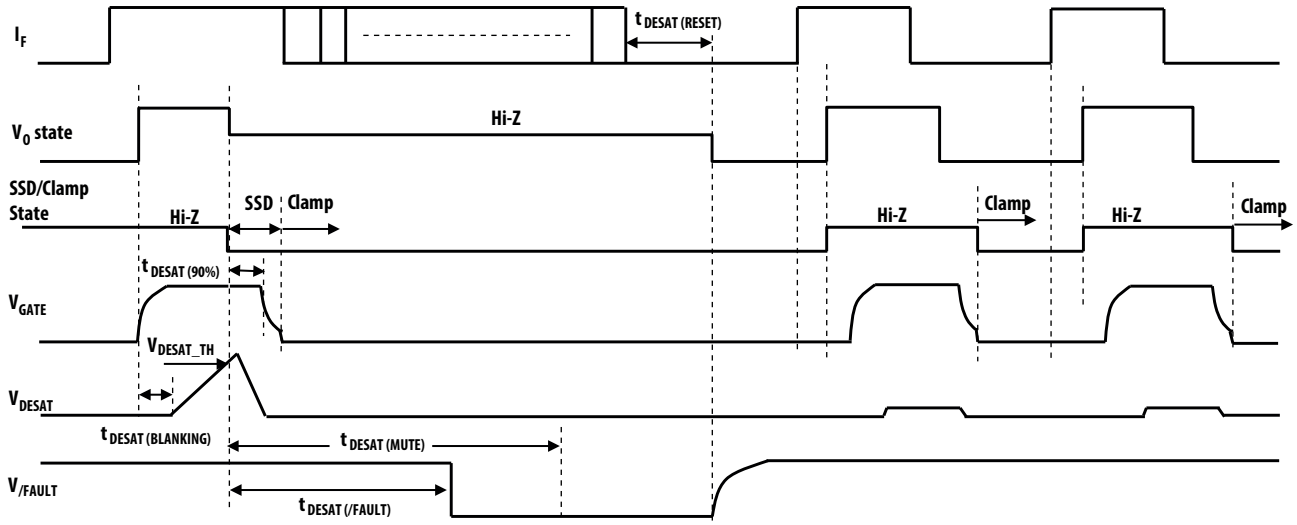


Figure 6. Circuit Behaviors During Desaturation Event

Regulatory Information

The ACPL-32JT is approved by the following organizations:

UL	CSA	IEC/EN/DIN EN 60747-5-5
Approved under UL 1577, component recognition program up to V_{ISO} = 5000 V_{RMS} expected before product release.	Approved under CSA Component Acceptance Notice #5, File CA 88324.	Approved under: IEC 60747-5-5: EN 60747-5-5: DIN EN 60747-5-5:

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol		Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	
for rated mains voltage ≤ 600 V_{rms}		I - IV	
for rated mains voltage ≤ 1000 V_{rms}		I - III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1230	V_{PEAK}
Input-to-Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	2306	V_{PEAK}
Input-to-Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test with t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	1968	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values – maximum values allowed in the event of a failure, (also see Figure 7)			
Case Temperature	Ts	175	°C
Input Power	$P_{S,INPUT}$	400	mW
Output Power	$P_{S,OUTPUT}$	1200	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$> 10^9$	Ω

Notes:
1. Isolation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits in the application. Surface mount classification is Class A in accordance with CECCOO802.
2. Refer to the Optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulation section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110)

Absolute Maximum Ratings

Unless otherwise specified, all voltages at input IC reference to V_{EE1}, all voltages at output IC reference to V_{EE2}.

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	150	°C	
Operating Temperature	T_A	-40	125	°C	1
IC Junction Temperature	T_J		150	°C	
Average Input Current	$I_{F(AVG)}$		20	mA	
Peak Transient Input Current (< 1 μs pulse width, 300 pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage (V_{CA}-V_{AN})	V_R		6	V	
Primary Switch Voltage	V_{SW}		36	V	
Input Supply Voltage	V_{CC1}	-0.5	26	V	33
/UVLO Pin Voltage	$V_{/UVLO}$	-0.5	6	V	
/Fault Pin Voltage	$V_{/FAULT}$	-0.5	6	V	
/Fault Output Current (Sinking)	$I_{/FAULT}$		10	mA	
/UVLO Output Current (Sinking)	$I_{/UVLO}$		10	mA	
Output Supply Voltage	V_{CC2} - V_{EE2}	-0.5	25	V	
Negative Output Supply Voltage	V_{EE2} - V_E	-10	0.5	V	2
Positive Output Supply Voltage	V_{CC2} - V_E	-0.5	25	V	
Gate Drive Output Voltage	$V_{o(peak)}$ - V_{EE2}	-0.5	V_{CC2}+0.5	V	
Miller Clamping Pin Voltage	V_{CLAMP} - V_{EE2}	-0.5	V_{CC2}+0.5	V	
Desat Voltage	V_{DESAT} - V_E	– 0.5	10	V	3
Peak Output Current	$\|I_{O(peak)}\|$		2.5	A	4
Output IC Power Dissipation	P_O		580	mW	1
Input IC Power Dissipation	P_I		180	mW	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Temperature	T_A	-40	125	℃	
Input IC Supply Voltage	V_{CC1}	8	18	V	5
Total Output IC Supply Voltage	$V_{CC2} – V_{EE2}$	18	22	V	6
Positive Output IC Supply Voltage	$V_{CC2} – V_E$	15	25		7
Negative Output IC Supply Voltage	V_{EE2}-V_E	-8	0		7
Input LED Turn on Current	$I_{F(ON)}$	10	16	mA	
Input LED Turn off Voltage (V_{AN}-V_{CA})	$V_{F(OFF)}$	-5.5	0.8	V	
PWM Duty Cycle	D_{MAX}		50	%	
Peak SW current	I_{SW_PK}		1.3	A	
Input pulse width	$t_{ON(LED)}$	500		ns	

Electrical Specifications

Unless otherwise specified, all Minimum/Maximum specifications are at recommended operating conditions, all voltages at input IC are referenced to V_{EE1}, all voltages at output IC referenced to V_{EE2}. All typical values at T_A = 25 °C, V_{CC1} = 12 V, V_{CC2}-V_{EE2} = 20 V, V_E-V_{EE2} = 0 V.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig.	Note
DCDC Flyback Converter								
PWM Switching Frequency	f_{PWM}	40	60	80	kHz			
Maximum PWM Duty Cycle	D		56		%		8	
V_{CC1} Turn-on Threshold	V_{CC1_TH}			6	V			
SW turn-on Resistance	R_{ON_SW}		0.9		Ω	I_{SW} = 1.3 A	9	
Regulated V_{CC2} Voltage	V_{CC2}	19	20	21.5	V	I_{COMP} = 0 A	10	
SW Overcurrent Protection Threshold	I_{SW_TH}		2		A			
V_{CC2} OverVoltage Protection Threshold	V_{OV_TH}		24		V			
IC Supply Current								
Input Supply Current	I_{CC1}		4.0	6.1	mA		11	
Output Low Supply Current	I_{CC2L}		10.5	13.2	mA	I_F = 0 mA V_{CC2} = 20 V	12	
Output High Supply Current	I_{CC2H}		10.6	13.6	mA	I_F = 10 mA V_{CC2} = 20 V	12	
Logic Input and Output								
LED Forward Voltage ($V_{AN} – V_{CA}$)	V_F	1.25	1.55	1.85	V	I_F = 10 mA	13	
LED Reverse Breakdown Voltage ($V_{CA} – V_{AN}$)	V_{BR}	6			V	I_F = -10 µA		
LED Input Capacitance	C_{IN}		90		pF			
LED Turn-on Current Threshold Low-to-High	I_{TH+}		2.4	6.6	mA	V_O = 5 V	14	
LED Turn-on Current Threshold High-to-Low	I_{TH-}		1.8	6.4	mA	V_O = 5 V	14	
LED Turn-on Current Hysteresis	I_{TH_HYS}		0.6		mA			
FAULT Logic Low Output Current	I_{FAULT_L}	4.0	9.0		mA	$V_{/FAULT}$ = 0.4 V		
FAULT Logic High Output Current	I_{FAULT_H}			20	µA	$V_{/FAULT}$ = 5 V		
UVLO Logic Low Output Current	I_{UVLO_L}	4.0	9.0		mA	$V_{/UVLO}$ = 0.4 V		
UVLO Logic High Output Current	I_{UVLO_H}			20	µA	$V_{/UVLO}$ = 5 V		

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Electrical Specifications (continued)

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Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig.	Note
Gate Driver								
High Level Output Current	I_{OH}		-1.9	-0.75	A	$V_O = V_{CC2}$ - 3 V	15	4
Low Level Output Current	I_{OL}	1.0	2.3		A	$V_O = V_{EE2}$ + 2.5 V	16	4
High Level Output Voltage	V_{OH}	V_{CC2}–0.5	V_{CC2}–0.15		V	I_O = -100 mA		8,9,10
Low Level Output Voltage	V_{OL}		0.1	0.5	V	I_O = 100 mA		
V_{source} to High Level Output Propagation Delay Time	t_{PLH}	50	120	250	ns	V_{source} = 5 V R_f = 260 Ω, R_g = 10 Ω C_{load} = 10 nF f = 10 kHz Duty Cycle = 50%	17,22	11
V_{source} to Low Level Output Propagation Delay Time	t_{PHL}	50	160	250	ns		17,22	12
Pulse Width Distortion	PWD	-40	40	140	ns			13,14
Dead Time Distortion (t_{PLH}-t_{PHL})	DTD	-160	-40	60	ns			14,15
10% to 90% Rise Time	t_R		70		ns			
90% to 10% Fall Time	t_F		35		ns			
Output High Level Common Mode Transient Immunity	$\|C_{MH}\|$	30	>50		kV/µs	T_A=25 °C, I_F = 10 mA, V_{CM} =1500 V	23	16
Output Low Level Common Mode Transient Immunity	$\|C_{ML}\|$	30	>50		kV/µs	T_A = 25 °C, I_F = 0 mA, V_{CM}=1500 V	24	17
Active Miller Clamp and Soft Shutdown								
Low Level Soft Shutdown Current During Fault Condition	I_{SSD}	22	35	55	mA	$V_{SSD} - V_{EE2}$ = 14 V	18	
Clamp Threshold Voltage	V_{TH_CLAMP}		2.0	3.0	V			
Clamp Low Level Sinking Current	I_{CLAMP}	0.5	2.0		A	$V_{CLAMP} = V_{EE2}$ + 2.5 V		
V_{CC2} UVLO Protection (UVLO voltage V_{UVLO} reference to V_E)								
V_{CC2} UVLO Threshold Low to High	V_{UVLO+}	10.9	12.5	13.8	V	V_O > 5 V		10,18
V_{CC2} UVLO Threshold High to Low	V_{UVLO-}	10.0	11.3	12.8	V	V_O < 5 V		10,19
V_{CC2} UVLO Hysteresis	V_{UVLO_HYS}		1.2		V			10
V_{CC2} to UVLO High Delay	t_{PLH_UVLO}		15		µs			20
V_{CC2} to UVLO Low Delay	t_{PHL_UVLO}		10.7		µs			21
V_{CC2} UVLO to V_{OUT} High Delay	t_{UVLO_ON}		5.3		µs			22
V_{CC2} UVLO to V_{OUT} Low Delay	t_{UVLO_OFF}		1.1		µs			23

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Electrical Specifications (continued)

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Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Fig.	Note
Desaturation Protection (Desat voltage V_{DESAT} reference to V_E)								
Desat Sensing Threshold	V_{DESAT}	6.2	7.0	7.8	V		19	10
Desat Charging Current	I_{CHG}	-1.1	-0.9	-0.65	mA	V_{DESAT} = 2 V	20	
Desat Discharging Current	I_{DSCHG}	20	53		mA	V_{DESAT} = 8 V	21	
V_{CC2} during fault condition	$V_{CC2(FAULT)}$		19		V			
I_{CC2} during fault condition	$I_{CC2(FAULT)}$		11.6		mA	V_{CC2} = 20 V		
Internal Desat Blanking Time	$t_{DESAT(BLANKING)}$	0.3	0.6	1.1	µs	C_{SSD}=10 nF		24
Desat Sense to 90% SSD Delay	$t_{DESAT(90\%)}$		0.6		µs			25
Desat Sense to 10% SSD Delay	$t_{DESAT(10\%)}$		6.0		µs			26
Desat to Low Level /FAULT Signal Delay	$t_{DESAT(/FAULT)}$			7.0	µs			27
Output Mute Time due to Desat	$t_{DESAT(MUTE)}$	2.3	3.2		ms			28
Time for Input Kept Low Before Fault Reset to High	$t_{DESAT(RESET)}$	2.3	3.2		ms			29

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			V_{RMS}	RH < 50%, t = 1 min. T_A = 25 °C	30, 31, 32
Resistance (Input-Output)	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 V_{DC}	32
Capacitance (Input-Output)	C_{I-O}		1.3		pF	f = 1 MHz	32
Thermal coefficient between LED and input IC	A_{EI}		35.4		°C/W		
Thermal coefficient between LED and output IC	A_{EO}		33.1		°C/W		
Thermal coefficient between input IC and output IC	A_{IO}		25.6		°C/W		
Thermal coefficient between LED and Ambient	A_{EA}		176.1		°C/W		
Thermal coefficient between input IC and Ambient	A_{IA}		92		°C/W		
Thermal coefficient between output IC and Ambient	A_{OA}		76.7		°C/W		

Notes:
1. Output IC power dissipation is derated linearly above 100 °C from 580 mW to 260 mW at 125 °C.
2. This supply is optional. Required only when negative gate drive is implemented.
3. Maximum 500 ns pulse width if peak V_{DESAT} > 10 V.
4. Maximum pulse width = 1 µs, maximum duty cycle = 1%.
5. In most applications V_{CC1} will be powered up first (before V_{CC2}) and powered down last (after V_{CC2}). This is desirable for maintaining control of the IGBT gate. In applications where V_{CC2} is powered up first, it is important to ensure that input remains low until V_{CC1} reaches the proper operating voltage to avoid any momentary instability at the output during V_{CC1} ramp-up or ramp-down.
6. 15 V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 13.5 V.
7. If DC-DC controller is not used for powering output IC.
8. For High Level Output Voltage testing, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero.
9. Maximum pulse width = 1.0 ms, maximum duty cycle = 20%.
10. Once V_{OUT} of the ACPL-32JT is allowed to go high (V_{CC2} - V_E > V_{UVLO}), the DESAT detection feature of the ACPL-32JT will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{CC2} exceeds V_{UVLO+} threshold, DESAT will remain functional until V_{CC2} is below V_{UVLO-} threshold. Thus, the DESAT detection and UVLO features of the ACPL-32JT work in conjunction to ensure constant IGBT protection.
11. t_{PLH} is defined as propagation delay from 50% of LED input I_F to 50% of High level output.
12. t_{PHL} is defined as propagation delay from 50% of LED input I_F to 50% of Low level output.
13. Pulse Width Distortion (PWD) is defined as (t_{PHL} – t_{PLH}) of any given unit.
14. As measured from I_F to V_O.
15. Dead Time Distortion (DTD) is defined as (t_{PLH} - t_{PHL}) between any two ACPL-32JT parts under the same test conditions.
16. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15 V). A 330 pF and a 10 kΩ pull-up resistor is needed in fault and UVLO detection mode.
17. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V). A 330 pF and a 10 kΩ pull-up resistor is needed in fault and UVLO detection mode.
18. This is the "increasing" (i.e. turn-on or "positive going" direction) of V_{CC2} - V_E.
19. This is the "decreasing" (i.e. turn-off or "negative going" direction) of V_{CC2} - V_E.
20. The delay time when V_{CC2} exceeds UVLO+ threshold to UVLO positive-going edge.
21. The delay time when V_{CC2} falls below UVLO- threshold to UVLO negative-going edge.
22. The delay time when V_{CC2} exceeds UVLO+ threshold to 50% of High level output.
23. The delay time when V_{CC2} falls below UVLO- threshold to 50% of Low level output.
24. The delay time for ACPL-32JT to respond to a DESAT fault condition without any external DESAT capacitor.
25. The amount of time from when DESAT threshold is exceeded to 90% of V_{GATE} at mentioned test conditions.
26. The amount of time from when DESAT threshold is exceeded to 10% of V_{GATE} at mentioned test conditions.
27. The amount of time from when DESAT threshold is exceeded to FAULT output Low – 50% of V_{CC1} voltage.
28. The amount of time when DESAT threshold is exceeded, Output is mute to LED input.
29. The amount of time when DESAT Mute time is expired, LED input must be kept Low for Fault status to return to High.
30. In accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second.
31. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.
32. Device considered a two-terminal device: pins 1 - 8 shorted together and pins 9 - 16 shorted together.
33. Max 34V, 10 pulses, 400ms pulse width, 60s intervals.

Thermal Characteristics are based on the ground planes layout of the evaluation PCB.

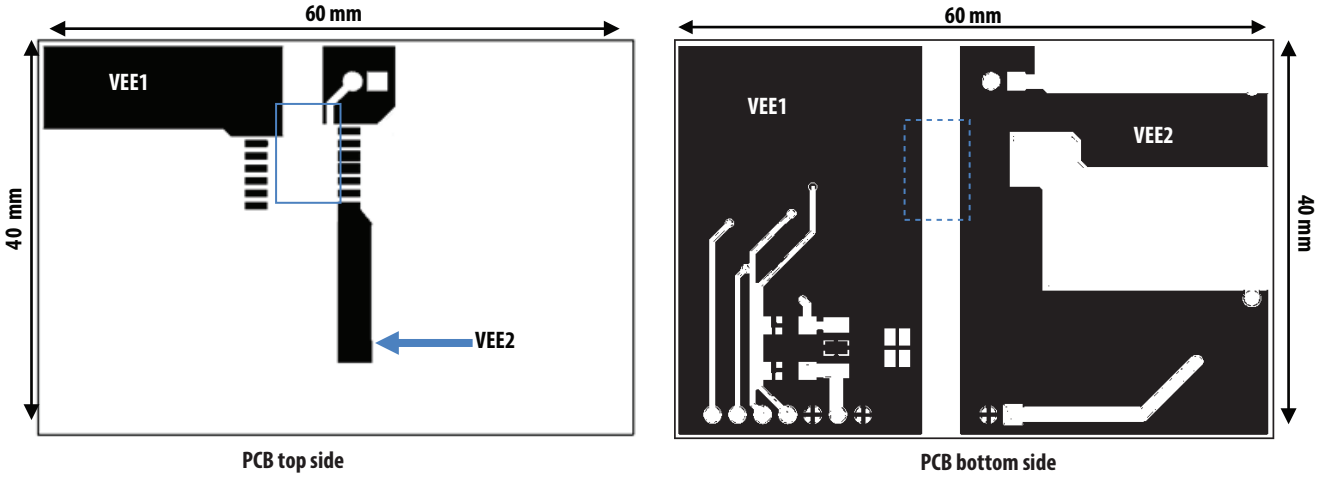


Figure 7. PCB Layout of evaluation board used for thermal characterization

Notes on Thermal Calculation

Application and environmental design for ACPL-32JT needs to ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler does not exceed 150 °C. The following equations are to calculate the maximum power dissipation and the corresponding effect on junction temperatures.

LED Junction Temperature = $A_{EA}*P_E + A_{EI}*P_I + A_{EO}*P_O + T_A$

Input IC Junction Temperature = $A_{EI}*P_E + A_{IA}*P_I + A_{IO}*P_O + T_A$

Output IC Junction Temperature = $A_{EO}*P_E + A_{IO}*P_I + A_{OA}*P_O + T_A$

P_E - LED Power Dissipation

P_I - Input IC Power Dissipation

P_O - Output IC Power Dissipation

Calculation of LED Power Dissipation

LED Power Dissipation, $P_E = I_{F(LED)}$ (Recommended Max) * $V_{F(LED)}$ (125 °C) * Duty Cycle

Example: $\mathbf{P_E}$ = 16 mA * 1.25 * 50% duty cycle = **10 mW**

Calculation of Input IC Power Dissipation

Input IC Power Dissipation, $P_I = P_{I(Static)} + P_{I(SW)}$

$P_{I(Static)}$ - static power dissipated by the input IC

$P_{I(SW)}$ - power dissipated in the SW pin due to switching current of primary winding of transformer. It is calculated based on averaging switching current and turn-on resistance of SW.

where

$P_{I(Static)} = I_{cc1} * V_{cc1}$

$P_{I(SW)} = I_{sw(avg)}^2 * R_{on\_sw}(125\ °C) = (I_{SW\_PK/2} * D_{max} * V_{in\_min}/V_{in})^2 * R_{on\_sw}(125\ °C)$

The highest input power dissipation is at minimum V_{in}, where the average current of SW pin is highest, $V_{in} = V_{CC1} = V_{IN(min)}$ = 8 V.

$P_{I(Static)}$ = 6 mA * 8 V = 48 mW

$P_{I(SW)} = (1.3\ A/2 * 50\% * 8V/8V)^2 * 0.9\ \Omega = 95$ mW

$P_I = P_{I(Static)} + P_{I(SW)}$ = 48 mW + 95 mW =143 mW

Calculation of Output IC Power Dissipation

Output IC Power Dissipation, $P_O = V_{CC2}$ (Recommended Max) * $I_{CC2\ (Max)} + P_{HS} + P_{LS}$

P_{HS} - High Side Switching Power Dissipation

P_{LS} - Low Side Switching Power Dissipation

$P_{HS} = (V_{CC2} * Q_G * f_{PWM}) * R_{OH(MAX)}/(R_{OH(MAX)} + R_{GH})/2$

$P_{LS} = (V_{CC2} * Q_G * f_{PWM}) * R_{OL(MAX)}/(R_{OL(MAX)} + R_{GL})/2$

Q_G – IGBT Gate Charge at Supply Voltage

f_{PWM} - LED Switching Frequency

$R_{OH(MAX)}$ – Maximum High Side Output Impedance - $V_{OH(MIN)}/I_{OH(MIN)}$

R_{GH} - Gate Charging Resistance

$R_{OL(MAX)}$ – Maximum Low Side Output Impedance - $V_{OL(MIN)}/I_{OL(MIN)}$

R_{GL} - Gate Discharging Resistance

Example:

$R_{OH(MAX)} = (V_{CC2}-V_{OH(MIN)})/I_{OH(MIN)} = 3.0\ V / 0.75\ A = 4.0\ \Omega$

$R_{OL(MAX)} = V_{OL(MIN)}/I_{OL(MIN)} = 2.5\ V / 1\ A = 2.5\ \Omega$

$P_{HS} = (20\ V * 1\ \mu C * 10\ kHz) * 4.0\ \Omega / (4.0\ \Omega + 10\ \Omega) / 2 = 28.5\ mW$

$P_{LS} = (20\ V * 1\ \mu C * 10\ kHz) * 2.5\ \Omega / (2.5\ \Omega + 10\ \Omega) / 2 = 20\ mW$

$P_O = 20\ V * 13.6\ mA + 25\ mW + 20\ mW = 320.5\ mW$

Calculation of Junction Temperature

LED Junction Temperature = 176.1 °C/W * 10 mW + 35.4 °C/W * 143 mW + 33.1 °C/W * 320.5 mW + T_A = **17.4 °C + T_A**

Input IC Junction Temperature = 35.4 °C/W * 10 mW + 92 °C/W * 143 mW + 25.6 °C/W * 320.5 mW + T_A = **21.7 °C + T_A**

Output IC Junction Temperature = 33.1 °C/W * 10 mW + 25.6 °C/W * 143 mW + 76.7 °C/W * 320.5 mW + T_A = **28.5 °C + T_A**

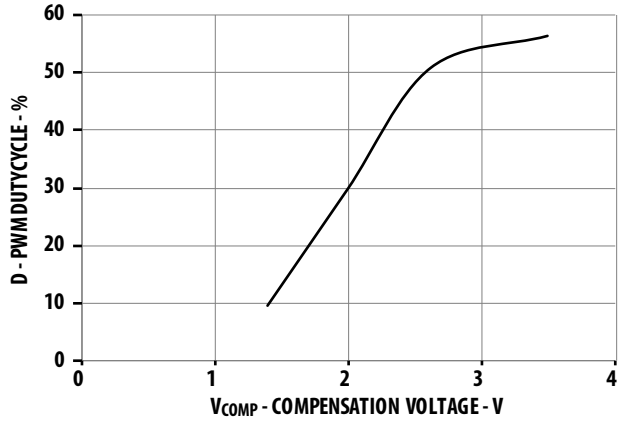


Figure 8. PWM Duty Cycle vs. V_{COMP}

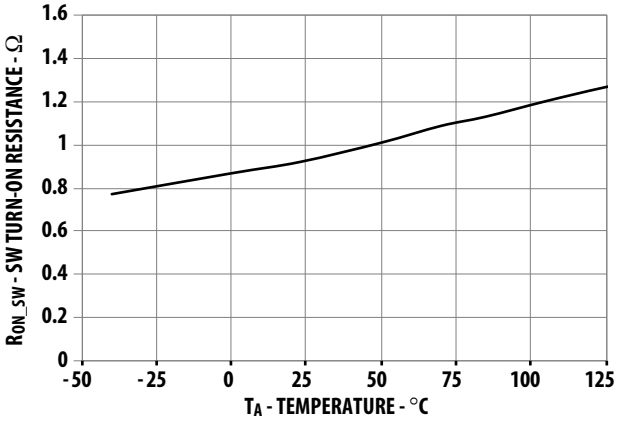


Figure 9. R_{ON_SW} vs. temperature

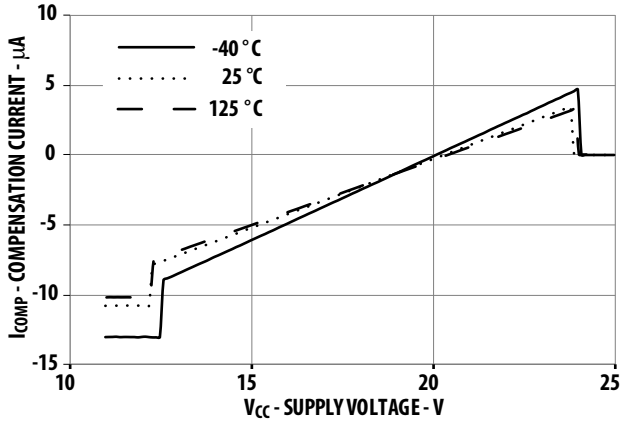


Figure 10. I_{COMP} vs. Supply Voltage

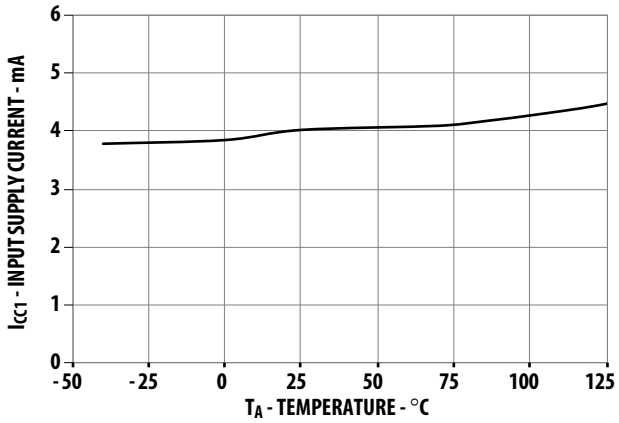


Figure 11. I_{CC1} vs. temperature

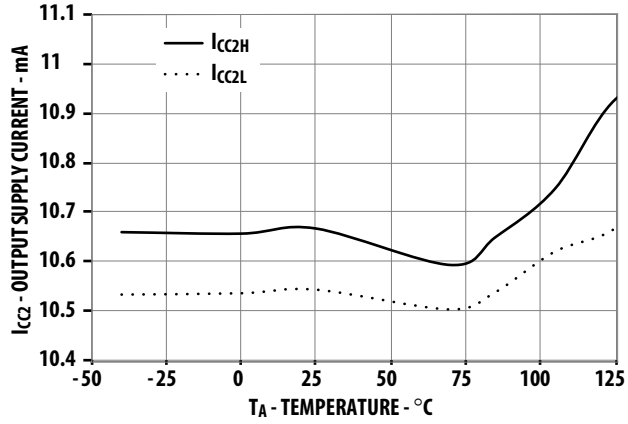


Figure 12. I_{CC2} vs. temperature

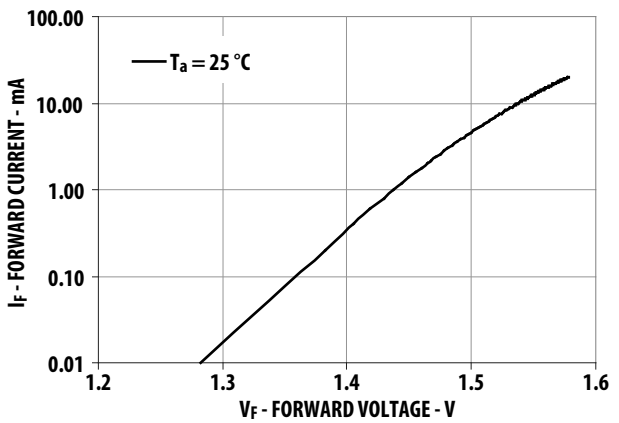


Figure 13. I_F vs. V_F

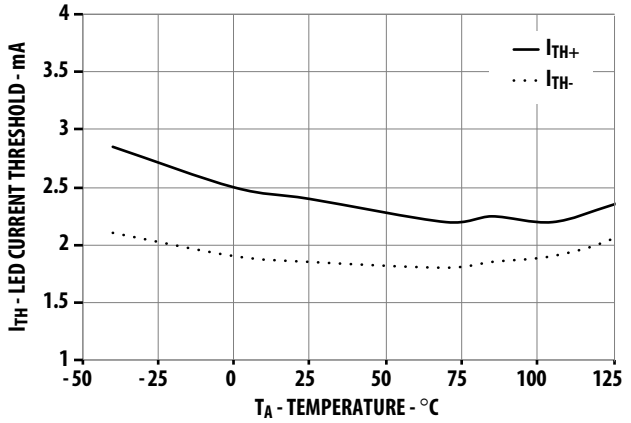


Figure 14. I_{TH} vs. temperature

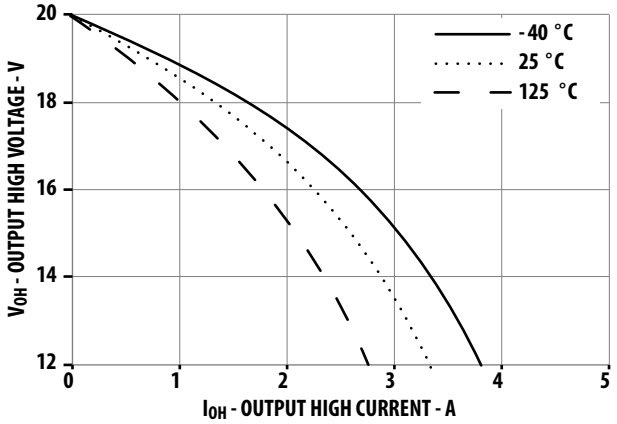


Figure 15. V_{OH} vs. I_{OH}

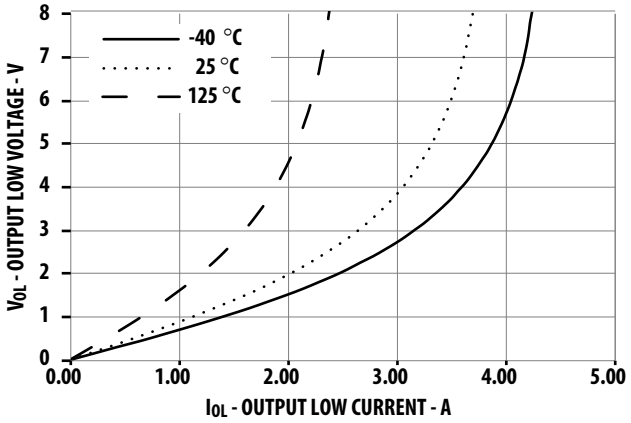


Figure 16. V_{OL} vs. I_{OL}

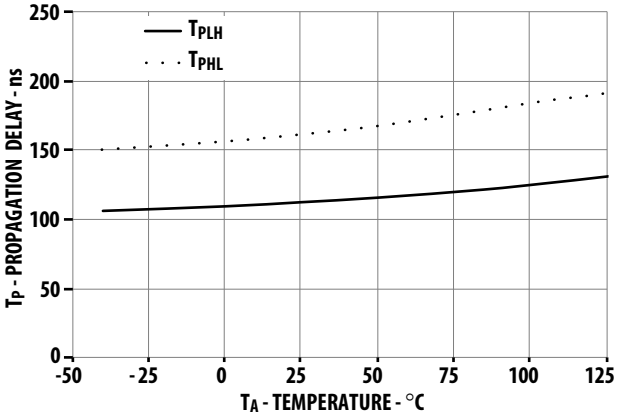


Figure 17. t_P vs. temperature

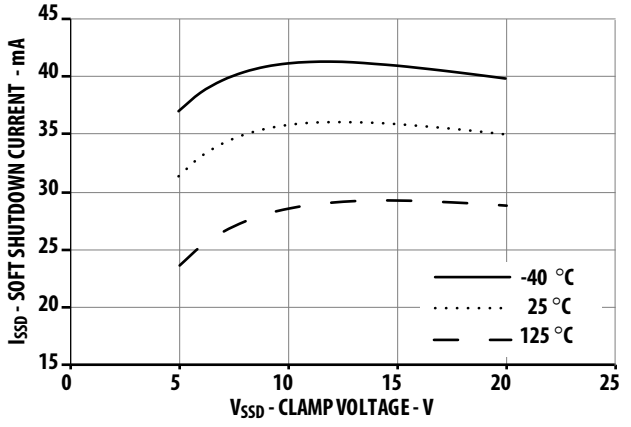


Figure 18. I_{SSD} vs. V_{SSD}

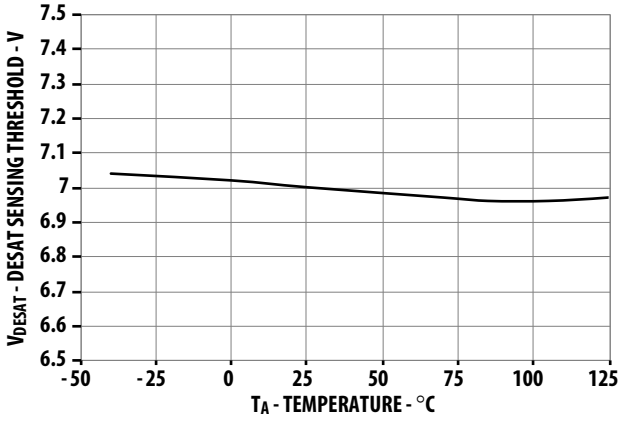


Figure 19. V_{DESAT} Threshold vs. temperature

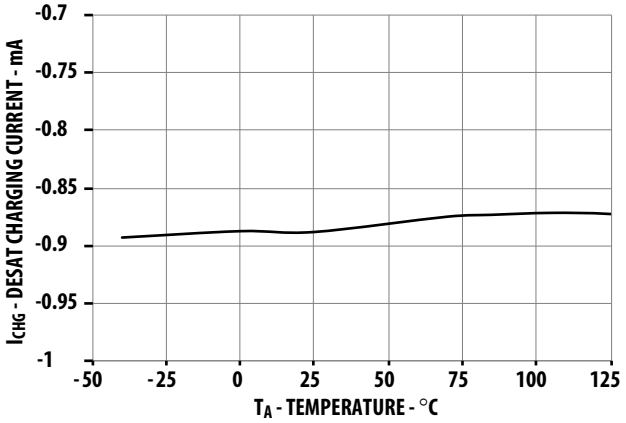


Figure 20. I_{CHG} vs. temperature

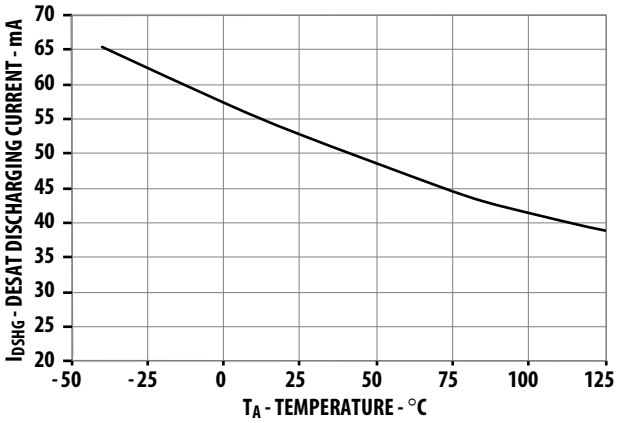
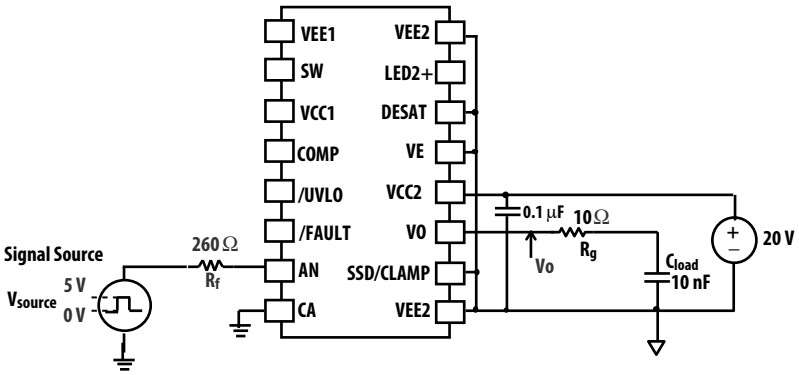


Figure 21. I_{DCHG} vs. temperature



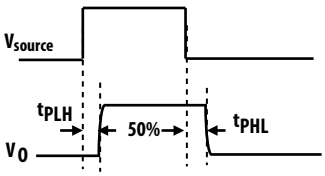


Figure 22. Propagation Delay Test Circuit

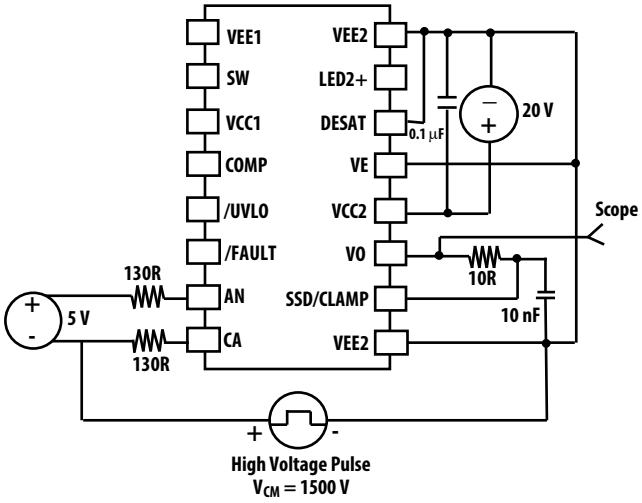


Figure 23. CMR V_o High Test Circuit

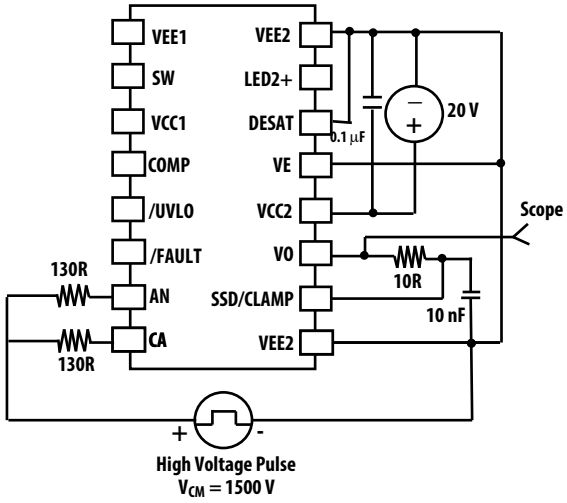


Figure 24. CMR V_o Low Test Circuit

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