LP38843 3A Ultra Low Dropout Linear Regulators *Stable with Ceramic Output Capacitors*

Check for Samples: LP38843

FEATURES

- **Ideal for Conversion From 1.8V or 1.5V Inputs**
- **Designed for use with low ESR Ceramic Capacitors**
- **0.8V, 1.2V and 1.5V Standard Voltages Available**
- **Ultra Low Dropout Voltage (210mV at 3A typ)**
- **1.5% Initial Output Accuracy**
- **Load Regulation of 0.1%/A (Typical)**
- **30nA Quiescent Current in Shutdown (Typical)**
- **Low Ground Pin Current at all Loads**
- **Over Temperature/Over Current Protection**
- **Available in 5 Lead TO-220 and DDPAK/TO-263 Packages**
- **−40°C to +125°C Junction Temperature Range**

APPLICATIONS

- **ASIC Power Supplies In:**
  - **Desktops, Notebooks, and Graphics Cards, Servers**
  - **Gaming Set Top Boxes, Printers and Copiers**
- **Server Core and I/O Supplies**
- **DSP and FPGA Power Supplies**
- **SMPS Post-Regulator**

DESCRIPTION

The LP38843 is a high-current, fast-response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in TO-220 and DDPAK/TO-263 packages.

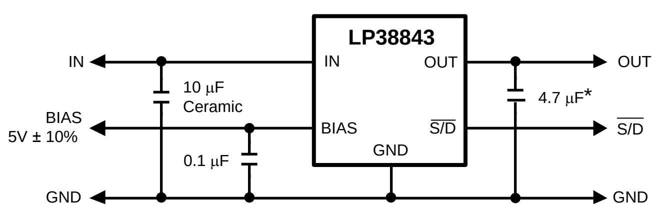
Dropout Voltage: 210 mV (typ) at 3A load current.

Quiescent Current: 30 mA (typ) at full load.

Shutdown Current: 30 nA (typ) when $\overline{S/D}$ pin is low.

Precision Output Voltage: 1.5% room temperature accuracy.

TYPICAL APPLICATION CIRCUIT



* Minimum value required if Tantalum capacitor is used (see Application Hints).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM

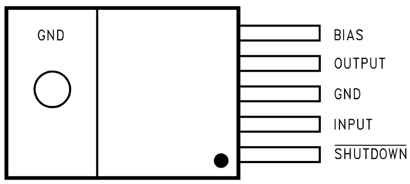


Figure 1. TO-220, Top View

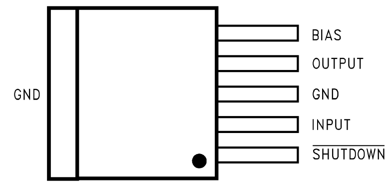
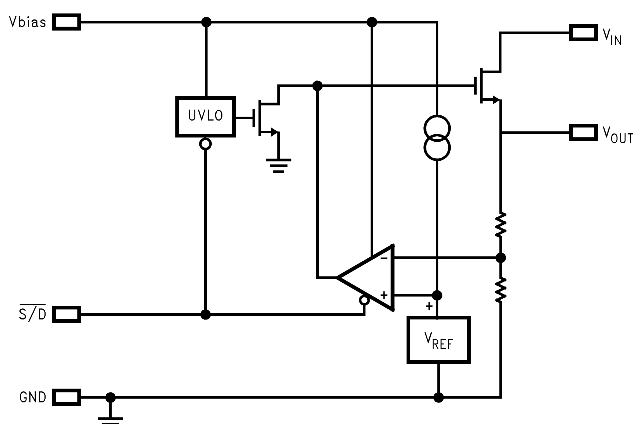


Figure 2. DDPAK/TO-263, Top View

PIN DESCRIPTIONS

Pin Name	Description
BIAS	The bias pin is used to provide the low current bias voltage to the chip which operates the internal circuitry and provides drive voltage for the N-FET.
OUTPUT	The regulated output voltage is connected to this pin.
GND	This is both the power and analog ground for the IC. Note that both pin three and the tab of the TO-220 and DDPAK/TO-263 packages are at ground potential. Pin three and the tab should be tied together using the PC board copper trace material and connected to circuit ground.
INPUT	The high current input voltage which is regulated down to the nominal output voltage must be connected to this pin. Because the bias voltage to operate the chip is provided separately, the input voltage can be as low as a few hundred millivolts above the output voltage.
SHUTDOWN	This provides a low power shutdown function which turns the regulated output OFF. Tie to V_{BIAS} if this function is not used.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS [1]

If Military/Aerospace specified devices are required, contact the Texas Instruments Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating Human Body Model [2] Machine Model [3]	 2 kV 200V
Power Dissipation [4]	Internally Limited
V_{IN} Supply Voltage (Survival)	−0.3V to +6V
V_{BIAS} Supply Voltage (Survival)	−0.3V to +7V
Shutdown Input Voltage (Survival)	−0.3V to +7V
I_{OUT} (Survival)	Internally Limited
Output Voltage (Survival)	−0.3V to +6V
Junction Temperature	−40°C to +150°C

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but **do not** ensure specific performance limits. For specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.
(2) The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.
(3) The machine model is a 220 pF capacitor discharged directly into each pin.
(4) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values. θ_{J-A} for TO-220 devices is 65°C/W if no heatsink is used. If the TO-220 device is attached to a heatsink, a θ_{J-S} value of 4°C/W can be assumed. θ_{J-A} for DDPAK/TO-263 devices is approximately 35°C/W if soldered down to a copper plane which is at least 1 square inches in area. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

RECOMMENDED OPERATING CONDITIONS

V_{IN} Supply Voltage	(V_{OUT} + V_{DO}) to 5.5V
Shutdown Input Voltage	0 to +5.5V
I_{OUT}	3A
Operating Junction Temperature Range	−40°C to +125°C
V_{BIAS} Supply Voltage	4.5V to 5.5V
V_{OUT}	0.8V to 1.5V

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, V_{BIAS} = 4.5V, I_L = 10 mA, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $V_{\overline{S/D}} = V_{BIAS}$. Min/Max limits are specified through testing, statistical correlation, or design.[(1)]

Symbol	Parameter	Conditions	MIN	TYP [(2)]	MAX	Units
V_O	Output Voltage Tolerance	10 mA < I_L < 3A $V_O(NOM) + 1V \le V_{IN} \le 5.5V$ $4.5V \le V_{BIAS} \le 5.5V$	0.788 **0.776**	0.8	0.812 **0.824**	V
			1.182 **1.164**	1.2	1.218 **1.236**	
			1.478 **1.455**	1.5	1.523 **1.545**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation [(3)]	$V_O(NOM) + 1V \le V_{IN} \le 5.5V$		0.01		%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation [(4)]	10 mA < I_L < 3A		0.1	0.4 **0.6**	%/A
V_{DO}	Dropout Voltage [(5)]	I_L = 3A		210	270 **500**	mV
$I_Q(V_{IN})$	Quiescent Current Drawn from V_{IN} Supply	10 mA < I_L < 3A		30	35 **40**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.06	1 **30**	µA
$I_Q(V_{BIAS})$	Quiescent Current Drawn from V_{BIAS} Supply	10 mA < I_L < 3A		2	4 **6**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.03	1 **30**	µA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V		8		A
Shutdown Input						
V_{SDT}	Output Turn-off Threshold	Output = ON		0.7	**1.3**	V
		Output = OFF	**0.3**	0.7		
Td (OFF)	Turn-OFF Delay	R_{LOAD} X C_{OUT} << Td (OFF)		20		µs
Td (ON)	Turn-ON Delay	R_{LOAD} X C_{OUT} << Td (ON)		15		
$I_{\overline{S/D}}$	$\overline{S/D}$ Input Current	$V_{\overline{S/D}}$ =1.3V		1		µA
		$V_{\overline{S/D}} \le 0.3V$		−1		
θ_{J-A}	Junction to Ambient Thermal Resistance	TO-220, No Heatsink		65		°C/W
		DDPAK/TO-263, 1 sq.in Copper		35		
AC Parameters						
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT}$ +1V, f = 120 Hz		80		dB
		$V_{IN} = V_{OUT}$ + 1V, f = 1 kHz		65		
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT}$ + 3V, f = 120 Hz		58		
		$V_{BIAS} = V_{OUT}$ + 3V, f = 1 kHz		58		
	Output Noise Density	f = 120 Hz		1		$\mu V/\sqrt{Hz}$
e_n	Output Noise Voltage V_{OUT} = 1.5V	BW = 10 Hz − 100 kHz		150		µV (rms)
		BW = 300 Hz − 300 kHz		90		

(1) If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.
(2) Typical numbers represent the most likely parametric norm for 25°C operation.
(3) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(4) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
(5) Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T_J = 25°C, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $\overline{S/D}$ Pin is tied to V_{BIAS}, V_{OUT} = 1.2V, I_L = 10mA, V_{BIAS} = 5V, V_{IN} = V_{OUT} + 1V.

V_{BIAS} Transient Response

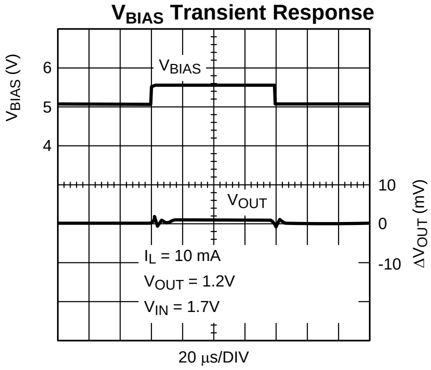


Figure 3.

Load Transient Response

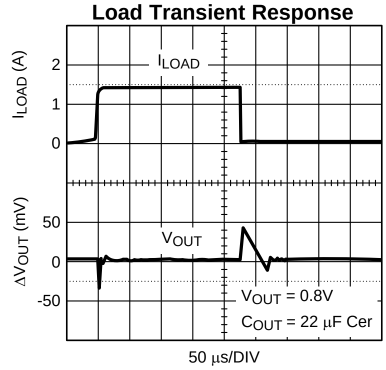


Figure 4.

Load Transient Response

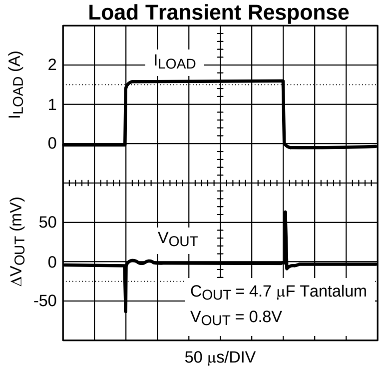


Figure 5.

Dropout Voltage Over Temperature

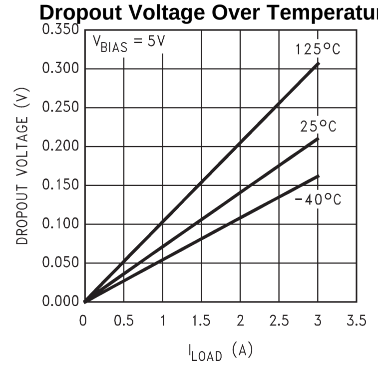


Figure 6.

V_{OUT} vs Temperature

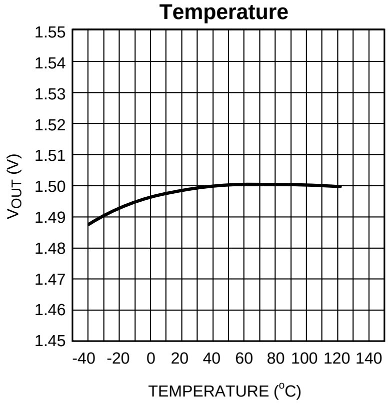


Figure 7.

V_{BIAS} PSRR

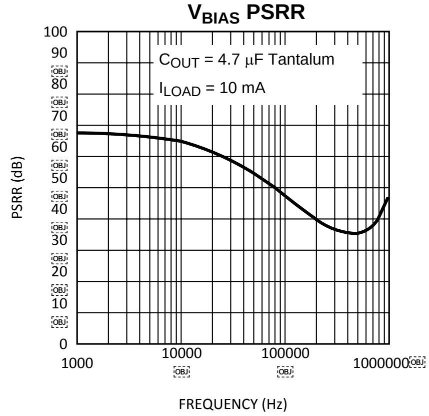


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $\overline{S/D}$ Pin is tied to V_{BIAS}, V_{OUT} = 1.2V, I_L = 10mA, V_{BIAS} = 5V, V_{IN} = V_{OUT} + 1V.

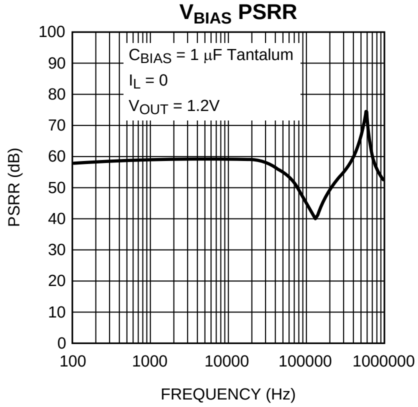


Figure 9.

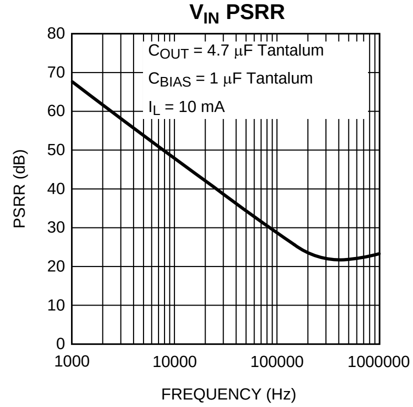


Figure 10.

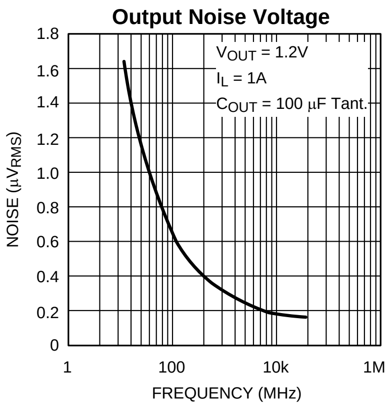


Figure 11.

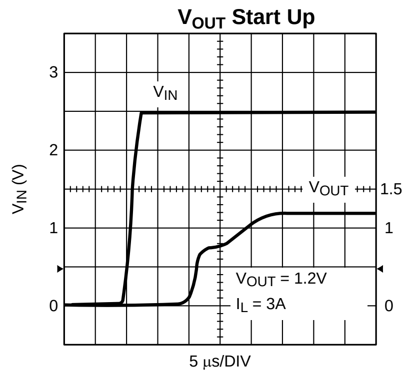


Figure 12.

Application Hints

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

OUTPUT CAPACITOR

An output capacitor is required on the LP3884X devices for loop stability. The minimum value of capacitance necessary depends on type of capacitor: if a solid Tantalum capacitor is used, the part is stable with capacitor values as low as 4.7µF. If a ceramic capacitor is used, a minimum of 22 µF of capacitance must be used (capacitance may be increased without limit). The reason a larger ceramic capacitor is required is that the output capacitor sets a pole which limits the loop bandwidth. The Tantalum capacitor has a higher ESR than the ceramic which provides more phase margin to the loop, thereby allowing the use of a smaller output capacitor because adequate phase margin can be maintained out to a higher crossover frequency. The tantalum capacitor will typically also provide faster settling time on the output after a fast changing load transient occurs, but the ceramic capacitor is superior for bypassing high frequency noise.

The output capacitor must be located less than one centimeter from the output pin and returned to a clean analog ground. Care must be taken in choosing the output capacitor to ensure that sufficient capacitance is provided over the full operating temperature range. If ceramics are selected, only X7R or X5R types may be used because Z5U and Y5F types suffer severe loss of capacitance with temperature and applied voltage and may only provide 20% of their rated capacitance in operation.

INPUT CAPACITOR

The input capacitor is also critical to loop stability because it provides a low source impedance for the regulator. The minimum required input capacitance is 10 µF ceramic (Tantalum not recommended). The value of C_{IN} may be increased without limit. As stated above, X5R or X7R must be used to ensure sufficient capacitance is provided. The input capacitor must be located less than one centimeter from the input pin and returned to a clean analog ground.

BIAS CAPACITOR

The 0.1µF capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 5.5V to assure proper operation of the part.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 4V.

SHUTDOWN OPERATION

Pulling down the shutdown ($\overline{S/D}$) pin will turn-off the regulator. Pin $\overline{S/D}$ must be actively terminated through a pull-up resistor (10 kΩ to 100 kΩ) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to V_{BIAS} if not used.

POWER DISSIPATION/HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} + (V_{IN}) I_{GND} \quad (1)$$

where I_{GND} is the operating ground current of the device.

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (2)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D \quad (3)$$

These parts are available in TO-220 and DDPAK/TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 60 °C/W for TO-220 package and ≥ 60 °C/W for DDPAK/TO-263 package no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

HEATSINKING TO-220 PACKAGE

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for DDPAK/TO-263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$$\theta_{HA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC}. \quad (4)$$

In this equation, θ_{CH} is the thermal resistance from the case to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. θ_{JC} is about 3°C/W for a TO-220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

HEATSINKING DDPAK/TO-263 PACKAGE

The DDPAK/TO-263 package uses the copper plane on the PCB as a heatsink. The tab of this package is soldered to the copper plane for heat sinking. The graph below shows a curve for the θ_{JA} of DDPAK/TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

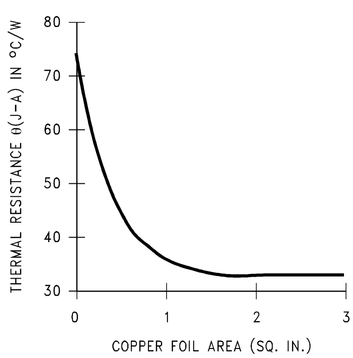


Figure 13. θ_{JA} vs Copper (1 Ounce) Area for DDPAK/TO-263 package

As shown in the graph below, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

Figure 14 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

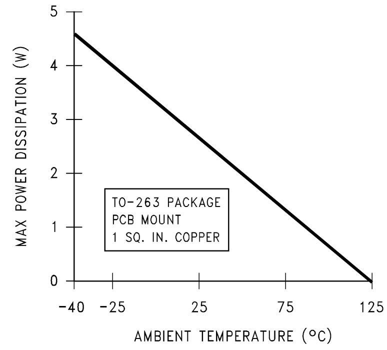


Figure 14. Maximum power dissipation vs ambient temperature for DDPAK/TO-263 package

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP38843S-1.2/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 5	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38843S -1.2
LP38843S-1.2/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38843S -1.2
LP38843S-1.5/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 5	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38843S -1.5
LP38843S-1.5/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38843S -1.5
LP38843SX-1.2/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38843S -1.2
LP38843SX-1.2/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38843S -1.2
LP38843SX-1.5/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38843S -1.5
LP38843SX-1.5/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38843S -1.5
LP38843T-0.8/NOPB	Active	Production	TO-220 (KC) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38843T -0.8
LP38843T-0.8/NOPB.A	Active	Production	TO-220 (KC) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38843T -0.8
LP38843T-1.2/NOPB	Active	Production	TO-220 (KC) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38843T -1.2
LP38843T-1.2/NOPB.A	Active	Production	TO-220 (KC) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38843T -1.2
LP38843T-1.5/NOPB	Active	Production	TO-220 (KC) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38843T -1.5
LP38843T-1.5/NOPB.A	Active	Production	TO-220 (KC) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38843T -1.5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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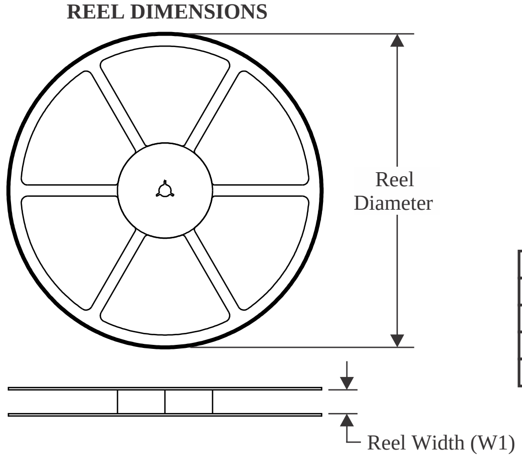
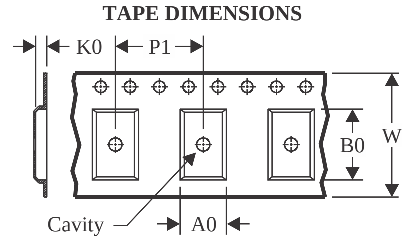
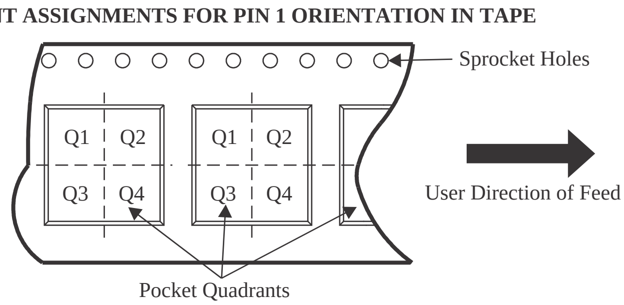
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





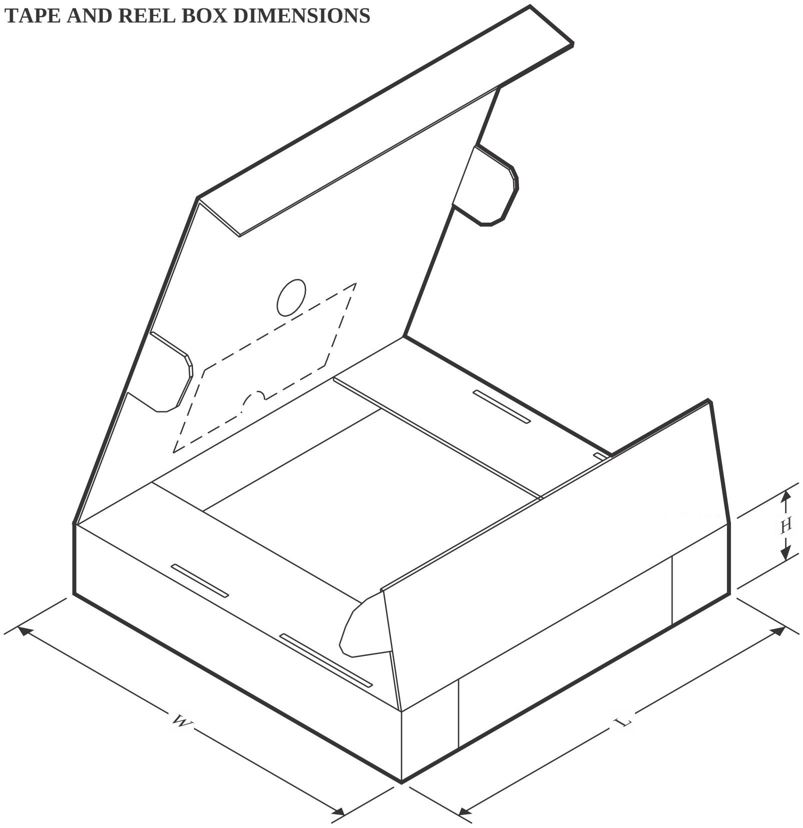
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38843SX-1.2/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP38843SX-1.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

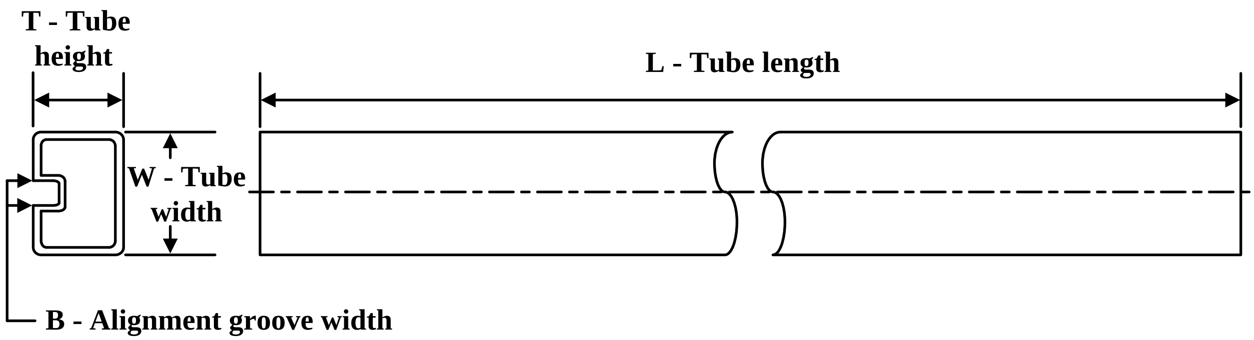
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38843SX-1.2/NOPB	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0
LP38843SX-1.5/NOPB	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0

TUBE



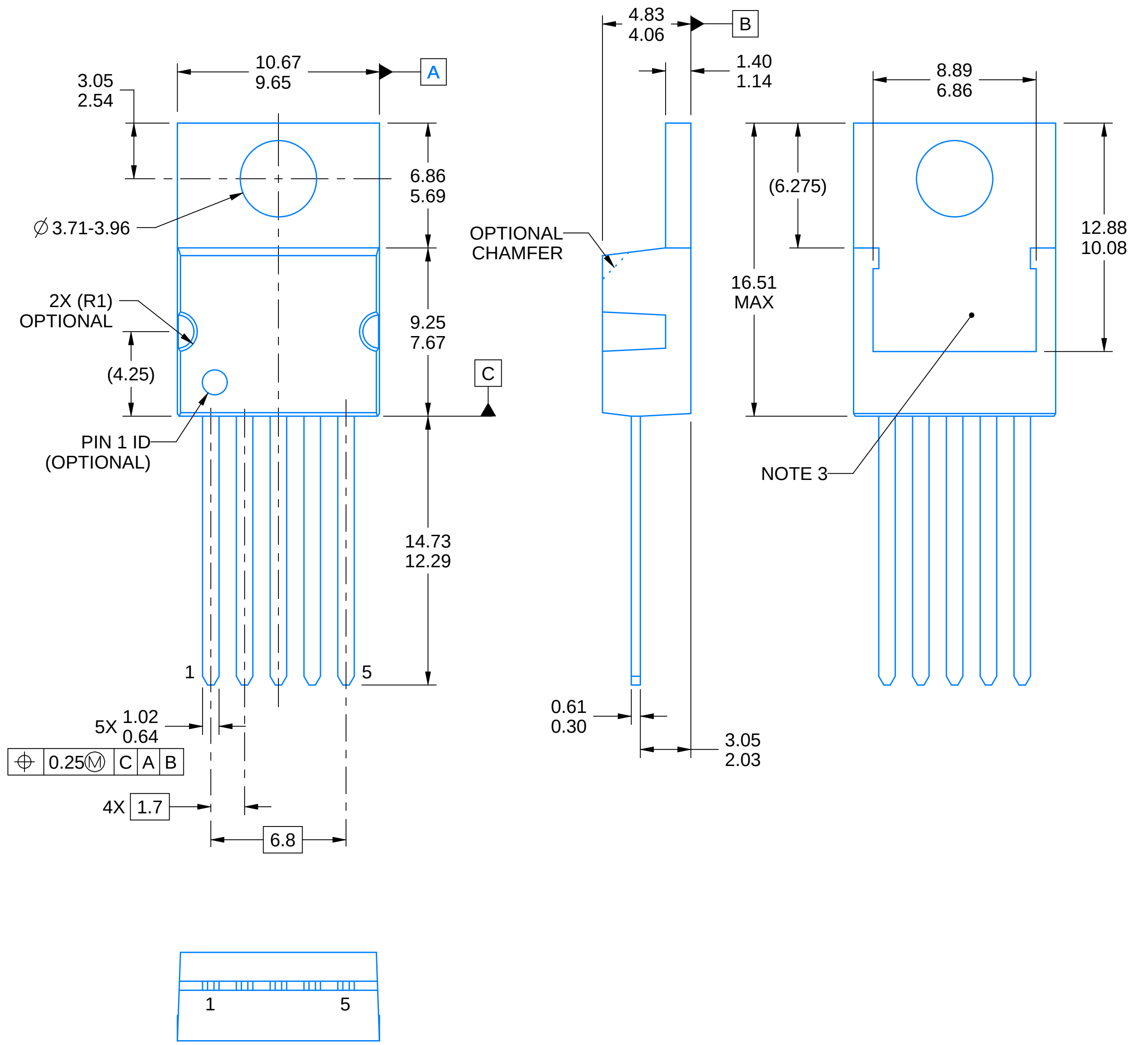
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38843S-1.2/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38843S-1.2/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38843S-1.5/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38843S-1.5/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38843T-0.8/NOPB	KC	TO-220	5	45	502	33	6985	4.06
LP38843T-0.8/NOPB.A	KC	TO-220	5	45	502	33	6985	4.06
LP38843T-1.2/NOPB	KC	TO-220	5	45	502	33	6985	4.06
LP38843T-1.2/NOPB.A	KC	TO-220	5	45	502	33	6985	4.06
LP38843T-1.5/NOPB	KC	TO-220	5	45	502	33	6985	4.06
LP38843T-1.5/NOPB.A	KC	TO-220	5	45	502	33	6985	4.06

PACKAGE OUTLINE

TO-220 - 16.51 mm max height

TO-220



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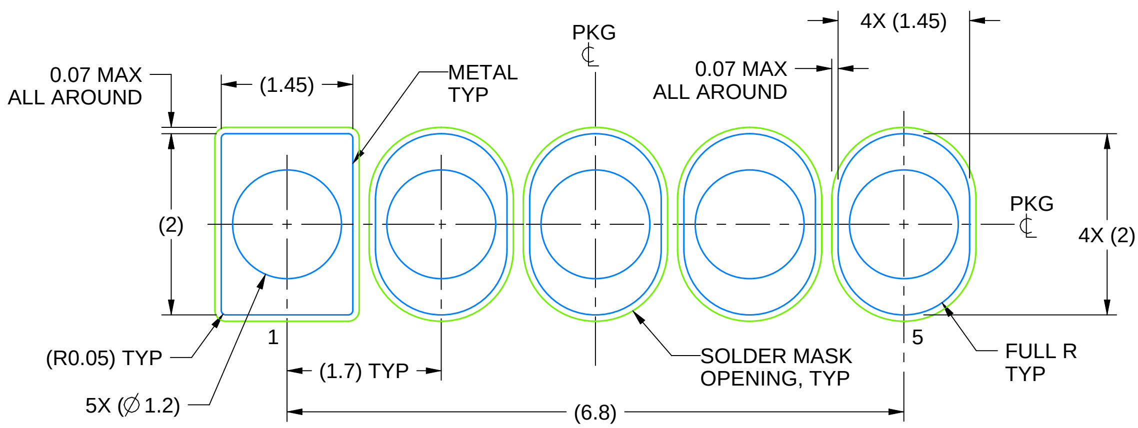
NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.



LAND PATTERN
NON-SOLDER MASK DEFINED
SCALE:12X

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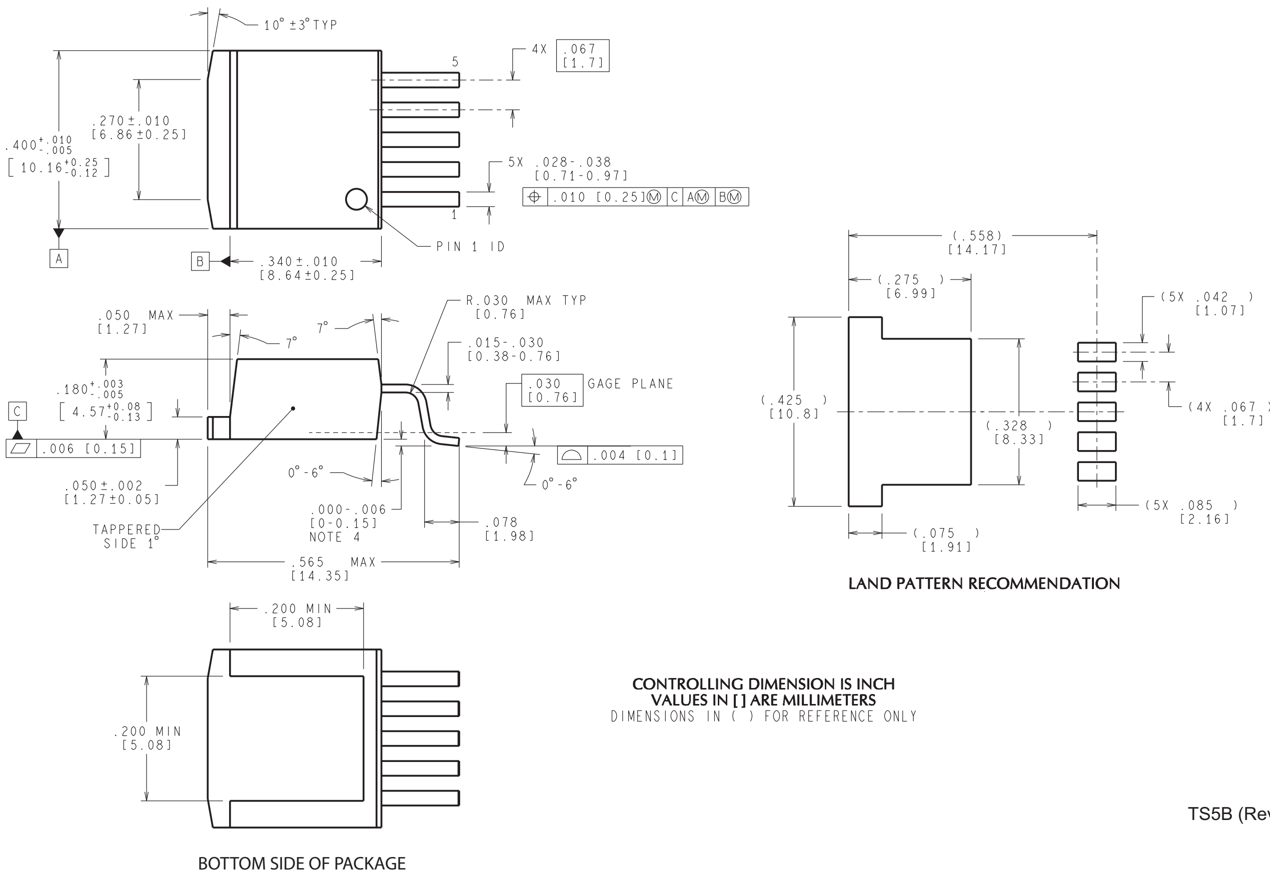
KTT0005B



TS5B (Rev D)

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