DATA SHEET

TDA3840
TV IF amplifier and demodulator with TV signal identification

Preliminary specification
File under Integrated Circuits, IC02

April 1991

Philips
Semiconductors

PHILIPS

TV IF amplifier and demodulator with TV signal identification

TDA3840

FEATURES

- Low supply voltage range, from 5.0 V to 8.0 V
- Low power dissipation, 200 mW at 5 V
- High supply ripple rejection
- Wide IF bandwidth of 80 MHz
- Synchronous demodulator with low differential phase and gain
- Additional video buffer with a wide bandwidth of 10 MHz
- Video off switch
- Peak sync AGC
- Adjustable take-over point (TOP); positive AGC slope
- Switching to fast AGC dependent on TV identification
- Alignment free AFC detector with integrated phase shift
- ESD protection
- TV signal identification
- Options: tracking of reference circuit

GENERAL DESCRIPTION

The TDA3840 is a bipolar integrated circuit for vision IF-signal processing in TV and VTRs, designed for a supply voltage range from 5.0 V to 8.0 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)		4.75	5.0	8.8	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
$V_{1\text{-}20(rms)}$	IF input signal for nominal video output voltage at pin 14 (RMS value)	f = 38.9 MHz	–	70	–	µV
	minimum IF input signal for TV signal identification at pin 6 (RMS value)	maximum G_v	–	20	40	µV
V_o	video output signal (pin 12)	buffered	–	2.0	–	V
G_v	IF voltage gain control range		–	66	–	dB
S/N	signal-to-noise ratio	$V_{1\text{-}20}$ = 10 mV	55	60	–	dB
V_8	AFC output voltage swing		–	4.0	–	V
S_{AFC}	AFC steepness (pin 8)		–	2	–	µA/kHz
RR	supply voltage ripple rejection (pin 12)		30	35	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3840	20	DIL	plastic	SOT146(1)
TDA3840T	20	mini-pack	plastic	SO20L; SOT163A(2)

Note

1. SOT146-1; 1996 December 13.
2. SOT163-1; 1996 December 13.

TV IF amplifier and demodulator with TV signal identification

TDA3840

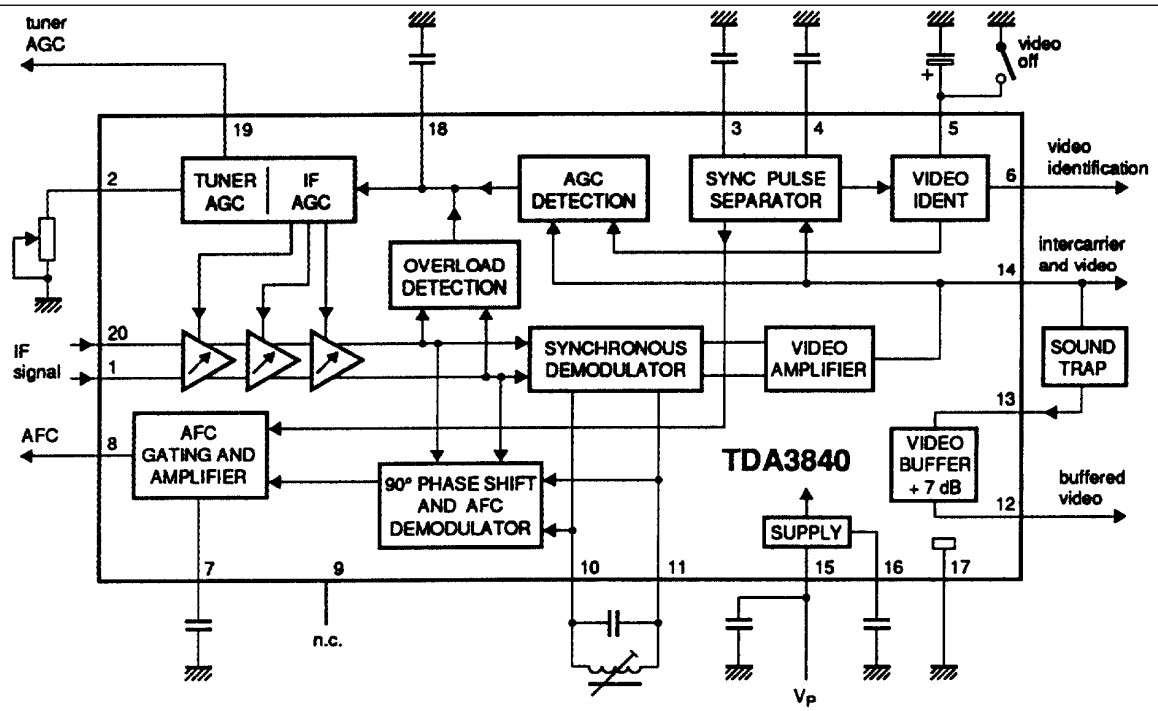


Fig.1 Block diagram.

PIN CONFIGURATION

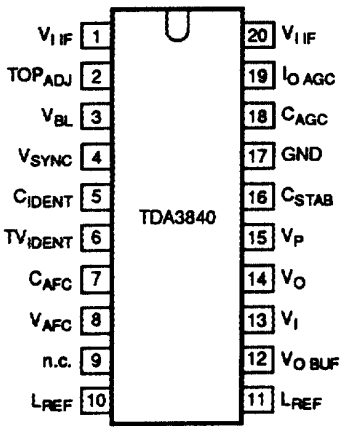


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{I\ IF}$	1	IF input (balanced)
TOP_{ADJ}	2	tuner AGC take-over point adjustment
V_{BL}	3	black level voltage
V_{SYNC}	4	sync pulse amplitude voltage
C_{IDENT}	5	identification capacitor
TV_{IDENT}	6	video identification output
C_{AFC}	7	AFC capacitor
V_{AFC}	8	AFC output signal
n.c.	9	not connected
L_{REF}	10	LC reference tuned circuit
L_{REF}	11	LC reference tuned circuit
$V_{O\ BUF}$	12	buffered video output signal
V_I	13	video input signal for buffer
V_O	14	video output signal with intercarrier signal
V_P	15	supply voltage
C_{STAB}	16	supply voltage stabilization
GND	17	ground
C_{AGC}	18	AGC capacitor
$I_{O\ AGC}$	19	tuner AGC output signal
$V_{I\ IF}$	20	IF input (balanced)

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

1. 3-stage gain controlled IF amplifier
2. Overload detector
3. Reference amplifier
4. Carrier signal reference limiter
5. Video demodulator
6. Video amplifier
7. Video buffer amplifier
8. AGC detector
9. IF and tuner AGC (with adjustable TOP)
10. Sync pulse separator
11. Video identification
12. 90° phase shift and AFC demodulator
13. AFC gating, AFC amplifier and AFC switch
14. Voltage stabilizer

1. 3-stage gain controlled IF amplifier (pins 1 and 20)

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Gain control is achieved by current divider stages. The emitter feedback resistors are optimized for low noise and signal handling capability.

2. Overload detector

The overload detector is fed from the output of the third IF amplifier. As soon as the IF voltage exceeds the overload threshold in the detector, its output current reduces the IF amplification by discharging the AGC capacitor.

3. Reference amplifier

For passive video carrier regeneration an integrated differential amplifier with resistive load allows capacitive coupling of the resonant circuit for notch and tracking functions.

4. Carrier signal reference limiter

A limiter stage after the reference amplifier eliminates amplitude modulation. Its output is fed to the video demodulator.

5. Video demodulator

The video demodulator receives both the limited reference carrier signal and the IF signal. The video signal can also be switched off.

6. Video amplifier

The video amplifier is an operational amplifier with internal feedback and wide bandwidth.

7. Video buffer amplifier

The video buffer amplifier is an operational amplifier with internal feedback, wide bandwidth and frequency compensation; gain and input impedance are adapted to operate with a ceramic sound trap. The load for the sound trap is an integrated resistive divider.

8. AGC detector

The peak sync AGC detector generates a fast current pulse to discharge the AGC capacitor (gain reduction). This minimizes the video signal distortion.
To filter out the sound carrier the video signal is fed through low pass filters. After the low pass filters the video signal with attenuated sound carrier, is fed to the AGC detector. The charging current of the AGC capacitor is optimized for minimum distortion of the video signal. With positive modulation the charging current is very low and consequently the AGC time constant is large. When the video identification circuit does not detect a video signal, the charging current is increased.

9. IF and tuner AGC

The voltage on the AGC capacitor is used to control the gain of the three IF amplifier stages and to supply the tuner AGC current (open-collector). The tuner AGC TOP potentiometer at pin 2 adjusts the IF signal level from the tuner. To stabilize the IF output voltage of the tuner, IF slip (= variation of IF gain over the total tuner range) is kept at a minimum.

10. Sync pulse separator

The sync pulse separator supplies two internally-used pulses using the bandwidth limited video signal. These are the composite sync for the AFC detector and the vertical sync for the video identification output. The bandwidth is limited to reduce the noise and increase the identification sensitivity.

11. Video identification

An analog integrator monitors the duty cycle of the vertical sync pulses to identify the video signal. The integrator output is fed to a window comparator which has an open collector output stage to provide the video ident signal. The complete circuit operates in combination with the sync separator and is optimized for high sensitivity.

12. 90° phase shift and AFC demodulator

The AFC demodulator needs a 90° phase-shifted carrier. The output of the carrier signal reference limiter is fed to an active 90° phase-shift circuit. The 90° (lead) phase-shifted carrier and the IF signal are fed to the AFC demodulator. The demodulated signal and the IF signal are fed to the AFC gating stage.

13. AFC gating, AFC amplifier and AFC switch

With negative modulated video IF signals the output of the AFC detector is gated by composite sync pulses to prevent video modulation on the AFC output. The gated signal is integrated by an AFC capacitor. The AFC amplifier converts the capacitor voltage to an AFC current (open collector sink/source output). The AFC function can be externally switched off for test purposes.

For high-performance signal handling the AFC signal can be used to track the resonant circuit as shown in Fig.11.

14. Voltage stabilizer

An integrated bandgap voltage stabilizer generates an internal supply voltage of 4 V. A decoupling capacitor reduces noise and supply voltage ripple.

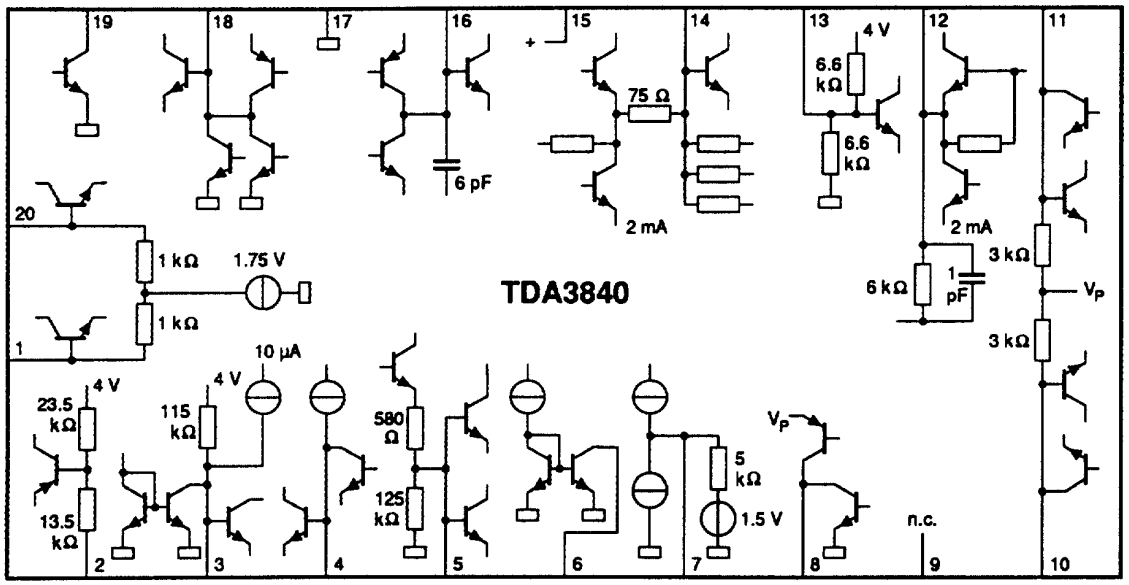


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT
V_P	supply voltage at pin 15:	SOT146	–	8.8	V
		SOT163A	–	6.0	V
V_{19}	tuner AGC voltage		–	13.2	V
V_8	permissible voltage at AFC output		–	V_P	V
I_{15}	supply current		–	55	mA
T_{stg}	storage temperature range		–25	+ 150	°C
T_{amb}	operating ambient temperature range		0	+ 70	°C
V_{ESD}	ESD sensitivity		–	± 300	V

CHARACTERISTICS

V_P = 5 V and T_{amb} = 25 °C; f_{VC} = 38.9 MHz; all voltages are measured to GND (pin 17); measured in test circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)	DIL-package	4.75	5.0	8.8	V
		SO-package	4.75	5.0	6.0	V
I_P	supply current (pin 15)	V_P = 5.0 V	–	42	–	mA
RR	ripple rejection (pin 12)		30	35	–	dB
IF amplifier						
B	bandwidth	–3 dB	–	80	–	MHz
R_I	input resistance (pins 1 and 20)		–	2	–	kΩ
C_I	input capacitance (pins 1 and 20)		–	1.5	–	pF
$V_{1\text{-}20(rms)}$	IF input signal (RMS value)	video output –1 dB	–	70	–	μV
	maximum IF input signal	minimum G_V; note 1	100	–	–	mV
G_V	gain control range		63	66	–	dB
IF AGC						
I_{18}	leakage current AGC capacitor		–	–	1	μA
	charging current AGC capacitor	with video identification	–	13	–	μA
	charging current AGC capacitor	without video identification	–	35	–	μA
I_{18M}	discharging peak current capacitor		–	2	–	mA
t_1	responsible time of IF input signal change	50 dB increasing step	–	1	–	ms
		50 dB decreasing step	–	150	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuner AGC (note 2)						
$V_{1\text{-}20(rms)}$	lower IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R2 = 22 kΩ	–	–	1	mV
	upper IF input signal for starting point of tuner take-over; see Fig.5 (RMS value)	R2 = 0 Ω	50	–	–	mV
	TOP variation	60 K temperature range	–	2	3	dB
I_{19}	tuner AGC output current	V_{19} = 0.5 V	1	2	–	mA
Synchronous demodulator and video amplifier (note 3)						
V_{14}	composite video output signal		0.9	1.0	1.1	V
	sync level voltage		–	1.5	–	V
	zero carrier level voltage		–	2.6	–	V
I_{14}	output current	DC and AC	–	–	± 1.0	mA
R_{14}	output resistance		–	75	–	Ω
B	video bandwidth at –1 dB (pin 14)	$C_{load} \leq 20$ pF	7	8	–	MHz
V_{14}	upper video clipping level		–	3.6	–	V
	lower video clipping level		–	0.3	–	V
Buffered video output signal (see Fig.6)						
G	gain of video buffer		6.5	7.0	–	dB
V_{12}	sync level clamping voltage		–	1.35	–	V
	upper video clipping level		–	4.25	–	V
	lower video clipping level		–	0.3	–	V
I_{12}	output current	DC and AC	–	–	± 1.0	mA
R_{12}	output resistance		–	–	10	Ω
B	video bandwidth at –1 dB (pin 12)	$C_{load} \leq 20$ pF	–	10	–	MHz
R_I	input resistance (pin 13)		–	3.3	–	kΩ
C_I	input capacitance (pin 13)		–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Overall video performance (see Fig.6)						
V_o	video output signal (pin 12)	negative modulation; note 3	–	2	–	V
B	video bandwidth at –2 dB (pin 12)	$C_{load} \leq 20$ pF	7	8	–	MHz
S/N	signal-to-noise ratio (see Fig.7)	$V_{1\text{-}20}$ = 10 mV; note 4	55	60	–	dB
α_1	intermodulation for blue (note 5)	f = 1.1 MHz	56	58	–	dB
		f = 3.3 MHz	62	–	–	dB
α_2	intermodulation for yellow (note 5)	f = 1.1 MHz	53	56	–	dB
		f = 3.3 MHz	60	–	–	dB
α_3	signal harmonic suppression		–	26	–	dB
V_5	video switch off voltage	note 6	–	–	1	V
α_4	attenuation of video signal (pin 14)	video signal switched off	50	60	–	dB
ΔG	differential gain	EBU test line 330	–	2	–	%
$\Delta\Phi$	differential phase	EBU test line 330	–	2	–	deg
$\Delta V/V$	variation of video output signal (pin 14)	gain control 50 dB; $V_{1\text{-}20(rms)}$ = 0.3 to 100 mV	–	–	0.5	dB
V_{res1}	residual vision carrier (pin 12)		–	1	–	mV
V_{res2}	residual second harmonic of the vision carrier (pin 12)		–	1	–	mV
Video identification						
$V_{1\text{-}20(rms)}$	minimum IF input signal for TV identification at pin 14 (RMS value)	maximum G_V	–	20	40	µV
V_6	video identification voltage (signal unidentified)	$V_{1\text{-}20}$ = < 40 μV_{rms} I_6 = 0.5 mA	–	–	0.4	V
	video identification voltage (signal identified)	$V_{1\text{-}20}$ = ≥ 40 μV_{rms} I_6 = –1 µA	4.5	–	–	V
T_{sync}/T_{field}	vertical pulse duty cycle		4.5	8	16	x 10^{-3}
C/N	carrier-to-noise ratio (pin 1 and pin 20)	note 7	–	8	–	dB
I_5	allowed leakage current		–	–	3	µA
α_5	sync pulse suppression for correct TV signal identification		–	–	70	%
t_d	delay time of mute output signal		–	100	150	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AFC (see Fig.9 **and** Fig.10**); note** 8						
I_8	AFC source current output		0.16	0.19	0.22	mA
	AFC sink current output		0.16	0.19	0.22	mA
V_8	upper output voltage		4.3	–	4.7	V
	lower output voltage		0.3	–	0.7	V
S	control steepness	QB = 40; $V_{1\text{-}20(rms)}$ = 10 mV	–	2	–	μA/kHz
I_7	leakage current at AFC gating		–	–	± 1	μA

Notes to the characteristics

1. The video signal is still gain-controlled, $V_{14(p\text{-}p)}$ = 1 V, but intermodulation figures are degraded.
2. The starting point of tuner AGC can be adjusted by the resistor at pin 2. Fig.5 shows the AGC characteristic.
3. IF input signals are RMS values measured at TOP sync (standard B/G) and with a vision carrier of 38.9 MHz (see Fig.4). The IF input signal is fed from 50 Ω via a 1:1 transformer, DSB, to pins 1 and 20. With a 10 mV_{RMS} IF input signal, the residual vision carrier is: = 10 % for white (standard B/G).
4. In the test circuit of Fig.4, measured and weighted according to CCIR Recommendation 567:

   $$S/N = \frac{V_{14\ (black\ to\ white)}}{V_{14\ noise}(RMS,\ black)}$$

5. Intermodulation figures are defined as follows: $\alpha_1 = 20 \times \log \frac{V_o \text{ at } 4.4\ MHz}{V_o \text{ at } 1.1\ MHz} + 3.6\ dB$

   and $\alpha_2 = 20 \times \log \frac{V_o \text{ at } 4.4\ MHz}{V_o \text{ at } 3.3\ MHz}$

6. When $V_5 < 1$ V (short-circuited identification capacitor at pin 5) the video output signal at pin 14 is switched off. V_{14} shifts to “zero carrier level” (“ultra white” (2.6 V) for negative modulation).
   During normal operation the capacitor at pin 5 should not be loaded ($|I_5| \leq 3$ μA).
7. The C/N at the IF input (pins 1 and 20) for TV identification is defined as the RMS sync level of the vision IF signal input, relative to the RMS value of a superimposed white noise signal, with a bandwidth limited to 5 MHz.
8. The values for the AFC measurements depend on the Q_B of the reference circuit at pins 10 and 11. The internal phase shift is matched to a vision carrier of 38.9 MHz. The AFC function can be switched off for test purposes when pin 7 is connected to ground (V_7 = 0 V).

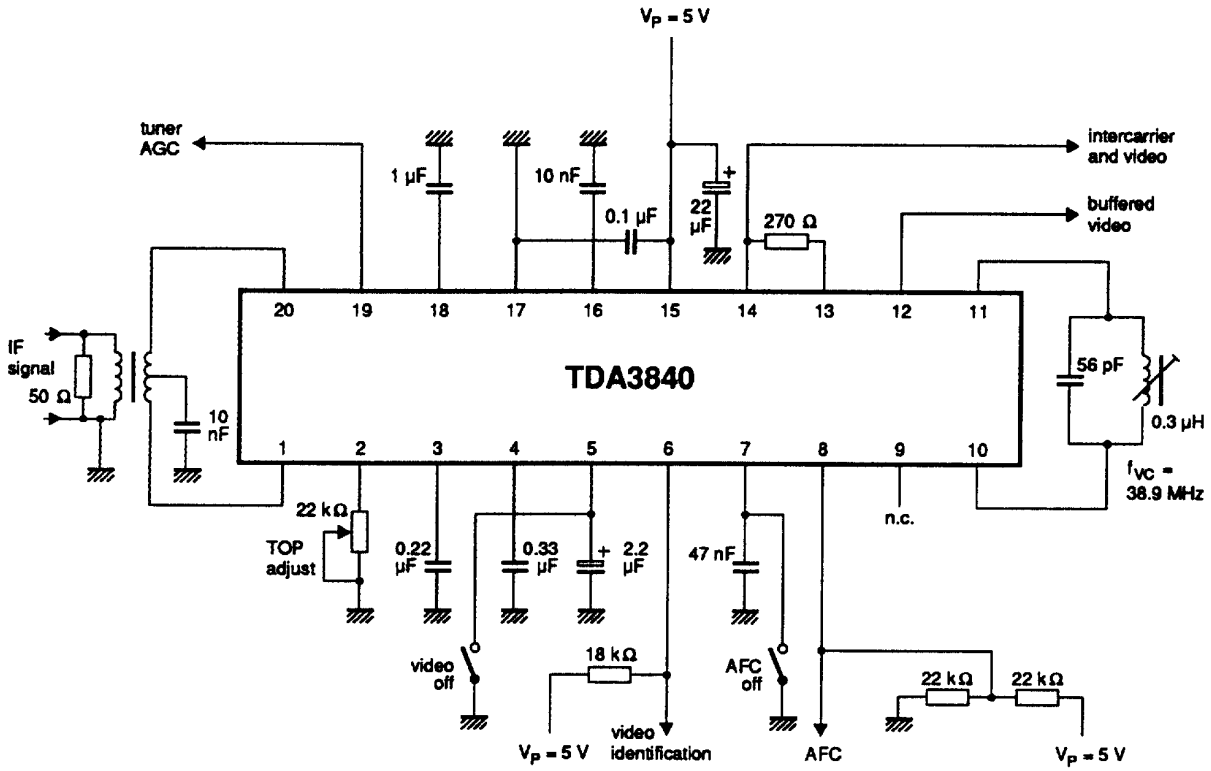


Fig.4 Test circuit.

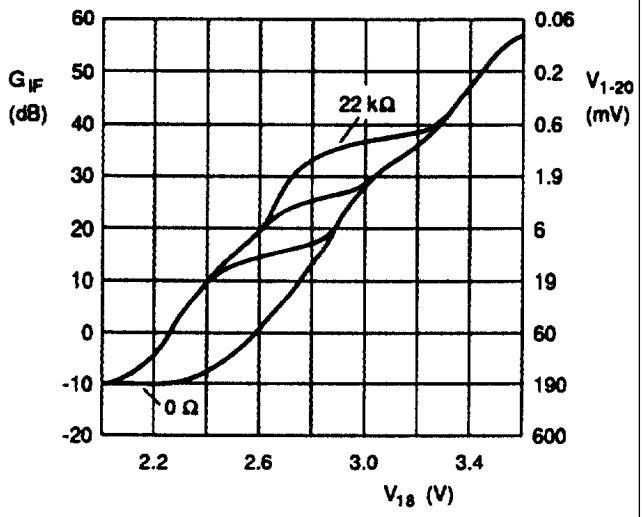


Fig.5 AGC characteristics with different values of R2.

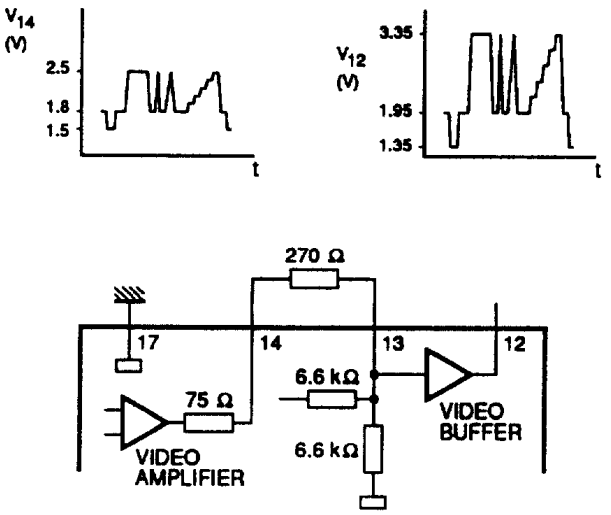


Fig.6 Video waveforms at intercarrier (pin 14) and buffered video (pin 12) outputs.

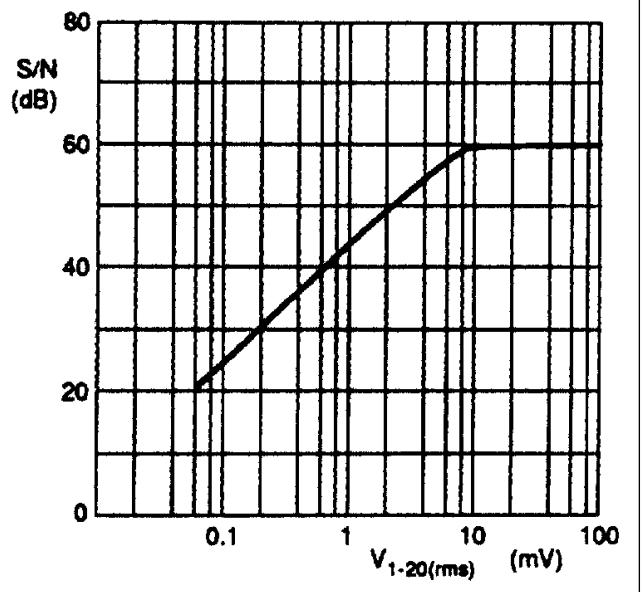
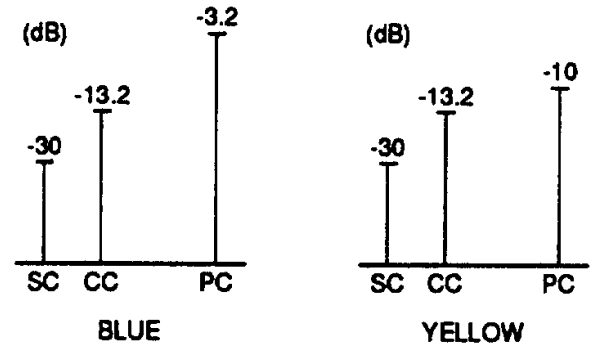


Fig.7 Signal-to-noise ratio as a function of IF input voltage (RMS value) at pins 1 and 20.



SC = sound carrier level; with respect to TOP sync level
CC = chrominance carrier level; with respect to TOP sync level
PC = picture carrier level; with respect to TOP sync level

Sound trap attenuation: 17 dB

Fig.8 Input conditions for intermodulation measurements.

APPLICATION INFORMATION

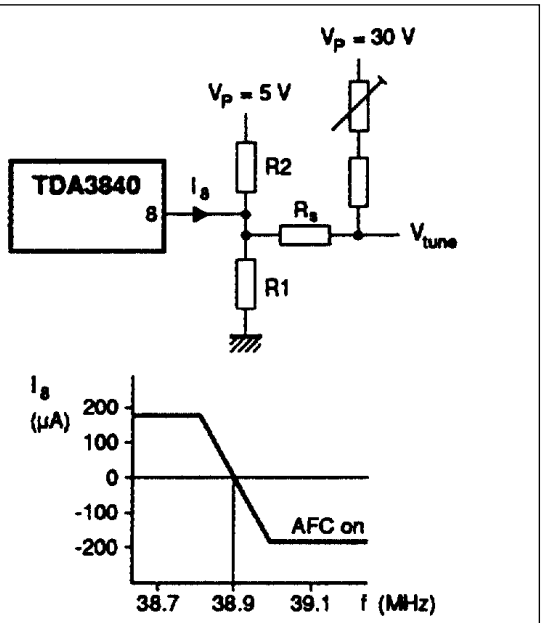


Fig.9 AFC interfacing for analog tuning systems and AFC characteristic.

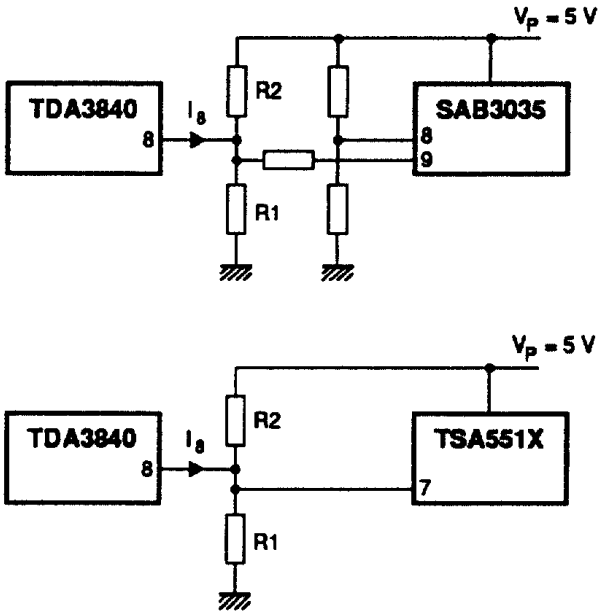
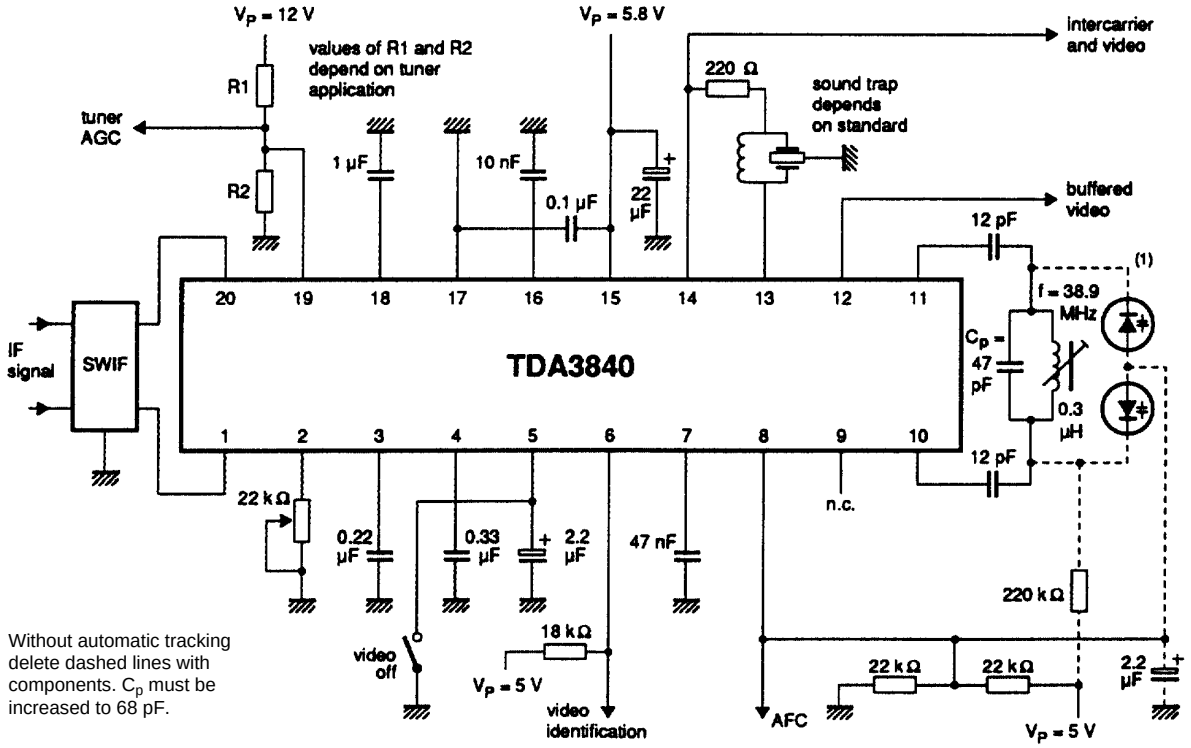


Fig.10 AFC interfacing for μP controlled systems.



(1) Without automatic tracking delete dashed lines with components. C_p must be increased to 68 pF.

Fig.11 Application circuit with automatic tracking function and notch filter (dashed lines).

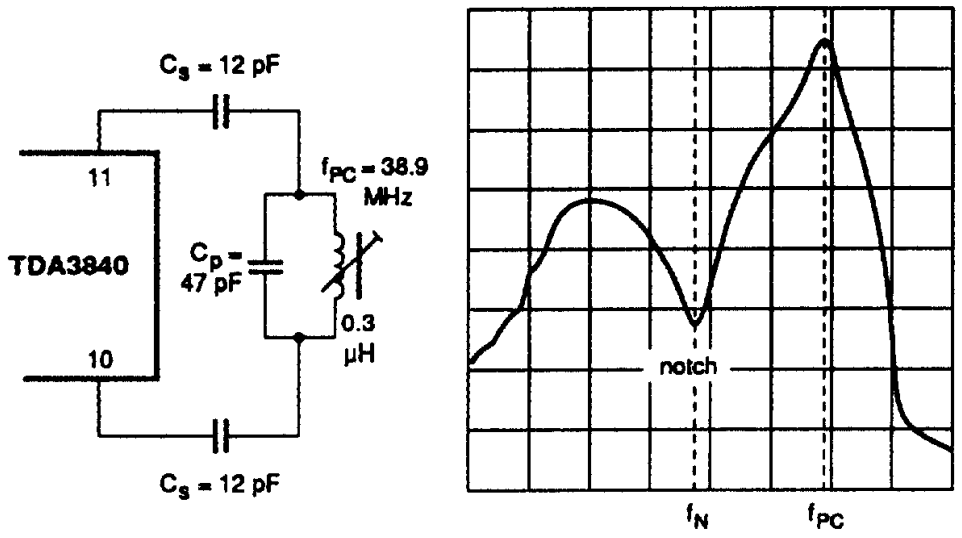


Fig.12 Reference circuit with notch filter for improved pulse response and better signal linearity.

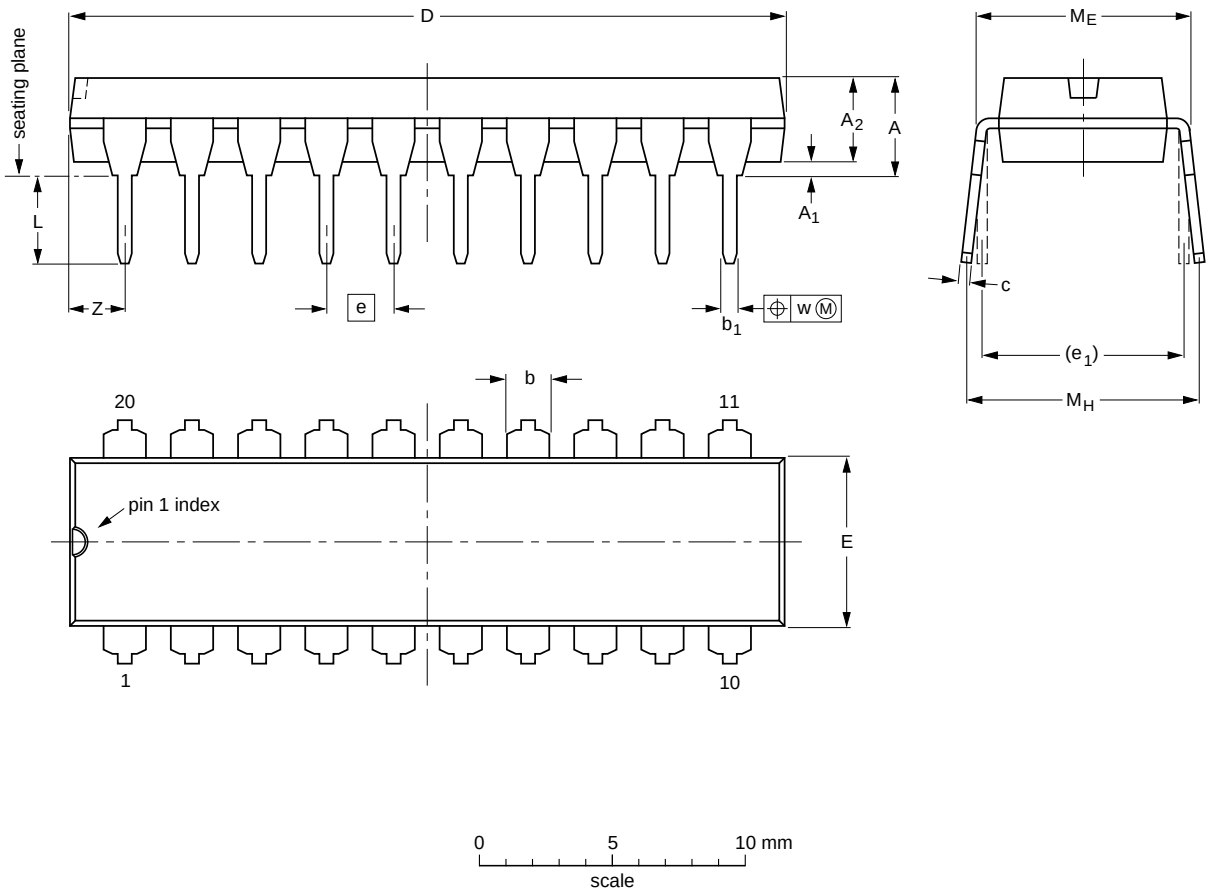
Note to figure 12

Recommended for reception of data signals e.g. in Teletext. Values in combination with SAW filter OFW G 1956 (Siemens). Curve shows combined frequency response of SAW filter and reference circuit.

For different standards C_s and C_p are calculated as follows: $C_S = 2C_p \left\{ \frac{f_{PC}^2}{f_N^2} - 1 \right\}$

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

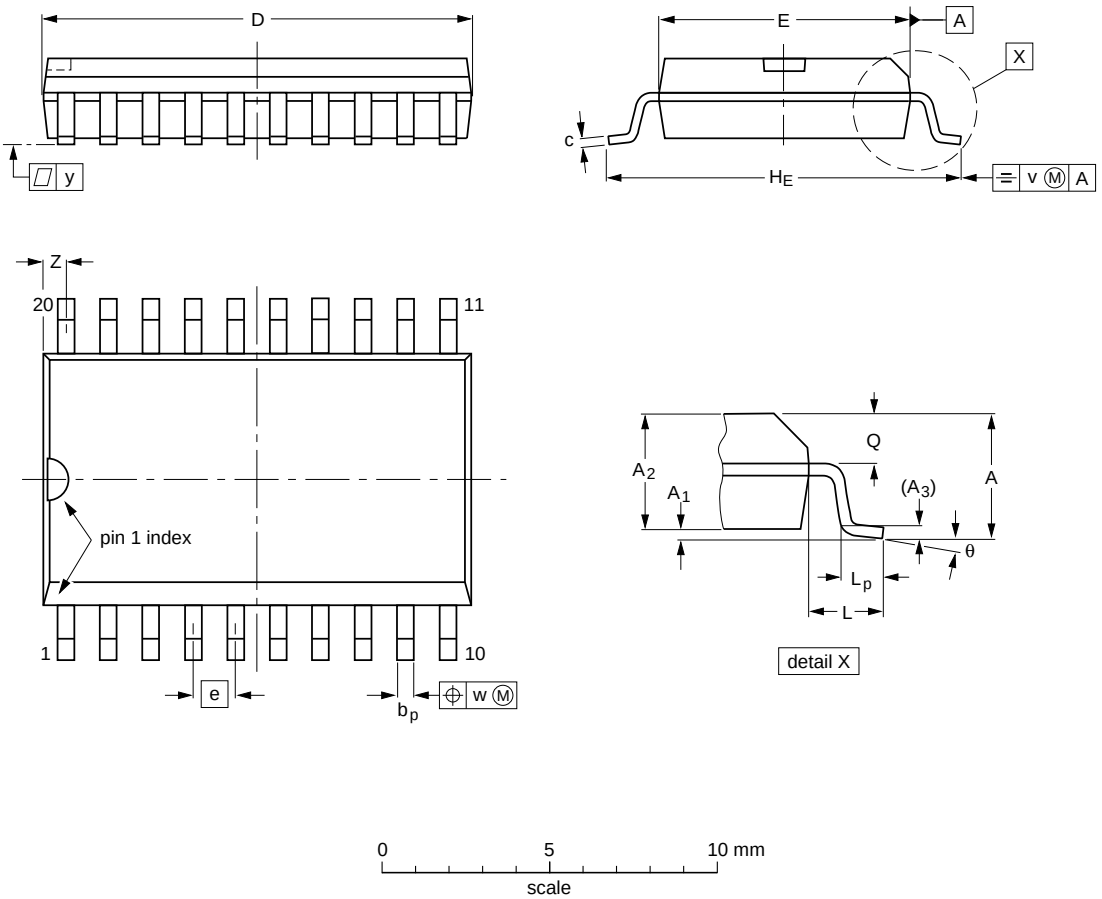
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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