

HD74HCT373/HD74HCT533

Octal D-type Transparent Latches (with 3-state outputs)/
Octal D-type Transparent Latches (with inverted 3-state outputs)

HITACHI

ADE-205-555 (Z)
1st. Edition
Sep. 2000

Description

When the latch enable input is high, the Q outputs of HD74HCT373 will follow the D inputs and the Q outputs of HD74HCT533 will follow the inversion of the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals present at the other inputs and the state of the storage elements.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (Data to Q) = 14 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

Output Control	Enable G	D	HD74HCT373 Q	HD74HCT533 $\overline{Q}$
L	H	H	H	L
L	H	L	L	H
L	L	X	No change	No change
H	X	X	Z	Z

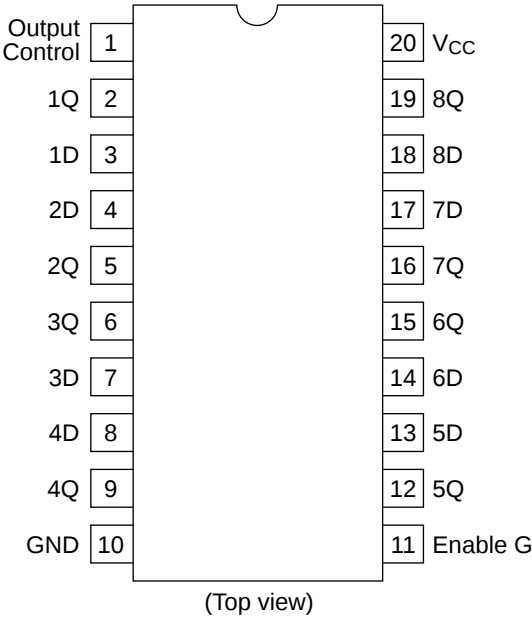
X : Irrelevant

Z : Off (high-impedance) state of a 3-state output.

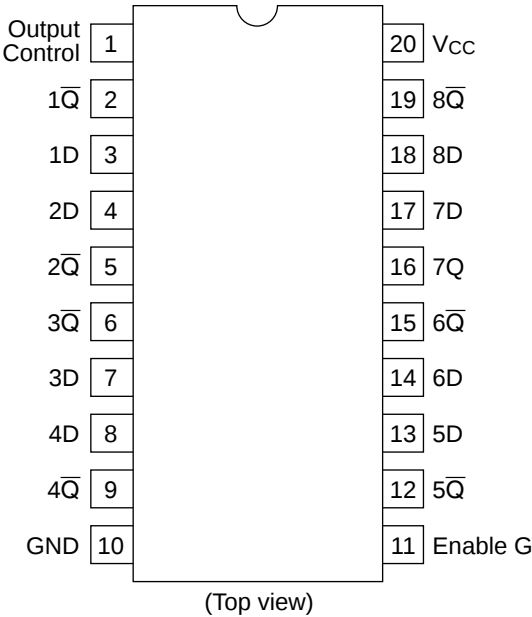
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Pin Arrangement

HD74HCT373

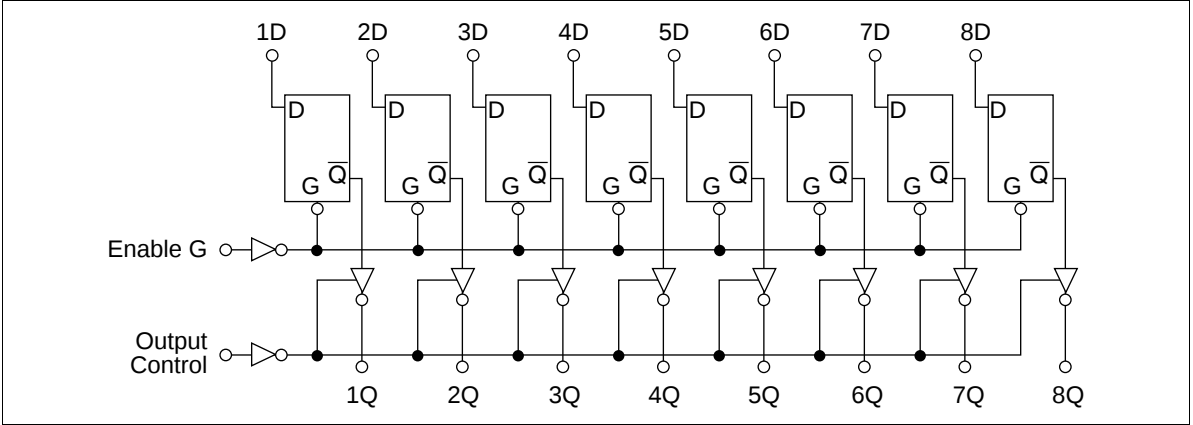


HD74HCT533

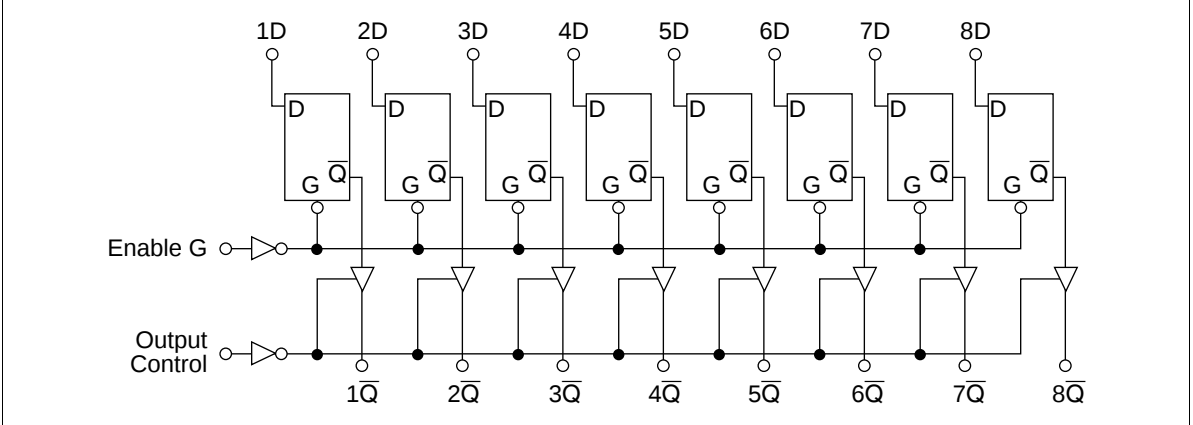


Block Diagram

HD74HCT373



HD74HCT533



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V _{CC}	−0.5 to +7.0	V
Input voltage	V _{IN}	−0.5 to V _{CC} + 0.5	V
Output voltage	V _{OUT}	−0.5 to V _{CC} + 0.5	V
DC current drain per pin	I _{OUT}	±35	mA
DC current drain per V _{CC} , GND	I _{CC} , I _{GND}	±75	mA
DC input diode current	I _{IK}	±20	mA
DC output diode current	I _{OK}	±20	mA
Power dissipation per package	P _T	500	mW
Storage temperature	T _{stg}	−65 to +150	°C

DC Characteristics

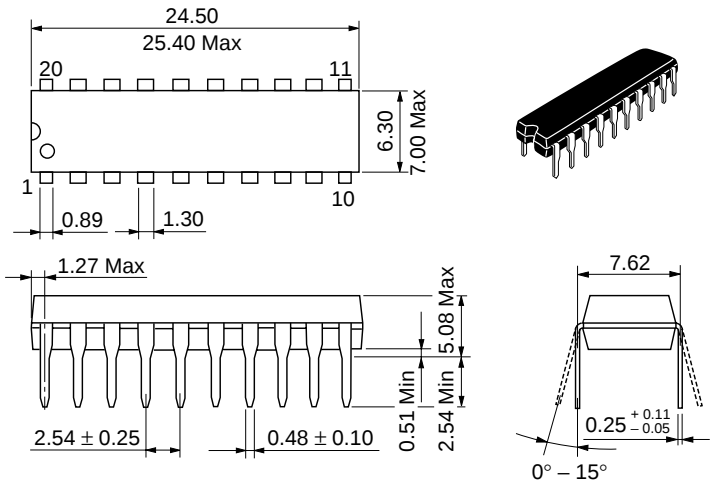
Item	Symbol	Ta = 25°C		Ta = −40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min	Max	V _{CC} (V)	
Input voltage	V _{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5
	V _{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5
Output voltage	V _{OH}	4.4	—	—	4.4	—	V	Vin = V _{IH} or V _{IL} I _{OH} = −20 μA
		4.18	—	—	4.13	—		I _{OH} = −6 mA
	V _{OL}	—	—	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA
		—	—	0.26	—	0.33		I _{OL} = 6 mA
Off-state output current	I _{OZ}	—	—	±0.5	—	±5.0	μA	5.5 Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND
Input current	I _{in}	—	—	±0.1	—	±1.0	μA	5.5 Vin = V _{CC} or GND
Quiescent current	I _{CC}	—	—	4.0	—	40	μA	5.5 Vin = V _{CC} or GND, Iout = 0 μA

AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min	Max		V _{CC} (V)	
Propagation delay time	t _{PLH}	—	13	30	—	38	ns	4.5	Latch control to Q
	t _{PHL}	—	16	30	—	38		4.5	
	t _{PLH}	—	14	25	—	31	ns	4.5	Data to Q
	t _{PHL}	—	12	25	—	31		4.5	
Output enable time	t _{ZL}	—	16	30	—	38	ns	4.5	
	t _{ZH}	—	15	30	—	38		4.5	
Output disable time	t _{LZ}	—	14	30	—	38	ns	4.5	
	t _{HZ}	—	16	30	—	38		4.5	
Setup time	t _{su}	20	—	—	25	—	ns	4.5	Data to latch control
Hold time	t _h	10	—	—	13	—	ns	4.5	Latch control to data
Pulse width	t _w	16	—	—	20	—	ns	4.5	Latch control, output control
Output rise/fall time	t _{TLH}	—	4	12	—	15	ns	4.5	
	t _{THL}	—	4	12	—	15			
Input capacitance	Cin	—	5	10	—	10	pF	—	

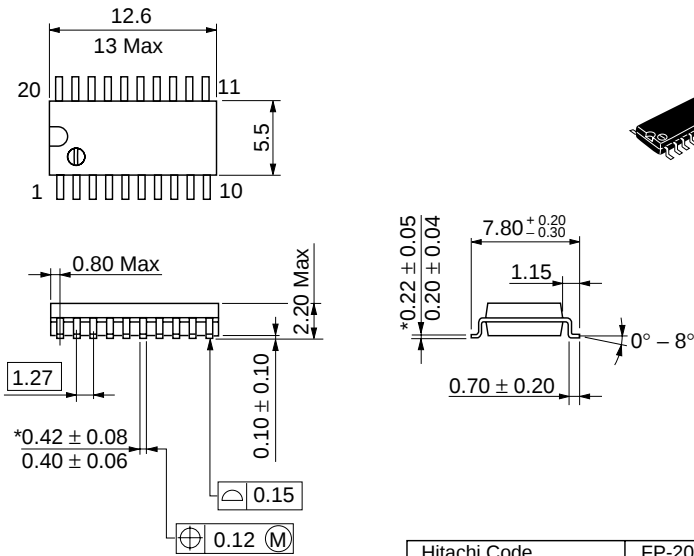
Package Dimensions

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Mass (reference value)	1.26 g

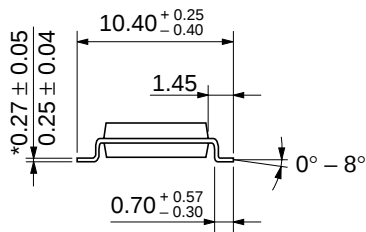
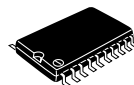
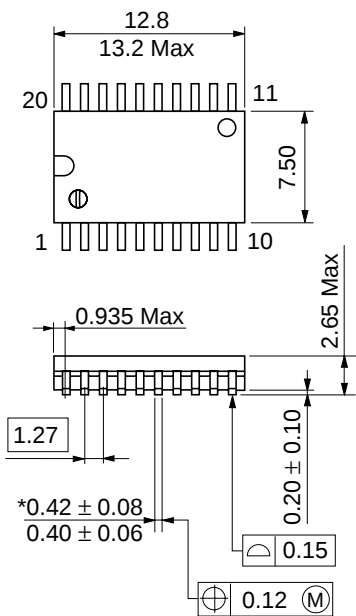
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.31 g

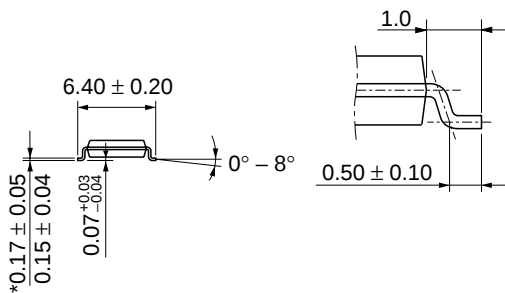
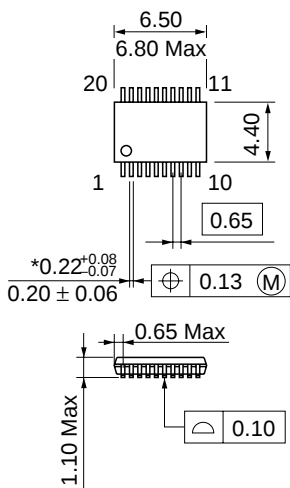
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.52 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.07 g

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