TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91FY27

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts $= (\overline{\text{NMI}}$, INT0, INTRTC), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontrollers
TMP91FY27U

1.   Outline and Features

TMP91FY27 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP91FY27U comes in a 64-pin flat package.Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)

- Instruction mnemonics are upward-compatible with TLCS-90/900

- 16 Mbytes of linear address space

- General-purpose registers and register banks

- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions

- Micro DMA: 4 channels (1.0 μs/2 bytes at 16 MHz)

(2) Minimum instruction execution time: 148 ns (at 27 MHz)

(3) Built-in RAM: 16 Kbytes
     Built-in ROM: 256-Kbyte Flash memory
                    2-Kbyte mask ROM (used for booting)

(4) External memory expansion

- Expandable up to 16 Mbytes (shared program/data area)

- Can simultaneously support 8-/16-bit width external data bus (Dynamic data bus sizing)

(5) 8-bit timers: 6 channels

(6) 16-bit timers: 1 channel

(7) General-purpose serial interface: 2 channels

- UART/Synchronous mode: 2 channels

- IrDA Ver.1.0 (115.2 kbps) mode selectable: 1 channel

(8) Serial bus interface: 1 channel

- I^2C bus mode/clock synchronous mode selectable

Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

(9) 10-bit AD converter (sample hold circuit is inside): 4 channels

(10) Watchdog timer

(11) Timer for real-time clock (RTC)

(12) Chip select/Wait controller: 4 blocks

(13) Interrupts: 34 interrupts

- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 21 internal interrupts: 7 priority levels are selectable
- 4 external interrupts: 7 priority levels are selectable
  (among 3 interrupts are selectable edge mode)

(14) Input/output ports: 53 pins

(15) Stand-by function

Three Halt modes: IDLE2 (programmable), IDLE1 and STOP

(16) Clock controller

- Clock gear function: Select a High-frequency clock fc to fc/16
- RTC (fs = 32.768 kHz)

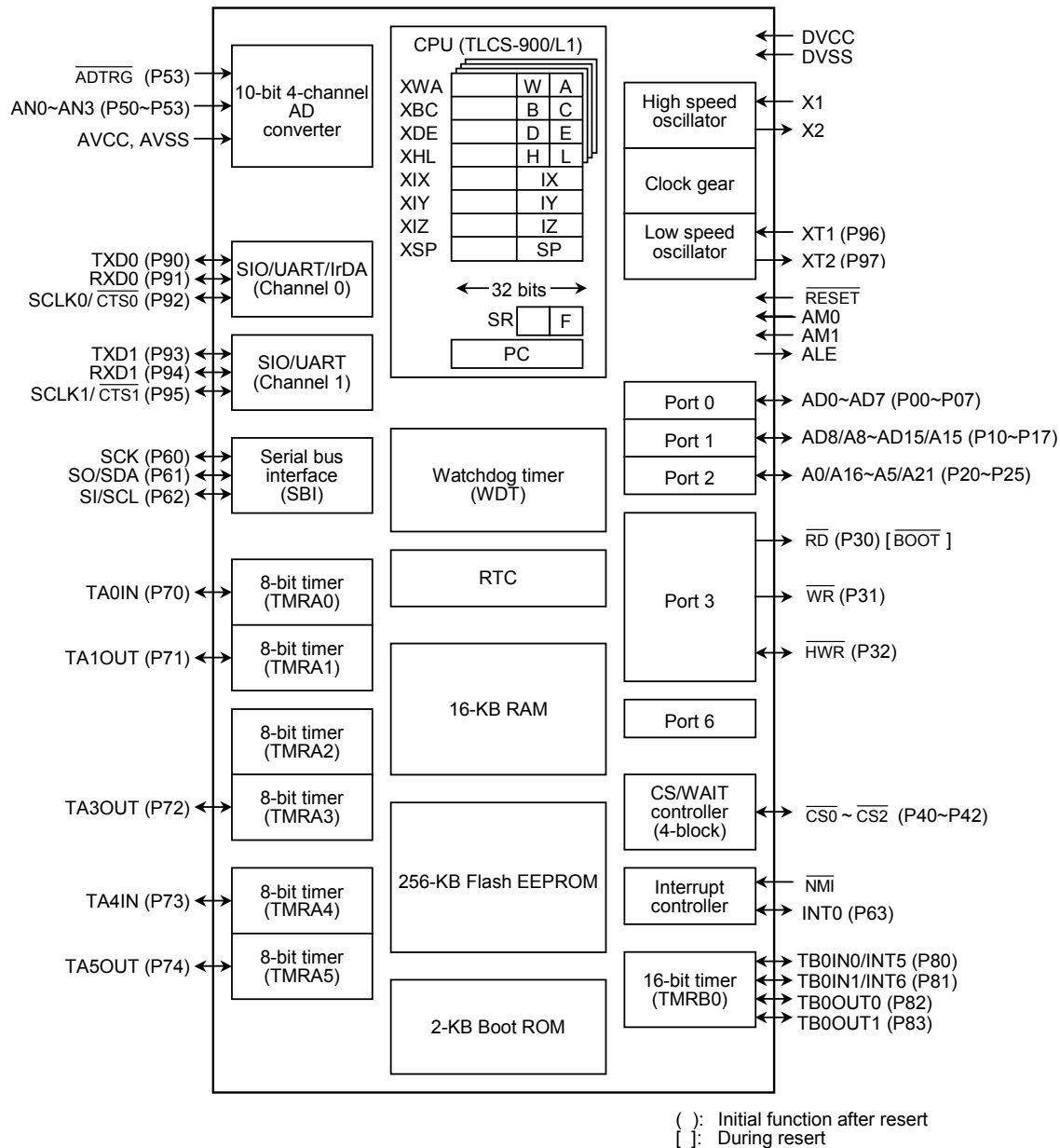(17) Operating voltage

- Vcc = 2.85 V to 3.6 V (fc max = 27 MHz)

(18) Package

- P-LQFP64-1010-0.50D

Figure 1.1 TMP91FY27 Block Diagram

( ): Initial function after resert
[ ]: During resert