Siliconix incorporated

DG535
16-Channel Wideband/Video Multiplexer

FEATURES

- −83 dB Single Channel Crosstalk at 5 MHz
- > 200 MHz Bandwidth
- 3 pF Input Capacitance
- 9 pF Output Capacitance
- Low Power (75 µw)
- 90 Ω (max) $r_{DS(ON)}$
- µP Interface Latches
- Fast Switching (300 ns)
- ESDS Protection > ±4000 V

BENEFITS

- Improved Isolation Between Channels
- Reduced Insertion Loss at High Frequencies
- Allows Formation of Large Matrices
- Minimizes System Power
- Simplifies µP Interface
- Improves Data Throughput

APPLICATIONS

- Video Switching/Routing
- High Speed Data Routing
- Wideband Signal Multiplexing
- Crosspoint Arrays
- Precision Data Acquisition
- FLIR Systems
- µP-Based Systems

DESCRIPTION

The DG535 is a 16-channel multiplexer designed for routing one of 16 wideband analog or digital input signals to a single output. It features low input and output capacitance, low ON resistance, and n-channel DMOS "T" switches, resulting in wide bandwidth, low crosstalk and high "OFF" isolation. The switch FETs were designed to pass signals in either direction, allowing the DG535 to be used as a demultiplexer as well as a multiplexer.

The DG535 includes on-board data latches and decode logic, facilitating a simplified microprocessor interface. Additional Chip Select and Enable inputs simplify addressing in larger matrices. The fast transition time of 300 ns (max) and low ON resistance 90 Ω (max) makes the DG535 ideal for multiplexing high speed signals through precision data acquisition systems. Single-supply operation and a low 75 µw power dissipation allow operation in battery powered systems and in multi-channel crosspoints and multiplexers with vastly reduced power supply requirements.

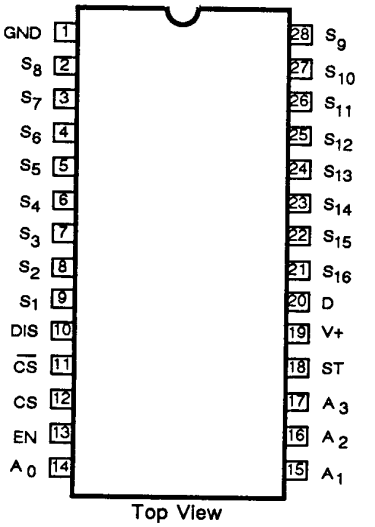
The technology used in the DG535 is called D/CMOS. This process combines low-capacitance DMOS FETs on the same substrate with dense, high-speed, low-power CMOS. The DMOS FETs are configured as "T" switches to improve OFF isolation and reduce crosstalk. The CMOS devices form all of the latches, decode logic and switch driver circuitry, resulting in a combination of high performance and high functional integration.

The DG535 is available in the plastic 28-lead DIP for the industrial, D suffix (−40 to 85°C), and the 28-lead side braze DIP for military, A suffix (−55 to 125°C) temperature range operations. For surface mount versions, see the DG536 data sheet.

For more information on the DG535, please refer to Siliconix Application Note AN86-1.

PIN CONFIGURATION

Dual-In-Line Package

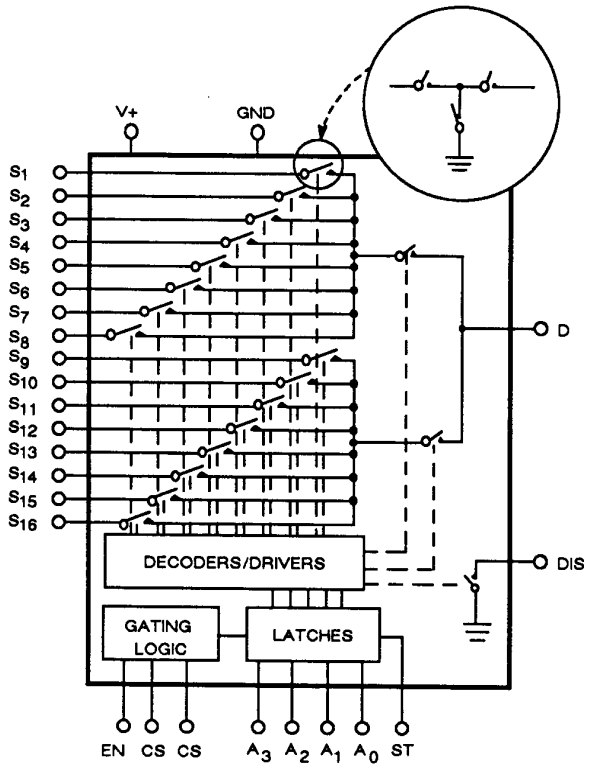


Top View

Ordering Information:

DG535AP DG535AP/883 Side Braze DIP	DG535DJ Plastic DIP

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

EN	CS	$\overline{CS}$	ST	A_3	A_2	A_1	A_0	Input Channel Selected	Disable Output
0	X	X							
X	0	X	1	X	X	X	X	NONE	HIGH Z
X	X	1							
				0	0	0	0	S1	
				0	0	0	1	S2	
				0	0	1	0	S3	
				0	0	1	1	S4	
				0	1	0	0	S5	
				0	1	0	1	S6	
				0	1	1	0	S7	
1	1	0	1	0	1	1	1	S8	LOW Z
				1	0	0	0	S9	
				1	0	0	1	S10	
				1	0	1	0	S11	
				1	0	1	1	S12	
				1	1	0	0	S13	
				1	1	0	1	S14	
				1	1	1	0	S15	
				1	1	1	1	S16	
X	X	X	0	X	X	X	X	Maintains previous switch condition	HIGH Z or LOW Z

Logic " 1 " : $V_{AH} \geq 10.5$ V

Logic " 0 " : $V_{AL} \leq 4.5$ V

1. LOW Z, HIGH Z = Impedance of Disable Output to GND. Disable output is current sink when any channel is selected.
2. Strobe Input (ST) is level triggered.

ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... -0.3 V to +18 V

Digital Inputs ..... (GND - 0.3 V) to (V+ plus 2 V)
..... or 20 mA, whichever occurs first

V_S,V_D ..... (GND - 0.3 V) to (V+ plus 2 V)
..... or 20 mA, whichever occurs first

Current (any terminal) Continuous ..... 20 mA

Current (S or D) Pulsed 1 ms 10% duty cycle .... 40 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
28-Pin Plastic DIP** ..... 625 mW
28-Pin Side Braze DIP*** ..... 1200 mW

* All leads welded or soldered to PC board.
** Derate 8.3 mW/°C above 75°C
*** Derate 16 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS [a]

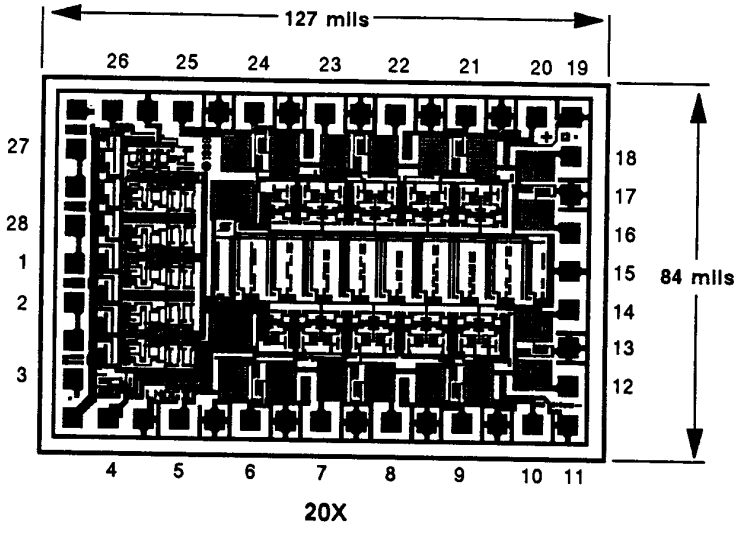
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, GND = 0 V, ST, CS = 10.5 V, $\overline{CS}$ = 4.5 V	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[c]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
SWITCH									
Analog Signal Range [d]	V_{ANALOG}		1		0	10	0	10	V
Drain - Source ON Resistance	$r_{DS(ON)}$	I_S = -1 mA, V_D = 3 V, V_{AH} = 4.5 V, V_{AL} = 10.5 V, Sequence Each Switch ON, EN = 10.5 V	1,3 2	55		90 120		90 120	Ω
Resistance Match Between Channels	$\Delta r_{DS(ON)}$		1			9		9	
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = 3 V, V_D = 0 V, EN = 4.5 V	1 2		-10 -100	10 100	-10 -100	10 100	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	V_S = 0 V, V_D = 3 V, EN = 4.5 V	1 2		-10 -500	10 500	-10 -100	10 100	
Total Switch ON Leakage Current	$I_{D(ON)}$	V_S = V_D = 3 V, EN = 10.5 V	1 2		-10 -1000	10 1000	-10 -100	10 100	
Disable Output	$R_{DISABLE}$	$I_{DISABLE}$ = 1 mA, EN = 10.5 V	1,3 2	100		200 250		200 250	Ω
INPUT									
Input Voltage High	V_{AIH}		1,2,3		10.5		10.5		V
Input Voltage Low	V_{AIL}		1,2,3			4.5		4.5	
Address Input Current	I_{AI}	V_{AI} = 0 V or 15 V	1,3 2	<0.01	-10 -100	10 100	-10 -100	10 100	nA
DYNAMIC									
ON State Input Cap.	$C_{S(ON)}$	V_D = V_S = 3 V	1	40					pF
OFF State Input Cap.	$C_{S(OFF)}$	V_S = 3 V	1	3					
OFF State Output Cap.	$C_{D(OFF)}$	V_D = 3 V	1	9					
Multiplexer Switching Time	t_{TRANS}	See Figure 4	1 2,3			300 300		300	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4	1 2,3		25 25		25		
EN, CS, $\overline{CS}$, ST Turn ON Time	t_{ON}	See Figures 2 & 3	1 2,3			300 300		300	
EN, CS, $\overline{CS}$ Turn OFF Time	t_{OFF}	See Figure 2	1 2,3			150 150		150	
Charge Injection	Q	See Figure 5	1	-35					pC

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, GND = 0 V, ST, CS = 10.5 V, $\overline{CS}$ = 4.5 V	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP[c]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
DYNAMIC (Cont'd)									
Single-Channel Crosstalk	$XTALK_{(SC)}$	R_{IN} = 75 Ω, R_L = 75Ω, f = 5 MHz, See Figure 9	1	-83					dB
Chip Disabled Crosstalk (See Figure 8)	$XTALK_{(CD)}$	R_L = 75 kΩ, f = 5 MHz, EN = 0.8 V	1	-60					
Adjacent Input Crosstalk (See Figure 10)	$XTALK_{(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz	1	-72					
All Hostile Crosstalk (See Figure 7)	$XTALK_{(AH)}$		1	-60					
Bandwidth	BW	R_L = 75 kΩ, See Figure 6	1	>200					MHz
SUPPLY									
Positive Supply Current	I+	Any One Channel Selected With Address Inputs at GND or V+	1,3 2	5		50 100		50 100	µA
Operating Supply Voltage Range	V+ to GND		1,2,3		10	16.5	10	16.5	V
MINIMUM INPUT TIMING REQUIREMENTS									
Strobe Pulse Width	t_{SW}	See Figure 1	1,2,3		200		200		ns
A_0, A_1, A_2, A_3, CS, $\overline{CS}$, EN Data Valid To Strobe	t_{DW}	See Figure 1	1,2,3		100		100		
A_0, A_1, A_2, A_3, CS, $\overline{CS}$, EN Data Valid After Strobe	t_{WD}	See Figure 1	1,2,3		50		50		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Analog signal range is measured from the GND pin to the designated Source (input) pin.

DIE TOPOGRAPHY



LNDG
695 Transistors 427, N-Channel
16 Diodes 268, P-Channel

Pad No.	Function
1	GND
2	S_8
3	S_7
4	S_6
5	S_5
6	S_4
7	S_3
8	S_2
9	S_1
10	DIS
11	CS
12	CS
13	EN
14	A_0
15	A_1
16	A_2
17	A_3
18	ST
19	V+
20	D
21	S_{16}
22	S_{15}
23	S_{14}
24	S_{13}
25	S_{12}
26	S_{11}
27	S_{10}
28	S_9

INPUT TIMING REQUIREMENTS

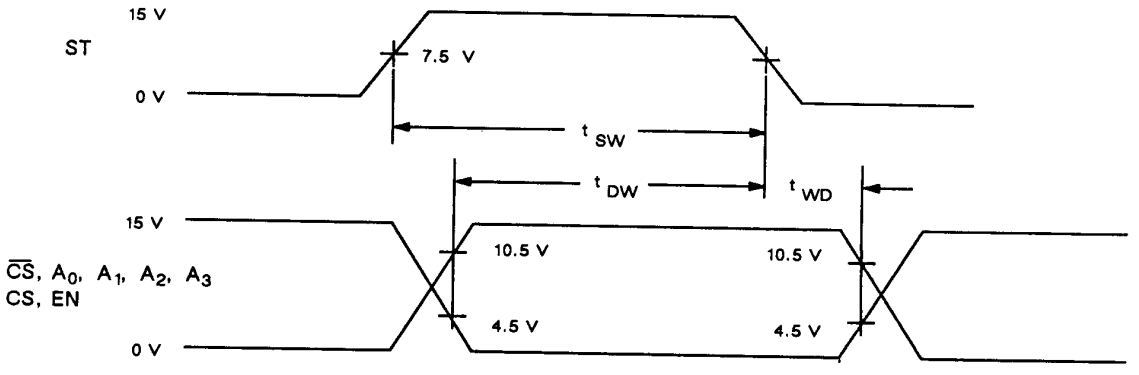


Figure 1

EN, CS, $\overline{CS}$, TURN ON/OFF TIME TEST CIRCUIT

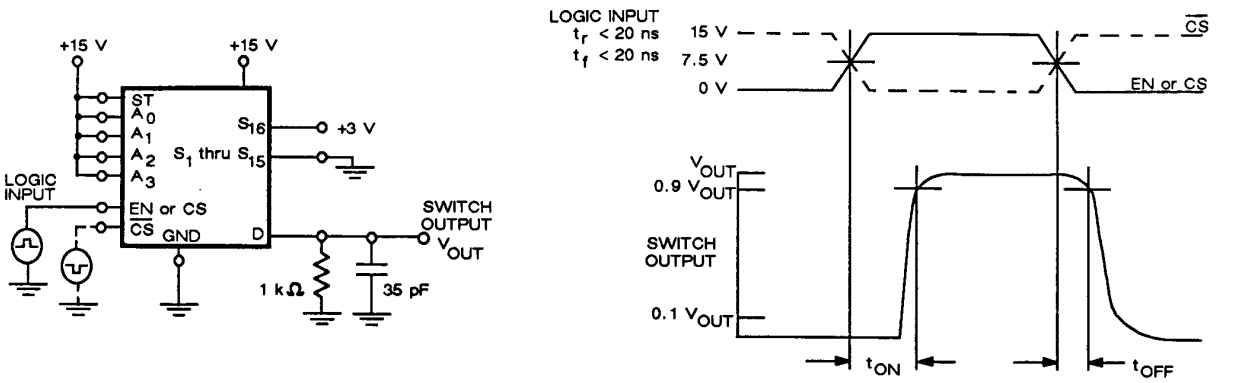


Figure 2

STROBE (ST) TURN ON TIME TEST CIRCUIT

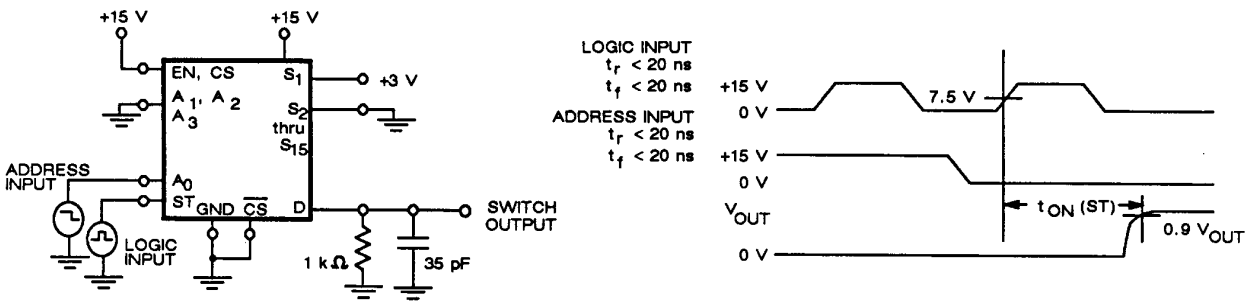


Figure 3

TRANSITION TIME and BREAK-BEFORE-MAKE INTERVAL TEST CIRCUIT

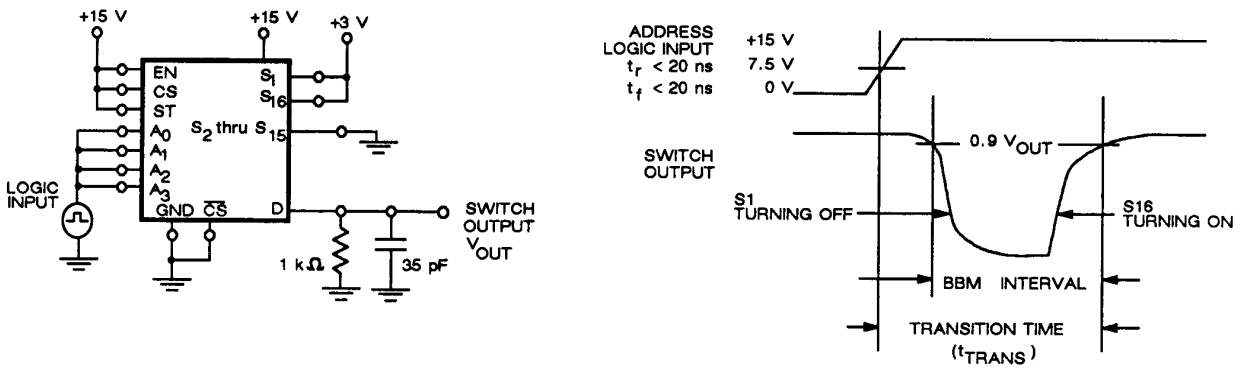


Figure 4

CHARGE INJECTION TEST CIRCUIT

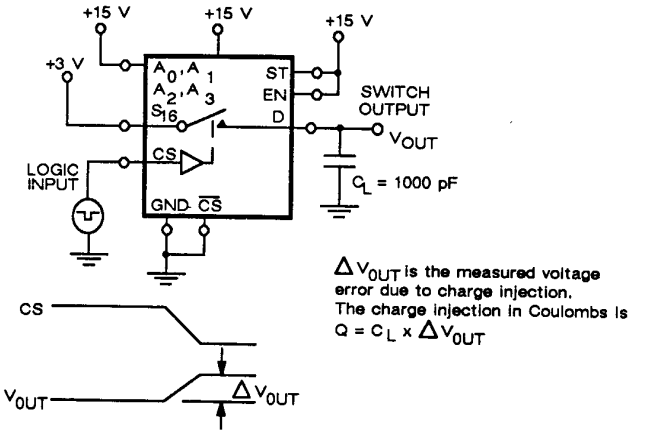


Figure 5

BANDWIDTH TEST CIRCUIT

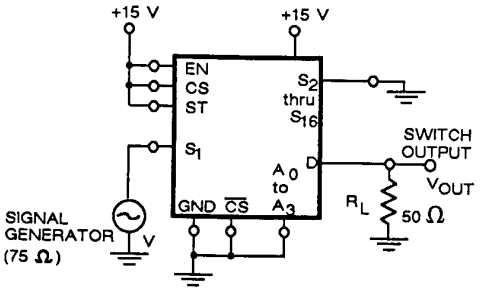


Figure 6

ALL HOSTILE CROSSTALK - X TALK (AH)

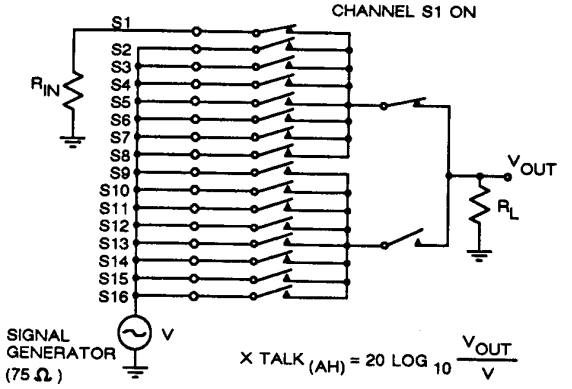


Figure 7

CHIP DISABLED CROSSTALK - X TALK (CD)

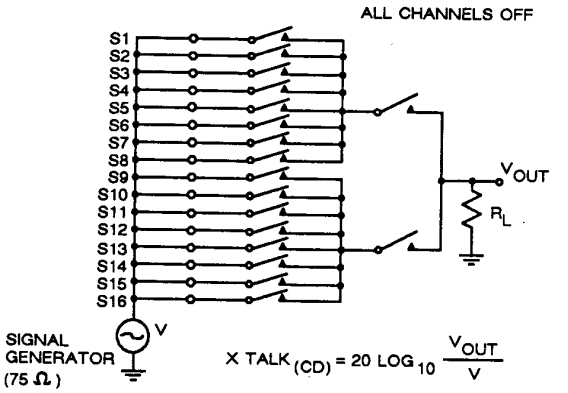
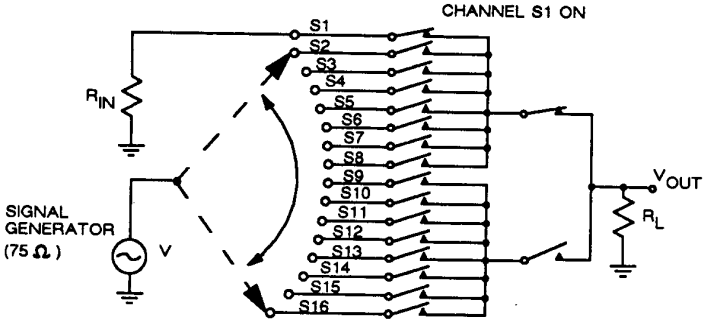


Figure 8

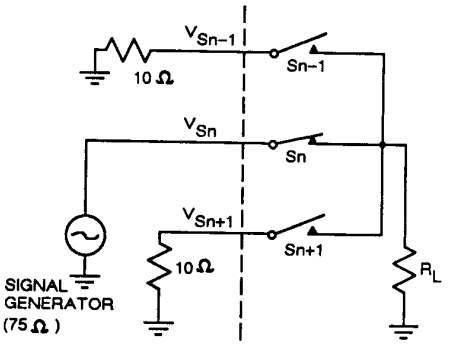
SINGLE CHANNEL CROSSTALK - X TALK (SC)



NOTES:
1. Any individual channel between S2 and S16 can be selected
2. X TALK (SC) = Average value of 20 LOG 10 VOUT / V is scanned sequentially from S2 to S16

Figure 9

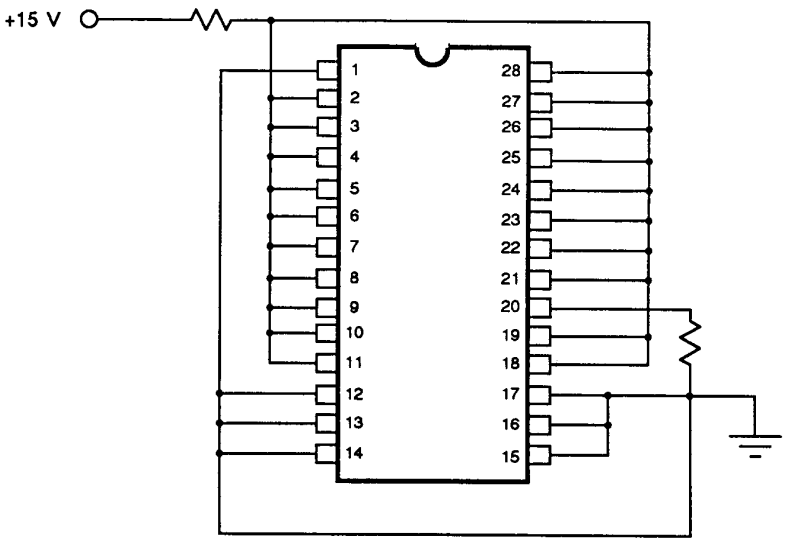
ADJACENT INPUT CROSSTALK - X TALK (AI)



$X\ TALK_{(AI)} = 20\ LOG_{10} \frac{V_{Sn-1}}{V_{Sn}}$ or $20\ LOG_{10} \frac{V_{Sn+1}}{V_{Sn}}$

Figure 10

BURN-IN CIRCUIT



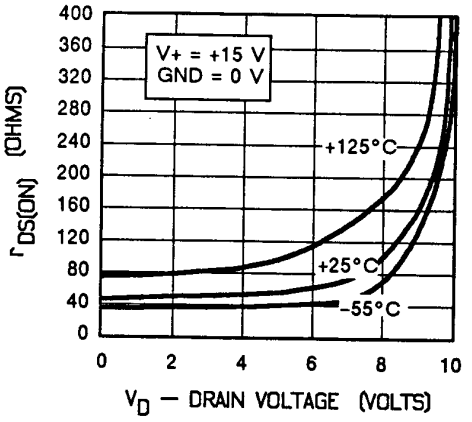
Note: All Resistors are 10 kΩ unless otherwise specified

PIN DESCRIPTION

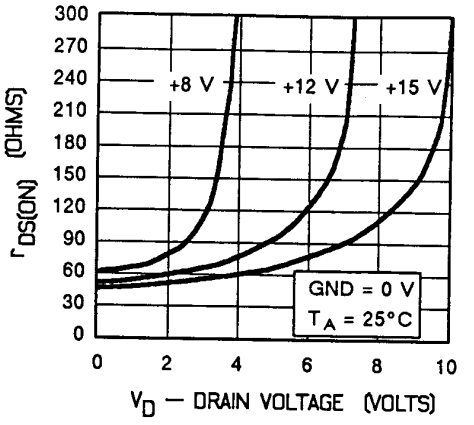
PIN NUMBER	SYMBOL	DESCRIPTION
1	GND	Analog Signal Ground and Most Negative Potential
2	S8	Channel 8 Analog Input
3	S7	Channel 7 Analog Input
4	S6	Channel 6 Analog Input
5	S5	Channel 5 Analog Input
6	S4	Channel 4 Analog Input
7	S3	Channel 3 Analog Input
8	S2	Channel 2 Analog Input
9	S1	Channel 1 Analog Input
10	DIS	Open drain high impedance output when DG535 is disabled (all channels OFF). When DG535 is enabled (any channel selected) this output is current sink to Analog GND.
11,12,13	$\overline{CS}$,CS,EN	Logic inputs to select required Multiplexer(s) when using several Multiplexers in a system
14 - 17	A_0 - A_3	Four binary address inputs that determine which one of the sixteen channels is selected.
18	ST	Strobe input that latches A_0, A_1, A_2, A_3, $\overline{CS}$,CS, EN
19	V+	Positive supply voltage
20	D	Analog output of Multiplexer or Analog input if device used in Demultiplexer configuration.
21	S16	Channel 16 Analog Input
22	S15	Channel 15 Analog Input
23	S14	Channel 14 Analog Input
24	S13	Channel 13 Analog Input
25	S12	Channel 12 Analog Input
26	S11	Channel 11 Analog Input
27	S10	Channel 10 Analog Input
28	S9	Channel 9 Analog Input

TYPICAL CHARACTERISTICS

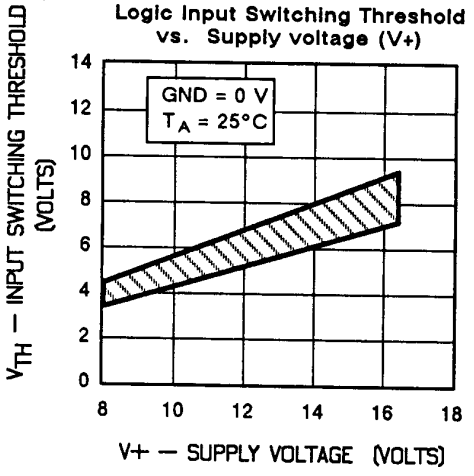
$r_{DS(ON)}$ vs. V_D and Temperature



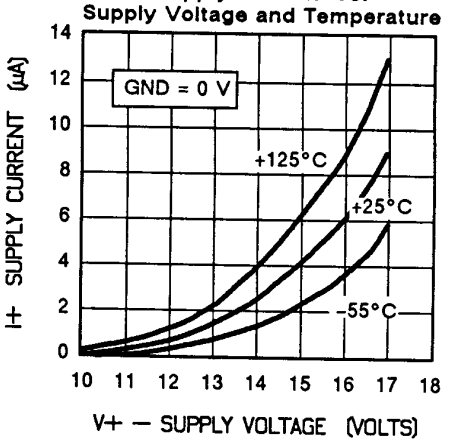
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



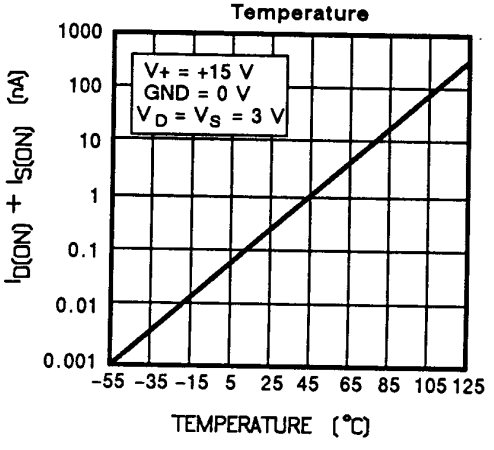
Logic Input Switching Threshold vs. Supply voltage (V+)



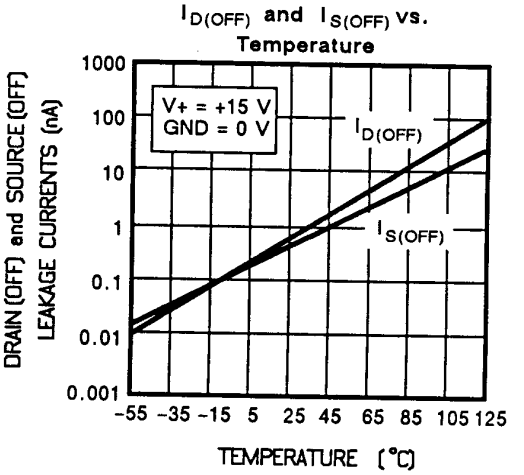
Supply Current vs. Supply Voltage and Temperature



$I_{D(ON)} + I_{S(ON)}$ vs. Temperature

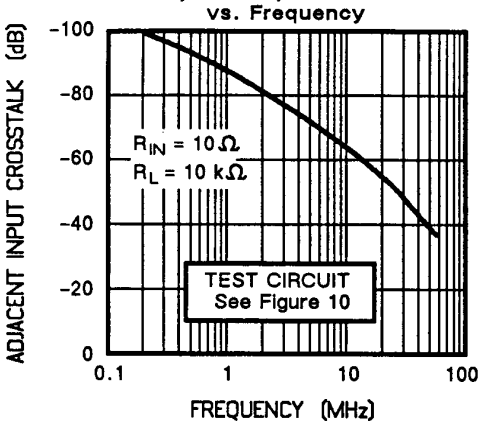


$I_{D(OFF)}$ and $I_{S(OFF)}$ vs. Temperature

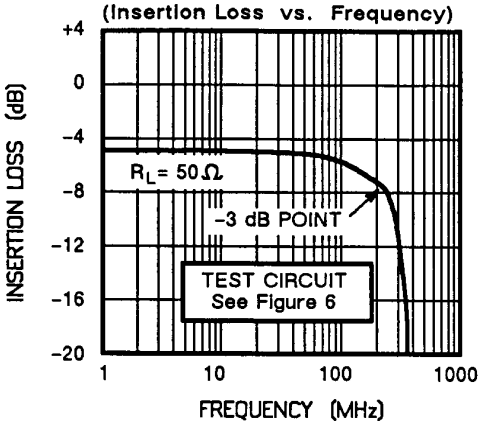


TYPICAL CHARACTERISTICS (Cont'd)

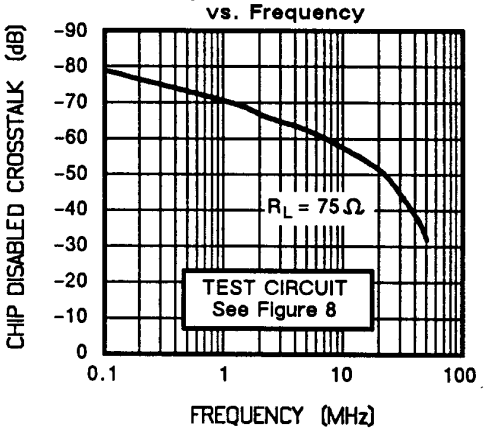
Adjacent Input Crosstalk vs. Frequency



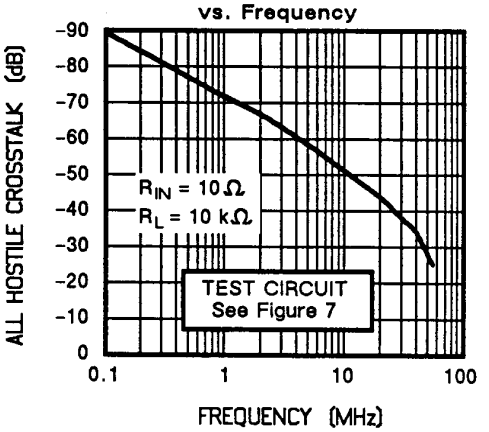
-3 dB Bandwidth (Insertion Loss vs. Frequency)



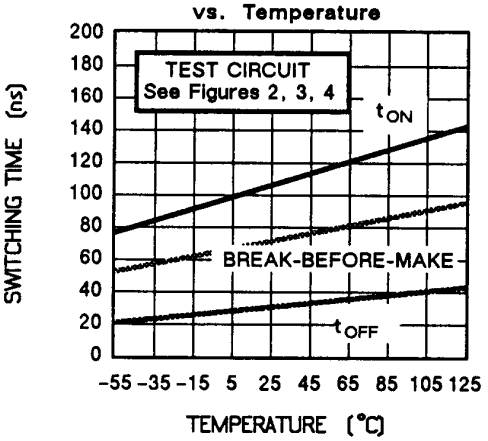
Chip Disabled Crosstalk vs. Frequency



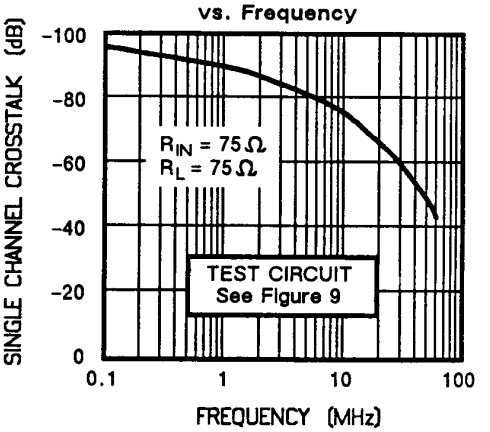
All Hostile Crosstalk vs. Frequency



t_{ON}, t_{OFF} and Break-Before-Make vs. Temperature



Single Channel Crosstalk vs. Frequency



DETAILED DESCRIPTION

The DG535 is a 16-channel single-ended multiplexer with on-chip address logic and control latches.

The circuit connects one of sixteen inputs (S1, S2,...S16) to a common output (D) under the control of a 4 bit binary address (A_0 to A_3). The specific input channel selected for each address is given in the Truth Table.

All four address inputs have on-chip data latches which are controlled by the Strobe (ST) input. These latches are transparent when Strobe is high but they maintain the chosen address when Strobe goes low. To facilitate easy microprocessor control in large matrices a choice of 3 independent logic inputs (EN, CS and $\overline{CS}$) are provided on chip. These inputs are gated together (see Figure 11) and only when EN = CS = 1 and $\overline{CS}$ = 0 is true can an output switch be selected by the appropriate address input (A_0 to A_3). This necessary logic condition can then be latched by Strobe (ST) going low.

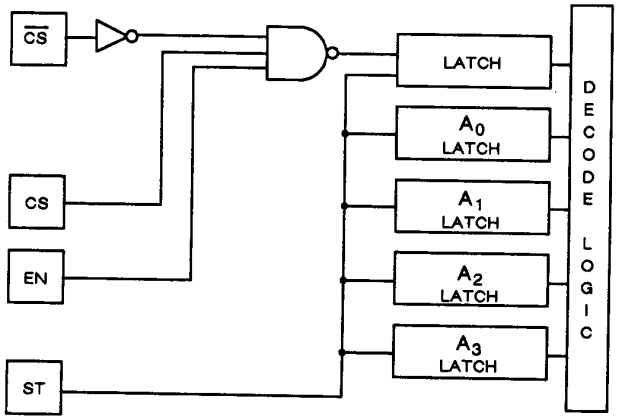


Figure 11. $\overline{CS}$, CS, EN, ST Control Logic

Break-before-make switching is included to prevent momentary shorting of an input channel when changing from one input to another.

The device features a two-level switch arrangement whereby two banks of eight switches (first level) are connected via two series switches (second level) to a common DRAIN output.

In order to improve crosstalk all sixteen first level switches are configured as "T" switches (see Figure 12).

With this method SW2 operates out of phase with SW1 and SW3. In the ON condition SW1 and SW3 are closed with SW2 open whereas in the OFF condition SW1 and SW3 are open and SW2 closed. In the OFF condition the input to SW3 is effectively the isolation leakage of SW1 working into the ON resistance of SW2 (typically 200 Ω).

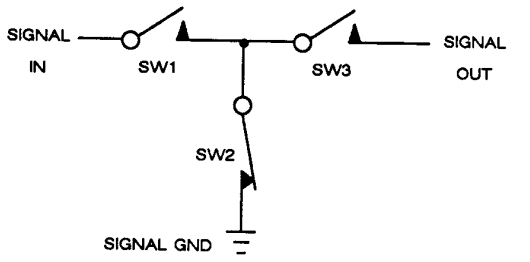


Figure 12. " T " Switch Arrangement

The two second level series switches further improve crosstalk and help to minimize output capacitance.

The DIS output (Pin 7) can be used to signal external circuitry. DIS is a high impedance to GND when no channel is selected and a low impedance to GND when any one channel is selected.

The DG535 has extensive applications where any high frequency video, audio or digital signals are switched or routed. Exceptional crosstalk and bandwidth performance is achieved by using N channel DMOS FETs for the "T" and series switches.

A cross section of a switch is shown in Figure 13.

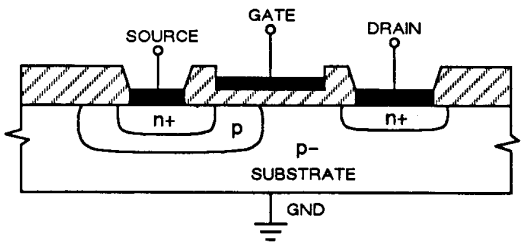


Figure 13. Cross-Section of a Single DMOS Switch

It can clearly be seen from Figure 13 that there exists a PN junction between the substrate and the drain/source terminals.

Should a signal which is negative with respect to the substrate (GND pin) be connected to a source or drain terminal, then the PN junction will become forward biased and current will flow between the signal source and GND. This effective shorting of the signal source to GND will not necessarily cause any damage to the device, provided that the total current flowing is less than the maximum rating, (i.e. 20 mA).

Since no PN junctions exist between the signal path and V+, positive overvoltages are not a problem, unless the breakdown voltage of the DMOS source terminal (see Figure 13) (+18 V) is exceeded. Positive overvoltage conditions must not exceed +18 V with respect to the GND pin. If this condition is possible (e.g. transients in the signal), then a diode or Zener clamp may be used to prevent breakdown occuring.

The overvoltage conditions described may exist if the supplies are collapsed while a signal is present on the inputs. If this condition is unavoidable, then the necessary steps outlined above should be taken to protect the device

DC BIASING

To avoid negative overvoltage conditions and subsequent distortion of analog signals, dc biasing is necessary. Biasing is not required, however, in applications where signals are always positive with respect to the GND or substrate connection, or in applications involving multiplexing of low level (up to ± 200 mV) signals, where forward biasing of the PN substrate-source/drain terminals would not occur.

Biasing can be accomplished in a number of ways, the simplest of which is a resistive potential divider and a few dc blocking capacitors as shown in Figure 14.

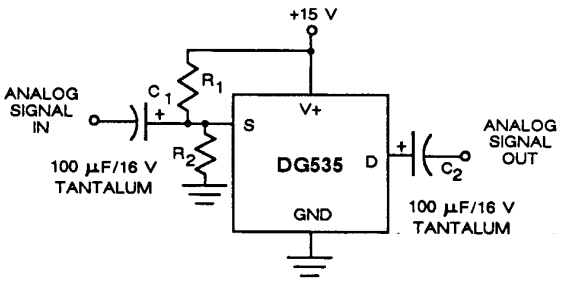


Figure 14. Simple Bias Circuit

R1 and R2 are chosen to suit the appropriate biasing requirements. For video applications, approximately 3 V of bias is required for optimal differential gain and phase performance. Capacitor C1 blocks the DC bias voltage from being coupled back to the analog signal source and C2 blocks the DC bias from the output signal. Both C1 and C2 should be tantalum or ceramic disc type capacitors in order to operate efficiently at high frequencies.

Active bias circuits are recommended if rapid switching time between channels is required.

An alternative method would be to offset the supply voltages (see Figure 15).

Decoupling would have to be applied to the negative supply to ensure that the substrate is well referenced to signal ground. Again the capacitors should be of a type offering good high frequency characteristics.

Level shifting of the logic signals may be necessary using this offset supply arrangement.