

MC74LVX259

8-Bit Addressable Latch/1-of-8 Decoder CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74LVX259 is an 8-bit Addressable Latch fabricated with silicon gate CMOS technology.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The LVX259 is designed for general purpose storage applications in digital systems. The device has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode, all outputs are LOW and unaffected by the address and data inputs. When operating the LVX259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The MC74LVX259 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74LVX259 to be used to interface 5.0 V circuits to 3.0 V circuits.

Features

- High Speed: $t_{PD} = 7.0$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC}
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- Pb-Free Packages are Available*

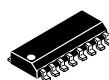
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



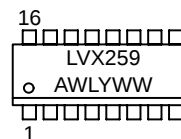
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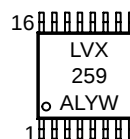
MARKING DIAGRAMS



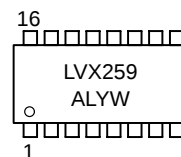
SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
M SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
Y = Year
WW or W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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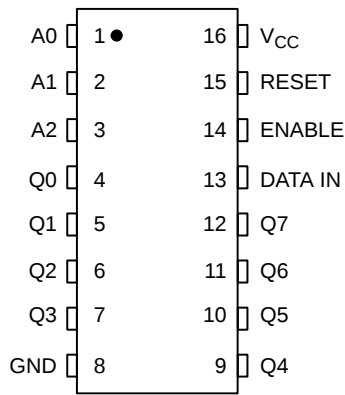


Figure 1. Pin Assignment

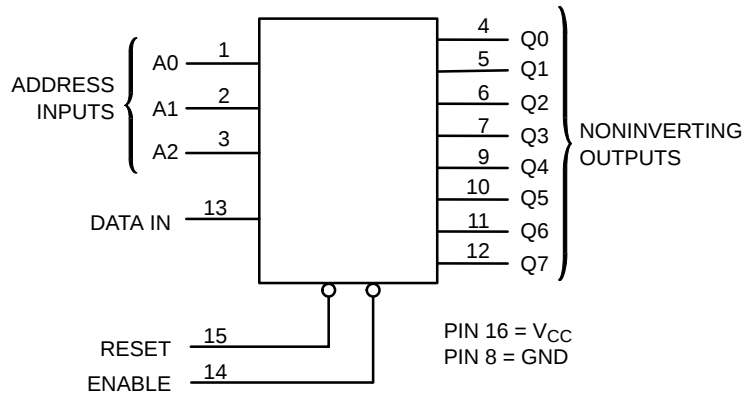


Figure 2. Logic Diagram

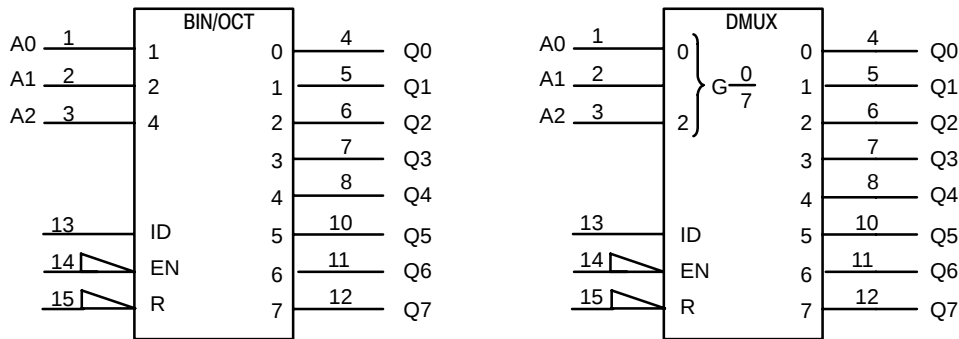


Figure 3. IEC Logic Symbol

MODE SELECTION TABLE

Enable	Reset	Mode
L	H	Addressable Latch
H	H	Memory
L	L	8-Line Demultiplexer
H	L	Reset

LATCH SELECTION TABLE

Address Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

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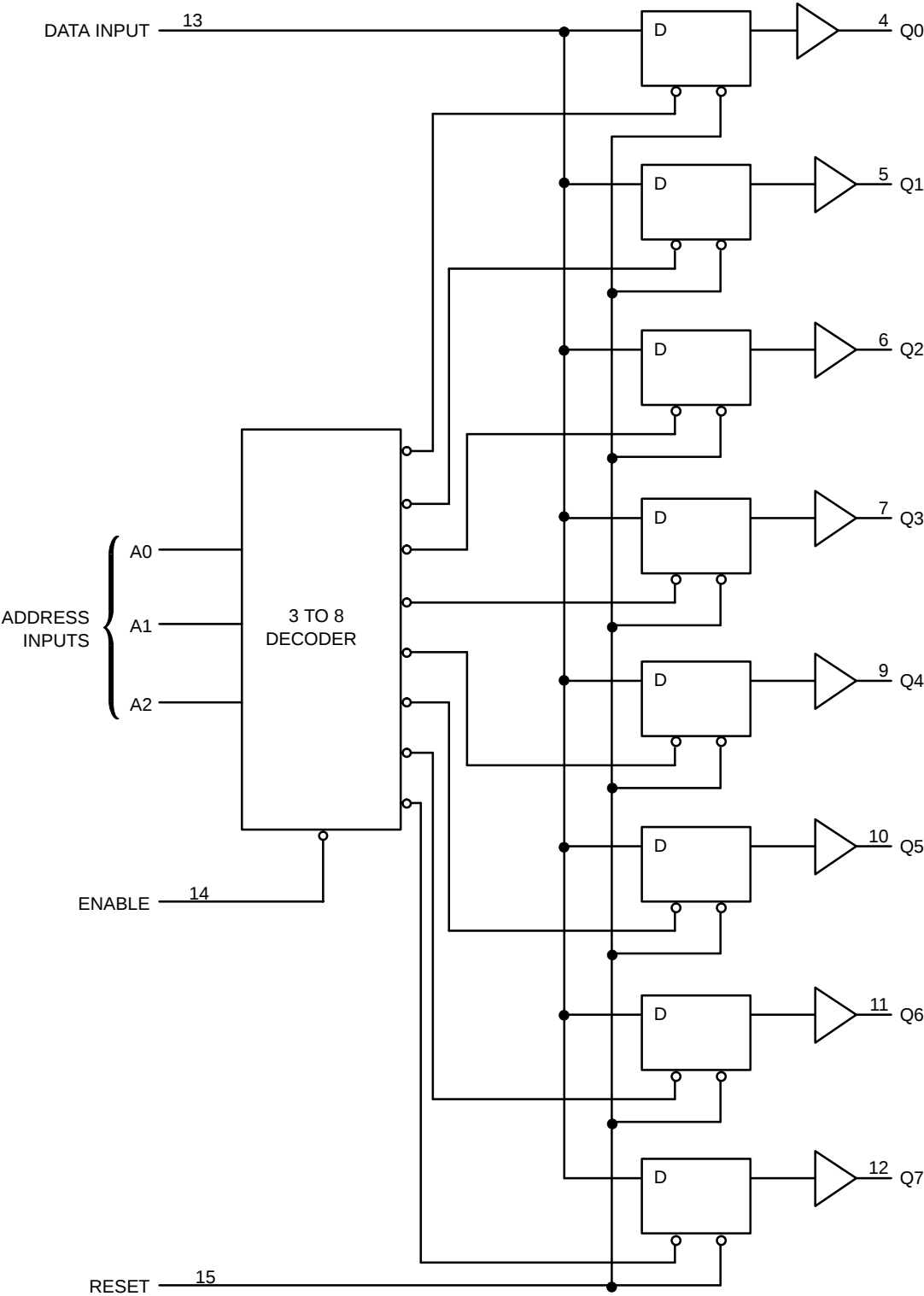


Figure 4. Expanded Logic Diagram

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	Digital Input Voltage	-0.5 to +7.0	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	Input Diode Current	-20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP 200 180	mW
T_{STG}	Storage Temperature Range	-65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3) >2000 >200 >2000	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 4) ± 300	mA
θ_{JA}	Thermal Resistance, Junction-to-Ambient	SOIC Package TSSOP 143 164	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range, all Package Types	−40	85	°C
t _r , t _f	Input Rise or Fall Time	V _{CC} = 3.3 V ± 0.3 V		ns/V

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DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 3.6	0.75 V _{CC} 0.7 V _{CC} 0.7 V _{CC}	– – –	– – –	0.75 V _{CC} 0.7 V _{CC} 0.7 V _{CC}	– – –	V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 3.6	– – –	– – –	0.25 V _{CC} 0.3 V _{CC} 0.3 V _{CC}	– – –	0.25 V _{CC} 0.3 V _{CC} 0.3 V _{CC}	V
V _{OH}	High-Level Output Voltage	I _{OH} = –50 μA	2.0	1.9	2.0	–	1.9	–	V
		I _{OH} = –50 μA	3.0	2.9	3.0	–	2.9	–	
		I _{OH} = –4 mA	3.0	2.58	–	–	2.48	–	
V _{OL}	Low-Level Output Voltage	I _{OL} = 50 μA	2.0	–	0.0	0.1	–	0.1	V
		I _{OL} = 50 μA	3.0	–	0.0	0.1	–	0.1	
		I _{OL} = 4 mA	3.0	–	–	0.36	–	0.44	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 3.6	–	–	±0.1	–	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per package)	V _{IN} = V _{CC} or GND	3.6	1.0	1.0	2.0	–	–	μA

AC ELECTRICAL CHARACTERISTICS Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions		T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Data to Output (Figures 5 and 9)	V _{CC} = 2.7 V	C _L = 15pF	–	6.3	9.0	1.0	12.0	ns
			C _L = 50pF	–	9.0	14.0	1.0	15.0	
		V _{CC} = 3.3 V ± 0.3 V	C _L = 15pF C _L = 50pF	– –	5.6 8.0	8.0 12.0	1.0 1.0	11.0 14.0	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Address Select to Output (Figures 6 and 9)	V _{CC} = 2.7 V	C _L = 15pF	–	6.3	9.0	1.0	12.0	ns
			C _L = 50pF	–	9.0	14.0	1.0	15.0	
		V _{CC} = 3.3 V ± 0.3 V	C _L = 15pF C _L = 50pF	– –	5.6 8.0	8.0 12.0	1.0 1.0	11.0 14.0	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Enable to Output (Figures 7 and 9)	V _{CC} = 2.7 V	C _L = 15pF	–	6.3	9.0	1.0	12.0	ns
			C _L = 50pF	–	9.0	14.0	1.0	15.0	
		V _{CC} = 3.3 V ± 0.3 V	C _L = 15pF C _L = 50pF	– –	5.6 8.0	9.0 12.0	1.0 1.0	11.0 14.0	
t _{PHL}	Maximum Propagation Delay, Reset to Output (Figures 7 and 9)	V _{CC} = 2.7 V	C _L = 15pF	–	6.3	9.0	1.0	12.0	ns
			C _L = 50pF	–	9.0	14.0	1.0	15.0	
		V _{CC} = 3.3 V ± 0.3 V	C _L = 15pF C _L = 50pF	– –	5.6 8.0	9.0 12.0	1.0 1.0	11.0 14.0	
C _{IN}	Maximum Input Capacitance			–	6	10	–	10	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	Typical @ 25°C, V _{CC} = 3.3 V							pF
		30							

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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TIMING REQUIREMENTS Input $t_r = t_f = 3.0$ ns

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
t_w	Minimum Pulse Width, Reset or Enable (Figure 8)	$V_{CC} = 2.7\text{ V}$	4.5	–	–	5.0	–	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	4.5	–	–	5.0	–	
t_{su}	Minimum Setup Time, Address or Data to Enable (Figure 8)	$V_{CC} = 2.7\text{ V}$	4.0	–	–	4.0	–	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	3.0	–	–	3.0	–	
t_h	Minimum Hold Time, Enable to Address or Data (Figure 7 or 8)	$V_{CC} = 2.7\text{ V}$	2.0	–	–	2.0	–	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2.0	–	–	2.0	–	
t_r, t_f	Maximum Input, Rise and Fall Times (Figure 5)	$V_{CC} = 2.7\text{ V}$	–	–	400	–	300	ns
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	–	–	300	–	300	

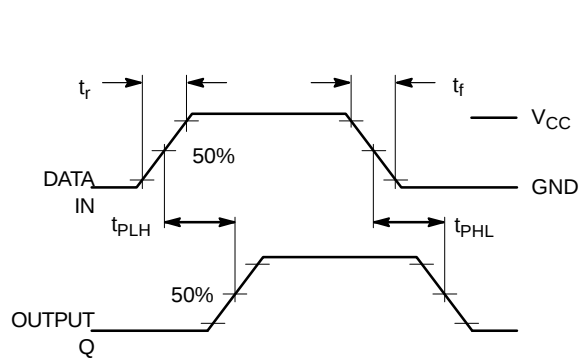


Figure 5. Switching Waveform

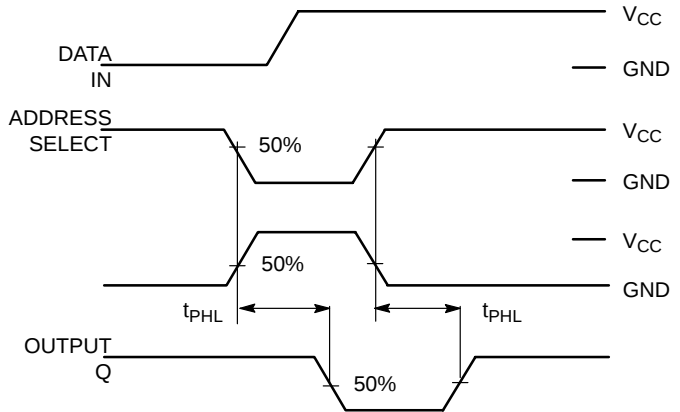


Figure 6. Switching Waveform

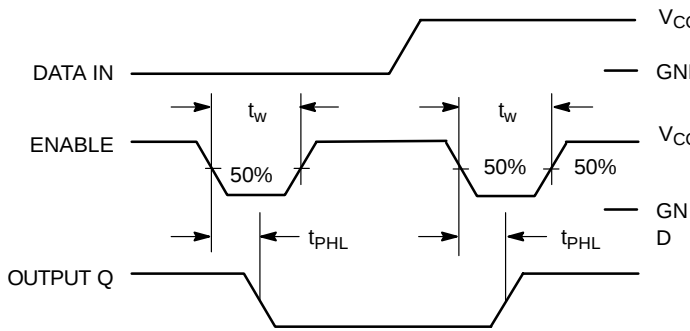


Figure 7. Switching Waveform

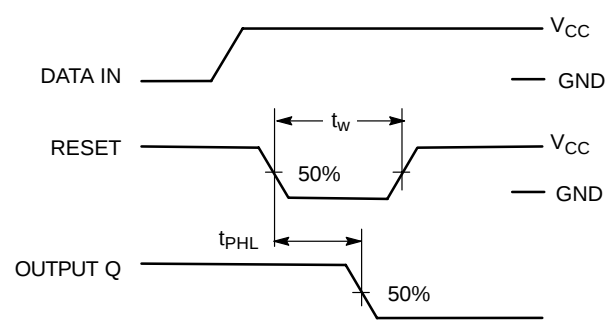


Figure 8. Switching Waveform

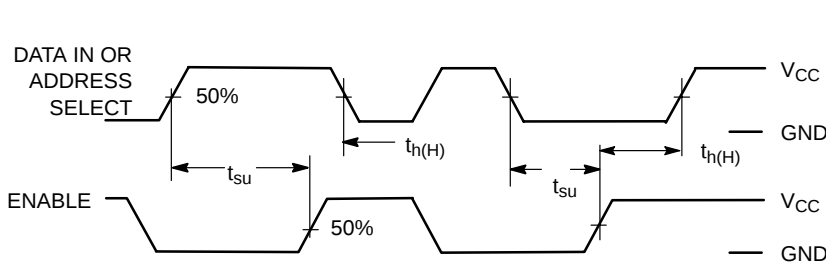
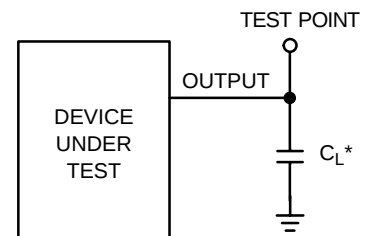


Figure 9. Switching Waveform



*Includes all probe and jig capacitance

Figure 10. Test Circuit

MC74LVX259

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVX259D	SOIC-16	48 Units / Rail
MC74LVX259DG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74LVX259DR2	SOIC-16	2500 Tape & Reel
MC74LVX259DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LVX259DT	TSSOP-16*	96 Units / Rail
MC74LVX259DTR2	TSSOP-16*	2500 Tape & Reel
MC74LVX259M	SOEIAJ-16	50 Units / Rail
MC74LVX259MG	SOEIAJ-16 (Pb-Free)	50 Units / Rail
MC74LVX259MEL	SOEIAJ-16	2000 Tape & Reel
MC74LVX259MELG	SOEIAJ-16 (Pb-Free)	2000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

EMBOSSED CARRIER DIMENSIONS (See Notes 6 and 7)

Tape Size	B ₁ Max	D	D ₁	E	F	K	P	P ₀	P ₂	R	T	W
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 -0.0 (0.059" +0.004 -0.0)	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024)	8.3 mm (0.327)
12 mm	8.2 mm (0.323")		1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")					12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642)
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957)

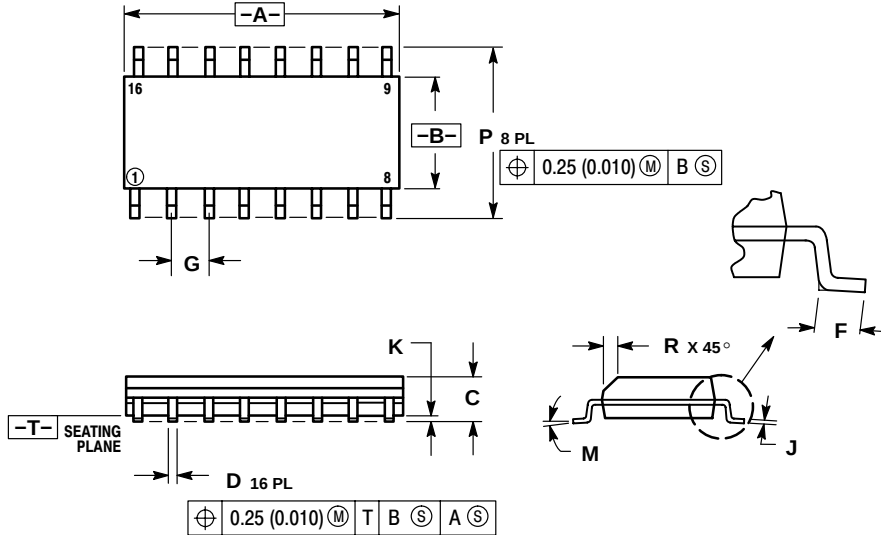
6. Metric Dimensions Govern—English are in parentheses for reference only.

7. A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

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PACKAGE DIMENSIONS

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J

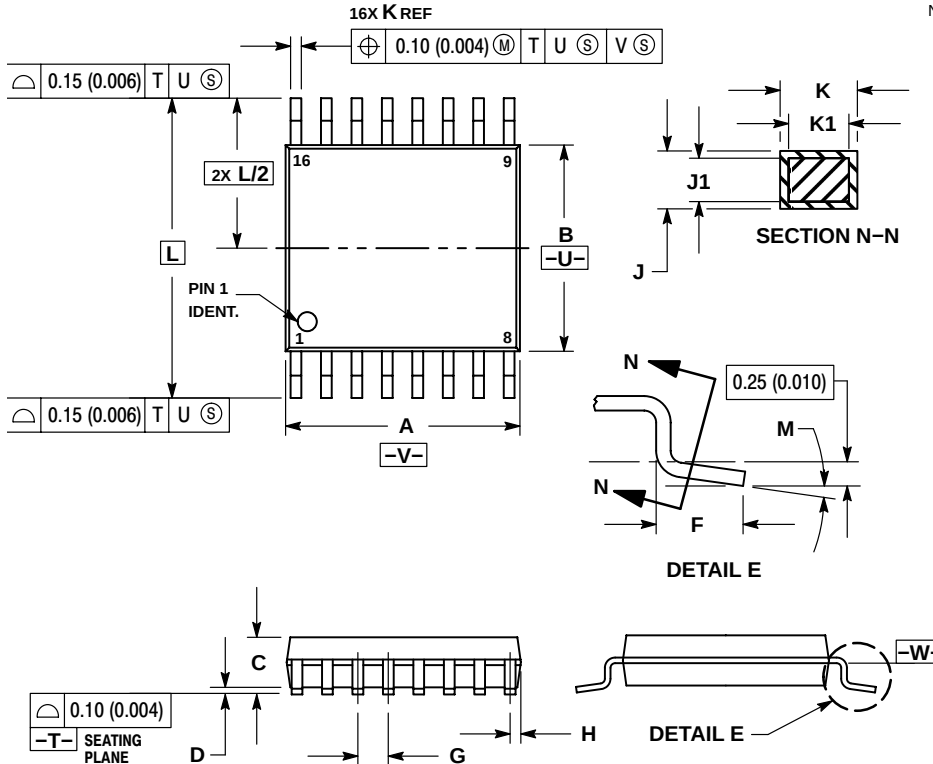


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE A



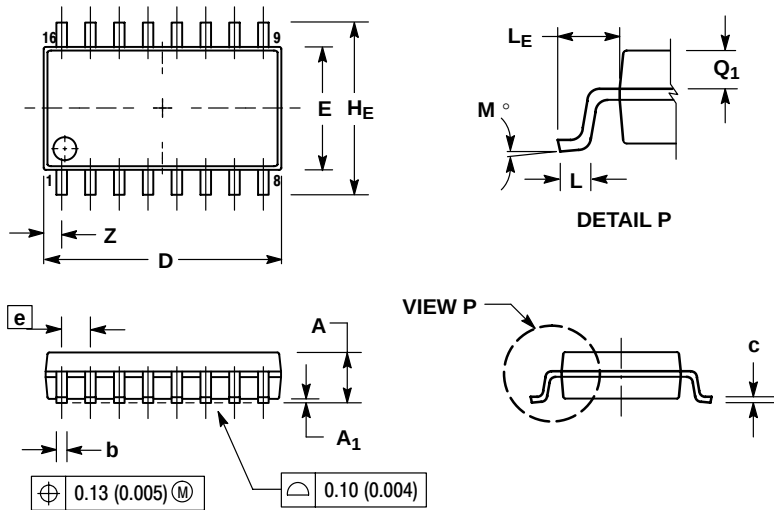
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74LVX259

SOEIAJ-16
M SUFFIX
CASE 966-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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