

TLC4501, TLC4501A, TLC4502, TLC4502A

FAMILY OF SELF-CALIBRATING (Self-Cal™) PRECISION CMOS RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS221B – MAY 1998 – REVISED APRIL 2001

- Self-Calibrates Input Offset Voltage to 40 μV Max
- Low Input Offset Voltage Drift . . . 1 $\mu\text{V}/^\circ\text{C}$
- Input Bias Current . . . 1 pA
- Open Loop Gain . . . 120 dB
- Rail-To-Rail Output Voltage Swing
- Stable Driving 1000 pF Capacitive Loads
- Gain Bandwidth Product . . . 4.7 MHz
- Slew Rate . . . 2.5 V/ μs
- High Output Drive Capability . . . ± 50 mA
- Calibration Time . . . 300 ms
- Characterized From -55°C to 125°C
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

description

The TLC4501 and TLC4502 are the highest precision CMOS single supply rail-to-rail operational amplifiers available today. The input offset voltage is 10 μV typical and 40 μV maximum. This exceptional precision, combined with a 4.7-MHz bandwidth, 2.5-V/ μs slew rate, and 50-mA output drive, is ideal for multiple applications including: data acquisition systems, measurement equipment, industrial control applications, and portable digital scales.

These amplifiers feature *self-calibrating* circuitry which digitally trims the input offset voltage to less than 40 μV within the first 300 ms of operation. The offset is then digitally stored in an integrated successive approximation register (SAR). Immediately after the data is stored, the calibration circuitry effectively drops out of the signal path, shuts down, and the device functions as a standard operational amplifier.

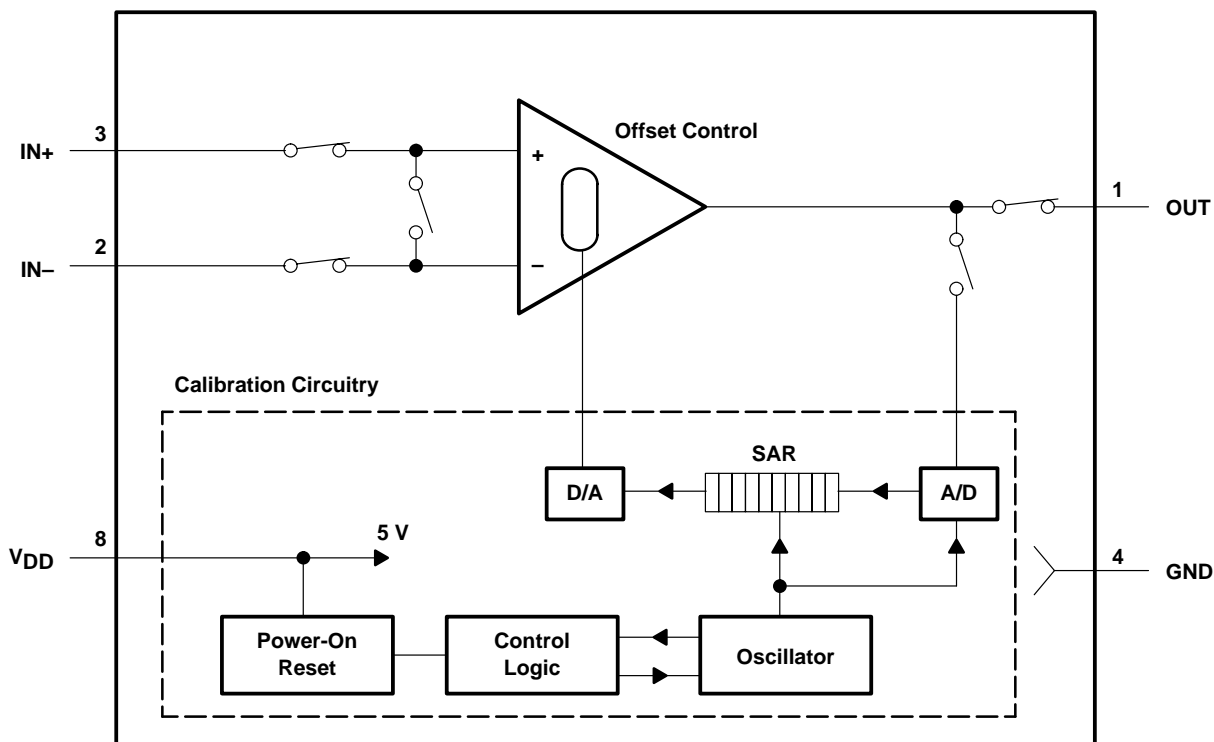


Figure 1. Channel One of the TLC4502



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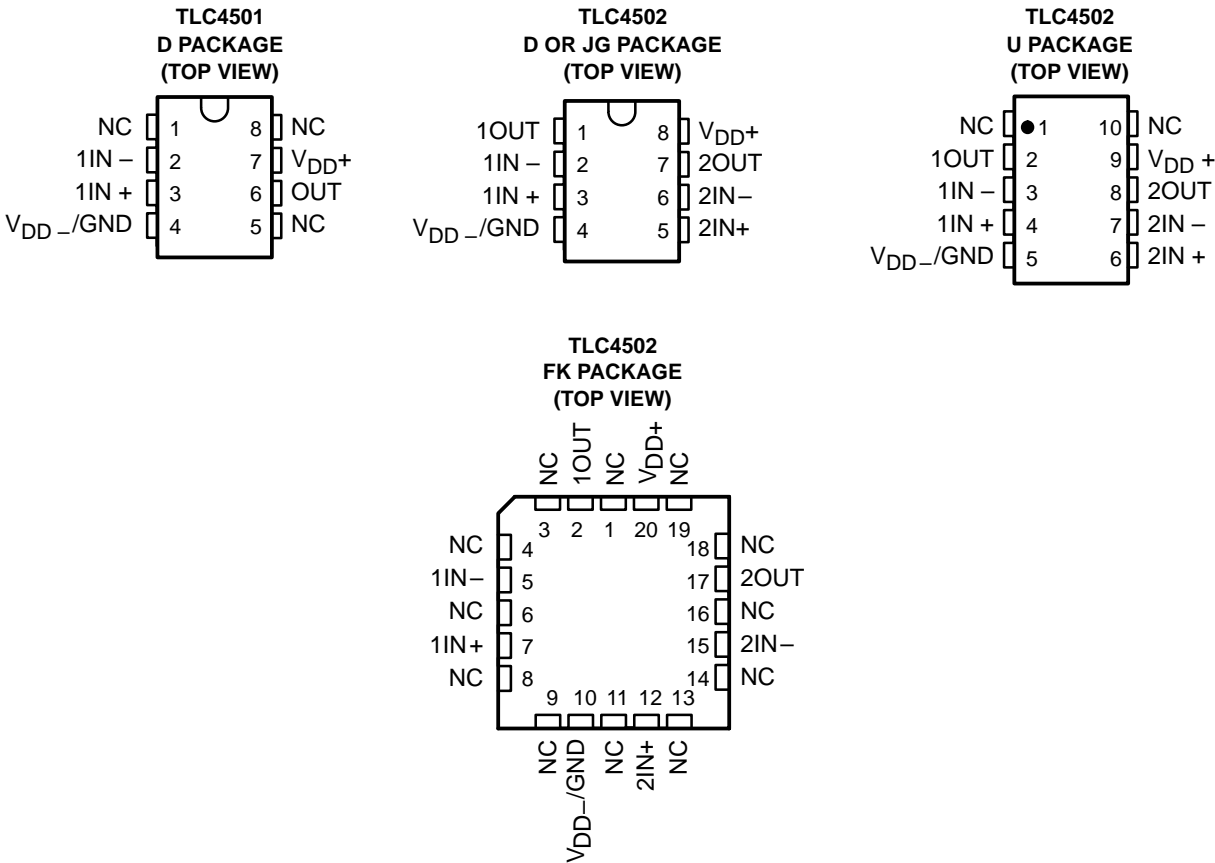
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description (continued)

Using this technology eliminates the need for noisy and expensive chopper techniques, laser trimming, and power hungry, split supply bipolar operational amplifiers.



NC – No internal connection

AVAILABLE OPTIONS					
T _A	V _{IO} max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	CERAMIC FLAT PACK (U)
0°C to 70°C	40 µV	TLC4501ACD	—	—	—
	50 µV	TLC4502ACD	—	—	—
	80 µV	TLC4501CD	—	—	—
	100 µV	TLC4502CD	—	—	—
–40°C to 125°C	40 µV	TLC4501AID	—	—	—
	50 µV	TLC4502AID	—	—	—
	80 µV	TLC4501ID	—	—	—
	100 µV	TLC4502ID	—	—	—
–40°C to 125°C	50 µV	TLC4502AQD	—	—	—
	100 µV	TLC4502QD	—	—	—
–55°C to 125°C	50 µV	TLC4502AMD	TLC4502AMFKB	TLC4502AMJGB	TLC4502AMUB
	100 µV	TLC4502MD	TLC4502MFKB	TLC4502MJGB	TLC4502MUB

† The D package is also available taped and reeled.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	7 V
Differential input voltage, V_{ID} (see Note 2)	± 7 V
Input voltage range, V_I (any input, see Note 1)	–0.3 V to 7 V
Input current, I_I (each input)	± 5 mA
Output current, I_O (each output)	± 100 mA
Total current into V_{DD+}	± 100 mA
Total current out of V_{DD-}/GND	± 100 mA
Electrostatic discharge (ESD)	> 2 kV
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : TLC4502C	0°C to 70°C
TLC4502I	–40°C to 125°C
TLC4502Q	–40°C to 125°C
TLC4502M	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND .
2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows when an input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	TLC4502C		TLC4502I		TLC4502Q		TLC4502M		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	4	6	4	6	4	6	4	6	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Operating free-air temperature, T_A	0	70	–40	125	–40	125	–55	125	°C



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$, $GND = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A †	TLC450xC			UNIT
					MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD} = ±2.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω	TLC4501	Full range	-80	10	80	μV
			TLC4501A		-40	10	40	
			TLC4502		-100	10	100	
			TLC4502A		-50	10	50	
α _{VIO}	Temperature coefficient of input offset voltage	V _{DD} = ±2.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω		Full range	1		μV/°C	
I _{IO}	Input offset current			25°C	1 60		pA	
				Full range	500			
I _{IB}	Input bias current			25°C	1 60		pA	
		Full range	500					
V _{OH}	High-level output voltage	I _{OH} = - 500 μA		25°C	4.99		V	
		I _{OH} = - 5 mA		25°C	4.9			
				Full range	4.7			
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 500 μA		25°C	0.01		V	
		V _{IC} = 2.5 V, I _{OL} = 5 mA		25°C	0.1			
				Full range	0.3			
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, V _O = 1 V to 4 V, R _L = 1 kΩ, See Note 4		25°C	200	1000	V/mV	
				Full range	200			
R _{I(D)}	Differential input resistance			25°C	10		kΩ	
R _L	Input resistance	See Note 4		25°C	10 ¹²		Ω	
C _L	Common-mode input capacitance	f = 10 kHz,	P package	25°C	8		pF	
z _O	Closed-loop output impedance	A _V = 10,	f = 100 kHz	25°C	1		Ω	
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 1 kΩ		25°C	90	100	dB	
				Full range	85			
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} ±/ΔV _{IO})	V _{DD} = 4 V to 6 V, V _{IC} = 0, No load		25°C	90	100	dB	
				Full range	90			
I _{DD}	Supply current	V _O = 2.5 V, No load	TLC4501/A	25°C	1	1.5	mA	
					Full range	2		
			TLC4502/A	25°C	2.5	3.5		
					Full range	4		
V _{IT(CAL)}	Calibration input threshold voltage			Full range	4		V	

† Full range is 0°C to 70°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.



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operating characteristics, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A †	TLC450xC, TLC450xAC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 0.5 V to 2.5 V, C _L = 100 pF		25°C	1.5	2.5		V/μs
				Full range	1			V/μs
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	70			nV/√Hz
		f = 1 kHz		25°C	12			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C	1			μV
		f = 0.1 to 10 Hz		25°C	1.5			
I _n	Equivalent input noise current			25°C	0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 1 kΩ, C _L = 100 pF	A _V = 1	25°C	0.02%			
			A _V = 10	25°C	0.08%			
			A _V = 100	25°C	0.55%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 1 kΩ,	25°C	4.7			MHz
B _{OM}	Maximum output swing bandwidth	V _{O(PP)} = 2 V, R _L = 1 kΩ,	A _V = 1, C _L = 100 pF	25°C	1			MHz
t _s	Settling time	A _V = −1, Step = 0.5 V to 2.5 V, R _L = 1 kΩ, C _L = 100 pF	to 0.1%	25°C	1.6			μs
			to 0.01%	25°C	2.2			
φ _m	Phase margin at unity gain	R _L = 1 kΩ,	C _L = 100 pF	25°C	74			
Calibration time				25°C	300			ms

† Full range is 0°C to 70°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$, $GND = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A †	TLC450xI			UNIT
					MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{DD} = ±2.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω	TLC4501	Full range	-80	10	80	μV
			TLC4501A		-40	10	40	
			TLC4502		-100	10	100	
			TLC4502A		-50	10	50	
α _{VIO}	Temperature coefficient of input offset voltage	V _{DD} = ±2.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω		Full range	1		μV/°C	
I _{IO}	Input offset current			25°C	1 60		pA	
				-40°C to 85°C	500			
				Full range	5		nA	
I _{IB}	Input bias current	V _{DD} = ±2.5 V, V _O = 0, V _{IC} = 0, R _S = 50 Ω	25°C	1 60		pA		
			-40°C to 85°C	500				
			Full range	10		nA		
V _{OH}	High-level output voltage	I _{OH} = - 500 μA	25°C	4.99		V		
		I _{OH} = - 5 mA	25°C	4.9				
			Full range	4.7				
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 500 μA	25°C	0.01		V		
		V _{IC} = 2.5 V, I _{OL} = 5 mA	25°C	0.1				
			Full range	0.3				
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, R _L = 1 kΩ, V _O = 1 V to 4 V, See Note 4	25°C	200	1000	V/mV		
			Full range	200				
R _{I(D)}	Differential input resistance		25°C	10		kΩ		
R _L	Input resistance	See Note 4	25°C	10 ¹²		Ω		
C _L	Common-mode input capacitance	f = 10 kHz, P package	25°C	8		pF		
z _O	Closed-loop output impedance	A _V = 10, f = 100 kHz	25°C	1		Ω		
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 1 kΩ	25°C	90	100	dB		
			Full range	85				
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} ±ΔV _{IO})	V _{DD} = 4 V to 6 V, V _{IC} = 0, No load	25°C	90	100	dB		
			Full range	90				
I _{DD}	Supply current	V _O = 2.5 V, No load	TLC4501/A	25°C	1	1.5	mA	
			TLC4502/A	Full range	2			
				25°C	2.5	3.5		
				Full range	4			
V _{IT(CAL)}	Calibration input threshold voltage		Full range	4		V		

† Full range is -40°C to 125°C.

NOTE 4: R_L and C_L values are referenced to 2.5 V.



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operating characteristics, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A †	TLC450xI, TLC450xAI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = 0.5 V to 2.5 V, C _L = 100 pF		25°C	1.5	2.5		V/μs
				Full range	1			V/μs
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	70			nV/√Hz
		f = 1 kHz		25°C	12			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz		25°C	1			μV
		f = 0.1 to 10 Hz		25°C	1.5			
I _n	Equivalent input noise current			25°C	0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = 0.5 V to 2.5 V, f = 10 kHz, R _L = 1 kΩ, C _L = 100 pF	A _V = 1	25°C	0.02%			
			A _V = 10	25°C	0.08%			
			A _V = 100	25°C	0.55%			
Gain-bandwidth product		f = 10 kHz, C _L = 100 pF	R _L = 1 kΩ,	25°C	4.7			MHz
B _{OM}	Maximum output swing bandwidth	V _{O(PP)} = 2 V, R _L = 1 kΩ,	A _V = 1, C _L = 100 pF	25°C	1			MHz
t _s	Settling time	A _V = −1, Step = 0.5 V to 2.5 V, R _L = 1 kΩ, C _L = 100 pF	to 0.1%	25°C	1.6			μs
			to 0.01%	25°C	2.2			
φ _m	Phase margin at unity gain	R _L = 1 kΩ,	C _L = 100 pF	25°C	74			
Calibration time				25°C	300			ms

† Full range is -40°C to 125°C .

NOTE 4: R_L and C_L values are referenced to 2.5 V.

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PARAMETER		TEST CONDITIONS		T _A †	TLC4502Q, TLC4502M			UNIT		
					MIN	TYP	MAX			
V _{IO}	Input offset voltage	V _{DD} = ±2.5 V, V _{IC} = 0,	V _O = 0, R _S = 50 Ω	TLC4502 TLC4502A	Full range	–100 –50	10 10	100 50	μV	
α _{VIO}	Temperature coefficient of input offset voltage	V _{DD} = ±2.5 V, V _{IC} = 0, R _S = 50 Ω			Full range	1			μV/°C	
I _{IO}	Input offset current				25°C	1			60	nA
					125°C				5	
I _{IB}	Input bias current				25°C	1			60	nA
		125°C				10				
V _{OH}	High-level output voltage	I _{OH} = – 500 μA		25°C	4.99			V		
		I _{OH} = – 5 mA		25°C	4.9					
				Full range	4.7					
V _{OL}	Low-level output voltage	V _{IC} = 2.5 V, I _{OL} = 500 μA		25°C	0.01			V		
		V _{IC} = 2.5 V, I _{OL} = 5 mA		25°C	0.1					
				Full range	0.3					
A _{VD}	Large-signal differential voltage amplification	V _{IC} = 2.5 V, R _L = 1 kΩ, V _O = 1 V to 4 V, See Note 4		25°C	200	1000		V/mV		
				Full range	200					
R _{I(D)}	Differential input resistance			25°C	10			kΩ		
R _L	Input resistance	See Note 4		25°C	10 ¹²			Ω		
C _L	Common-mode input capacitance	f = 10 kHz, P package		25°C	8			pF		
z _O	Closed-loop output impedance	A _V = 10, f = 100 kHz		25°C	1			Ω		
CMRR	Common-mode rejection ratio	V _{IC} = 0 to 2.7 V, V _O = 2.5 V, R _S = 1 kΩ		25°C	90	100		dB		
				Full range	85					
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} ±/ΔV _{IO})	V _{DD} = 4 V to 6 V, V _{IC} = V _{DD} /2, No load		25°C	90	100		dB		
				Full range	90					
I _{DD}	Supply current	V _O = 2.5 V, No load		25°C	2.5	3.5		mA		
				Full range	4					
V _{IT(CAL)}	Calibration input threshold voltage			Full range	4			V		

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: R_L and C_L values are referenced to 2.5 V.

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operating characteristics, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLC4502Q, TLC4502M, TLC4502AQ, TLC4502AM			UNIT
			MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.5\text{ V to }2.5\text{ V},$ See Note 4 $C_L = 100\text{ pF}$	25°C	1.5	2.5		V/ μs
		Full range	1			V/ μs
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		70		nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		12		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$	25°C		1		μV
	$f = 0.1\text{ to }10\text{ Hz}$	25°C		1.5		
I_n Equivalent input noise current		25°C		0.6		fA/ $\sqrt{\text{Hz}}$
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V},$ $f = 10\text{ kHz},$ $R_L = 1\text{ k}\Omega,$ $C_L = 100\text{ pF}$	$A_V = 1$ 25°C		0.02%		
		$A_V = 10$ 25°C		0.08%		
		$A_V = 100$ 25°C		0.55%		
Gain-bandwidth product	$f = 10\text{ kHz},$ $R_L = 1\text{ k}\Omega,$ $C_L = 100\text{ pF}$	25°C		4.7		MHz
BOM Maximum output swing bandwidth	$V_{O(PP)} = 2\text{ V},$ $A_V = 1,$ $R_L = 1\text{ k}\Omega,$ $C_L = 100\text{ pF}$	25°C		1		MHz
t_s Settling time	$A_V = -1,$ Step = $0.5\text{ V to }2.5\text{ V},$ $R_L = 1\text{ k}\Omega,$ $C_L = 100\text{ pF}$	to 0.1% 25°C		1.6		μs
		to 0.01% 25°C		2.2		
ϕ_m Phase margin at unity gain	$R_L = 1\text{ k}\Omega,$ $C_L = 100\text{ pF}$	25°C		74		
Calibration time		25°C		300		ms

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: R_L and C_L values are referenced to 2.5 V.



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TYPICAL CHARACTERISTICS

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V_{OL}	Low-level output voltage	vs Low-level output current	9
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	10
I_{OS}	Short-circuit output current	vs Free-air temperature	11
V_O	Output voltage	vs Differential input voltage	12
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature	13
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z_o	Output impedance	vs Frequency	15
CMRR	Common-mode rejection ratio	vs Frequency	16
		vs Free-air temperature	17
SR	Slew rate	vs Load capacitance	18
		vs Free-air temperature	19
	Inverting large-signal pulse response		20
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	Inverting small-signal pulse response		22
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V_n	Equivalent input noise voltage	vs Frequency	24
		Over a 10-second period	25
THD + N	Total harmonic distortion plus noise	vs Frequency	26
		vs Free-air temperature	27
ϕ_m	Phase margin	vs Load capacitance	28
		vs Frequency	14
	Gain margin	vs Load capacitance	29
		vs Free-air temperature	30
PSRR	Power-supply rejection ratio	vs Free-air temperature	30
	Calibration time at -40°C		31
	Calibration time at 25°C		32
	Calibration time at 85°C		33
	Calibration time at 125°C		34

TYPICAL CHARACTERISTICS

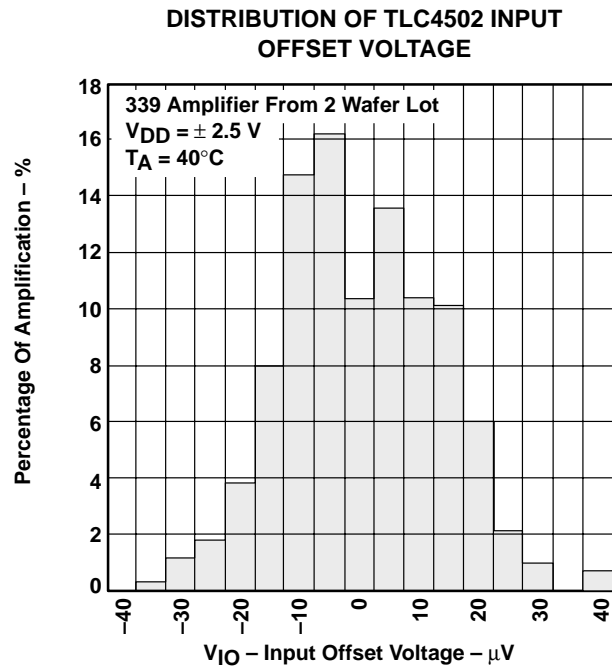


Figure 2

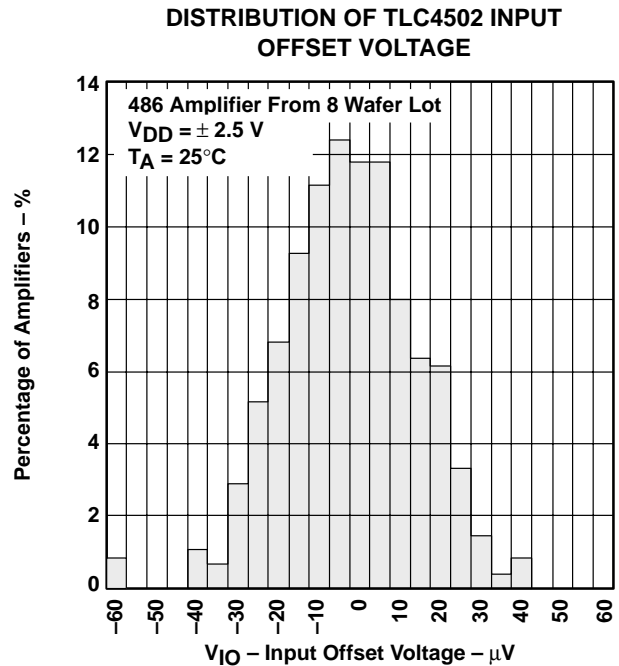


Figure 3

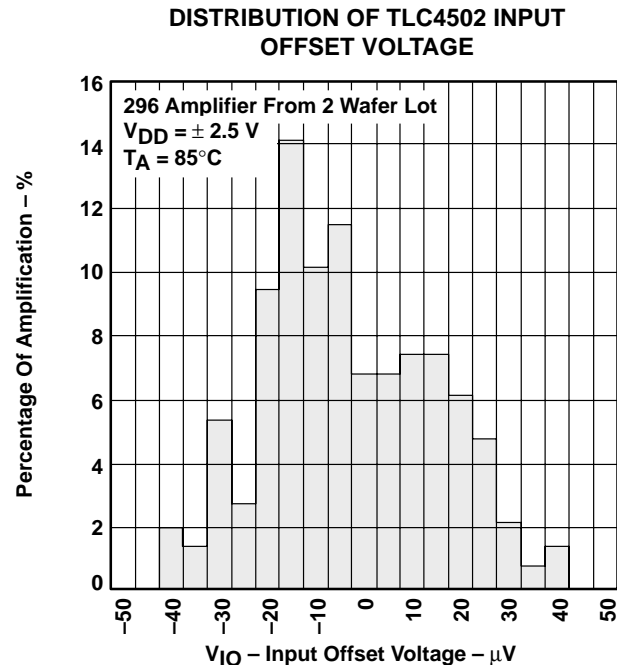


Figure 4

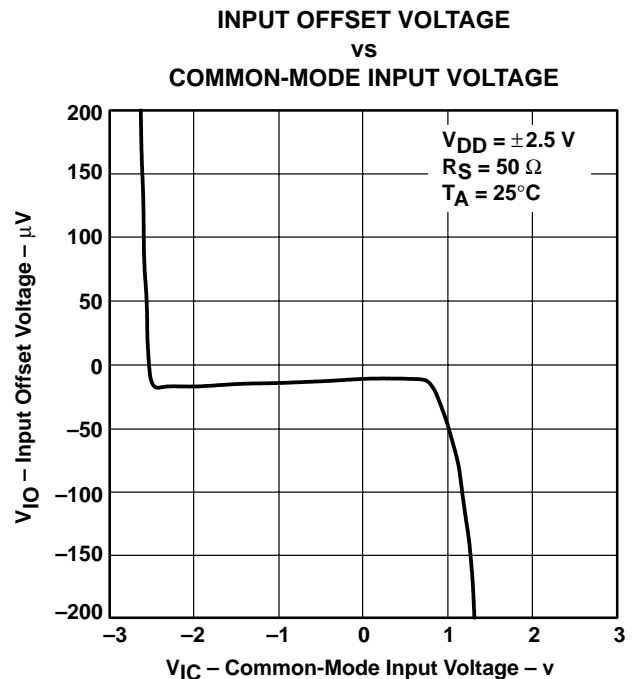


Figure 5

TLC4501, TLC4501A, TLC4502, TLC4502A
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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

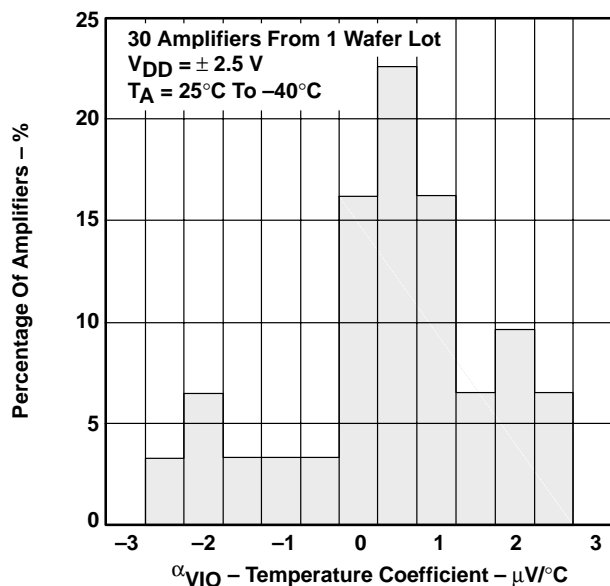


Figure 6

DISTRIBUTION OF TLC4502 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

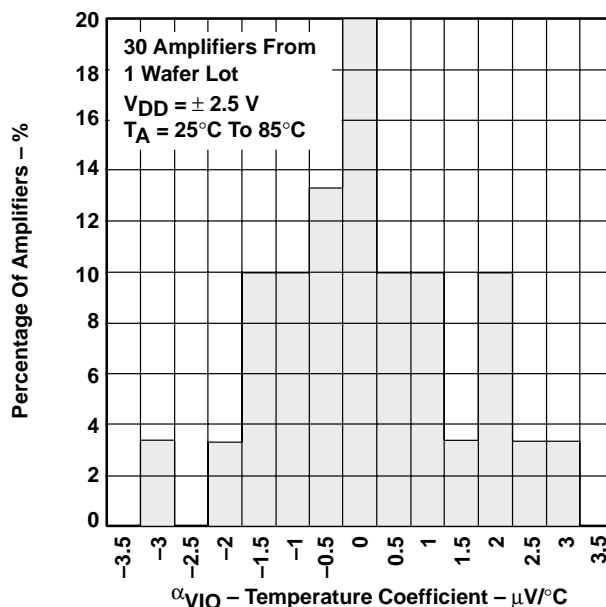


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

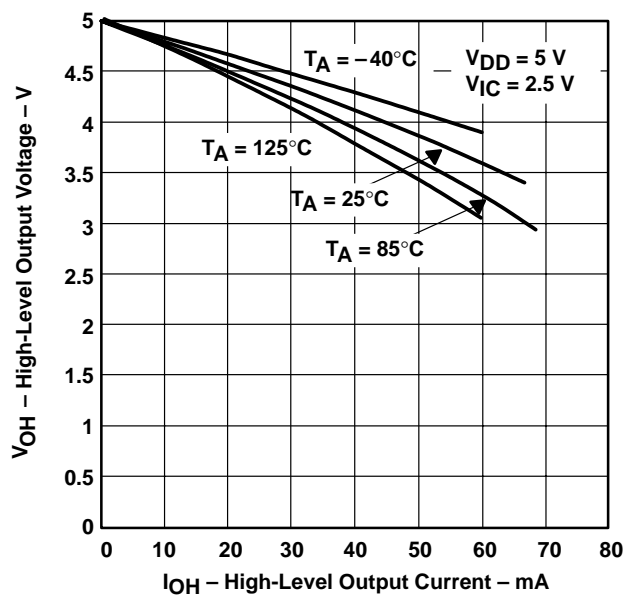


Figure 8

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

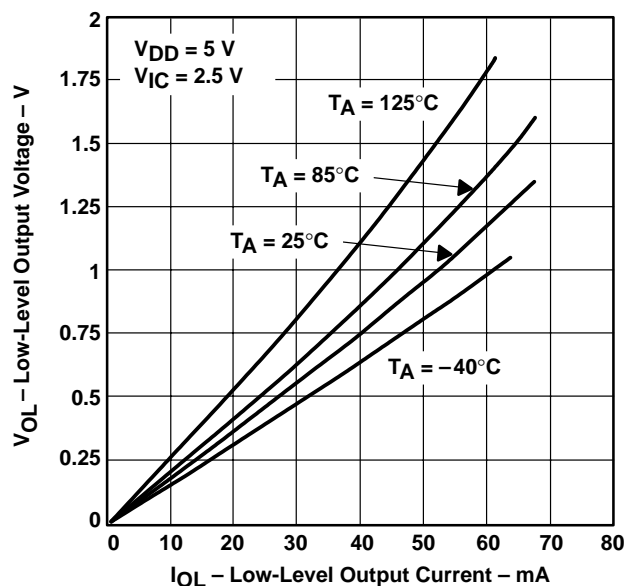
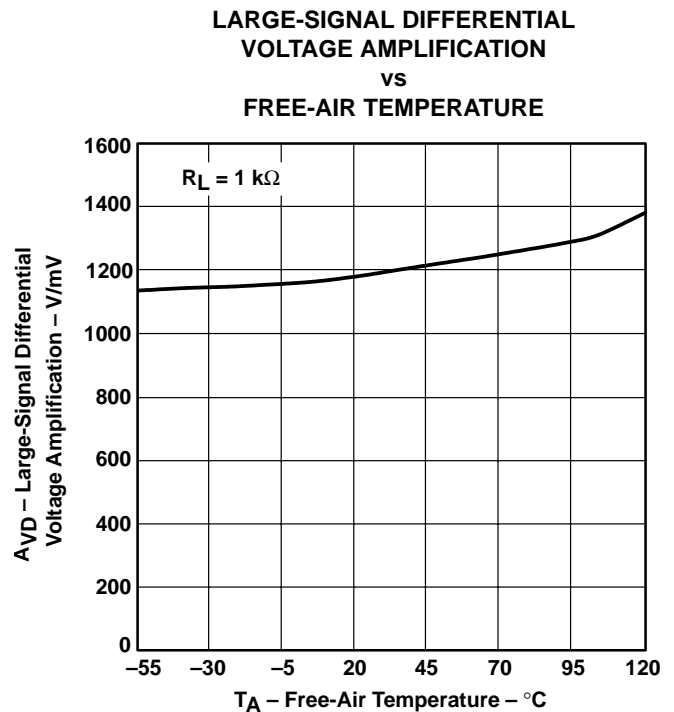
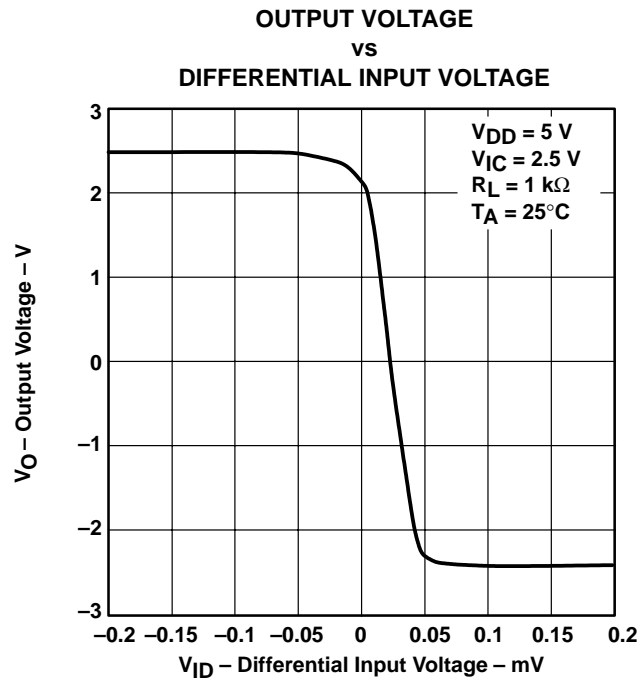
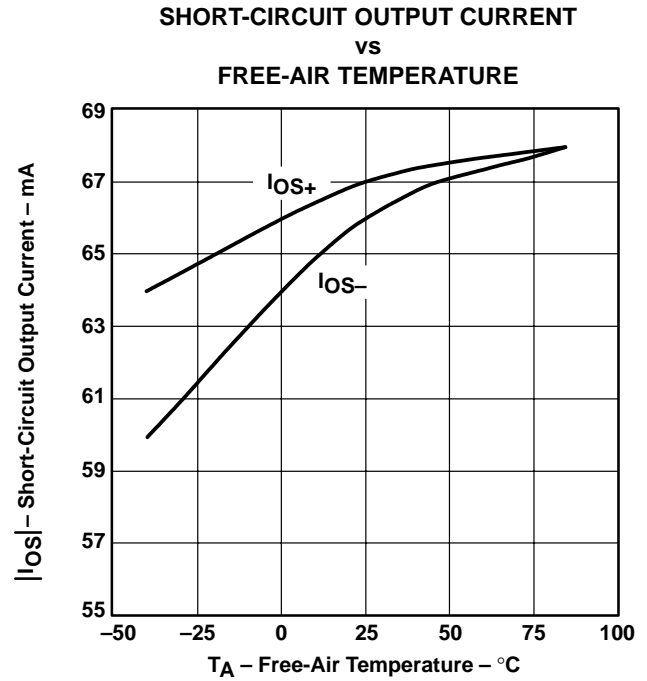
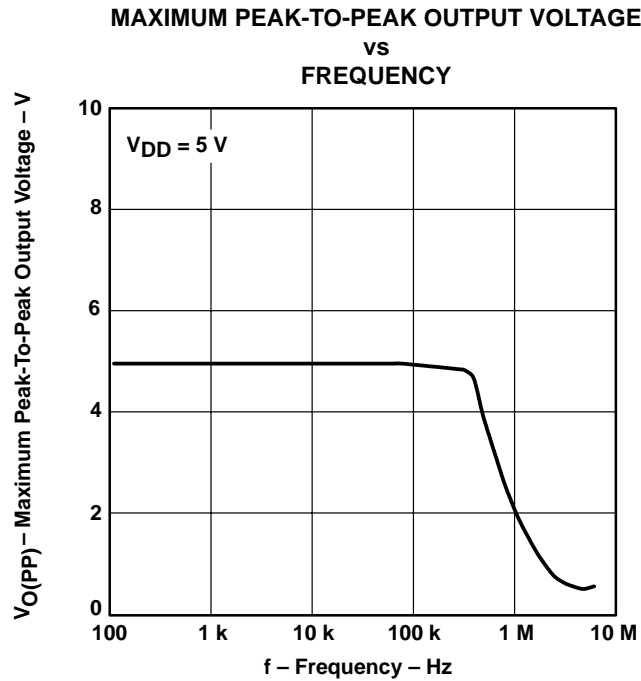


Figure 9

TYPICAL CHARACTERISTICS



TLC4501, TLC4501A, TLC4502, TLC4502A
FAMILY OF SELF-CALIBRATING (Self-Cal™)
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TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN**

**vs
FREQUENCY**

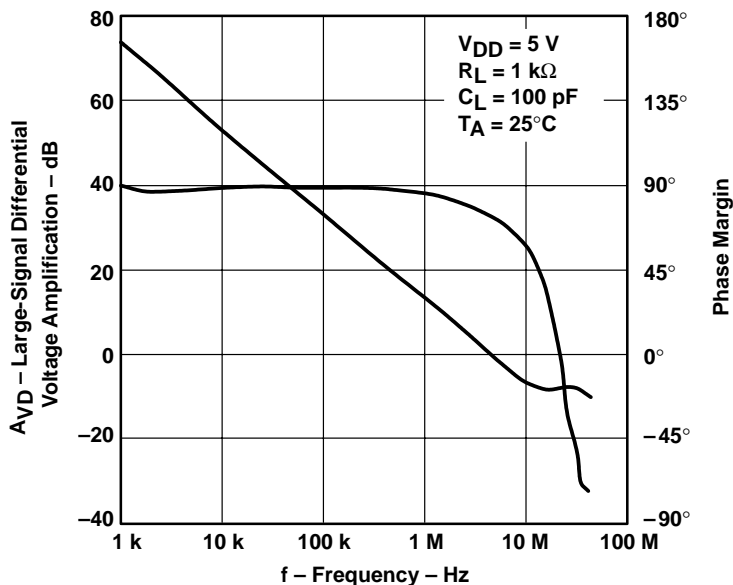


Figure 14

OUTPUT IMPEDANCE

**vs
FREQUENCY**

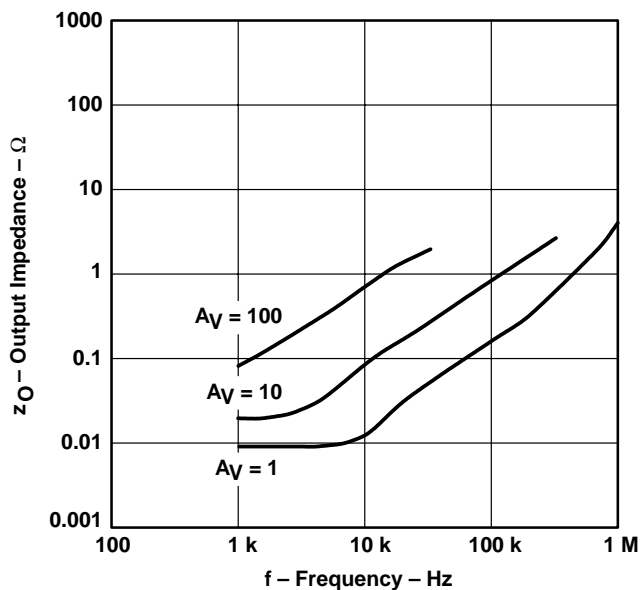


Figure 15

TYPICAL CHARACTERISTICS

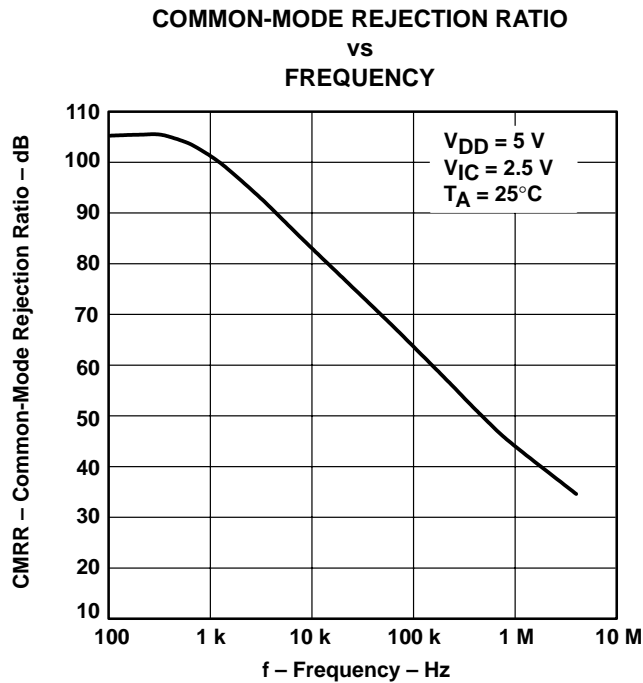


Figure 16

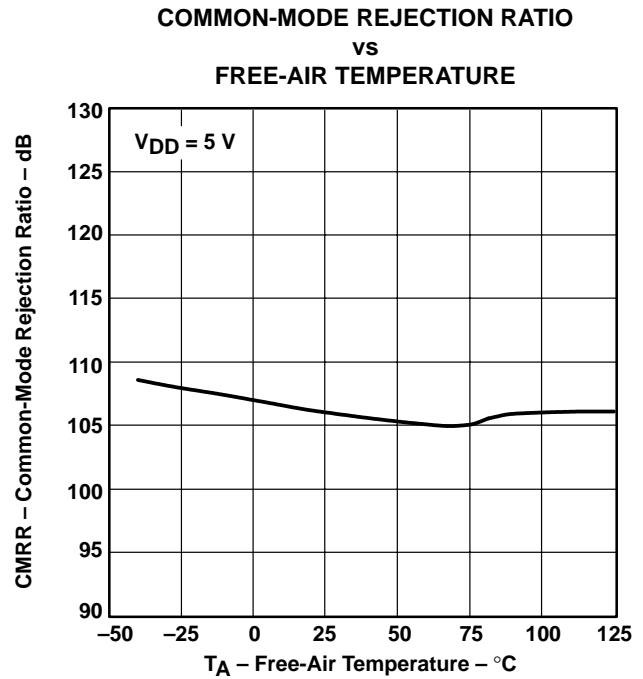


Figure 17

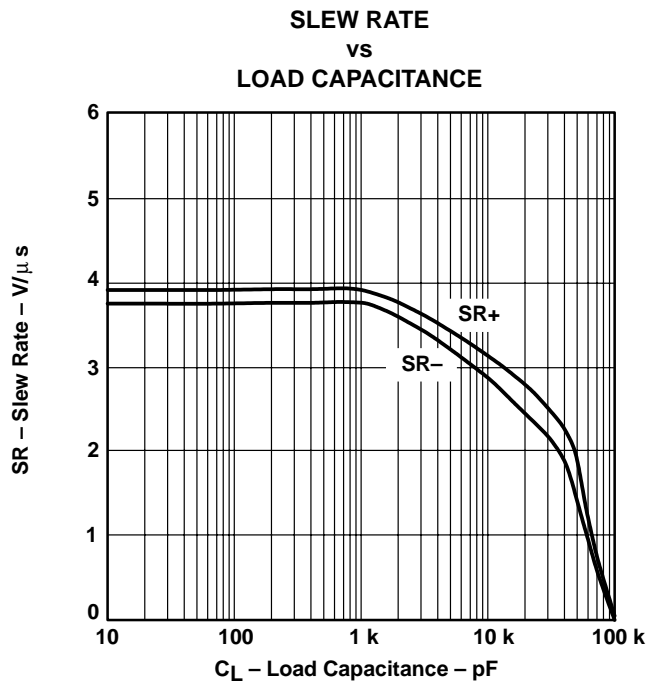


Figure 18

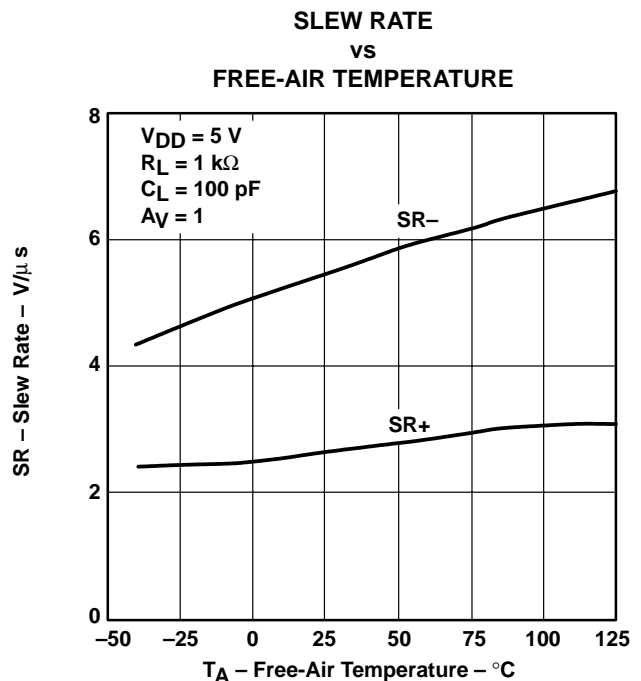


Figure 19

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

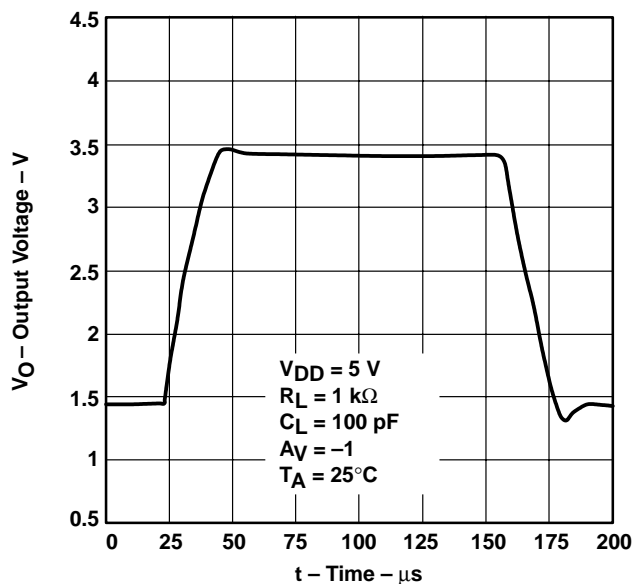


Figure 20

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

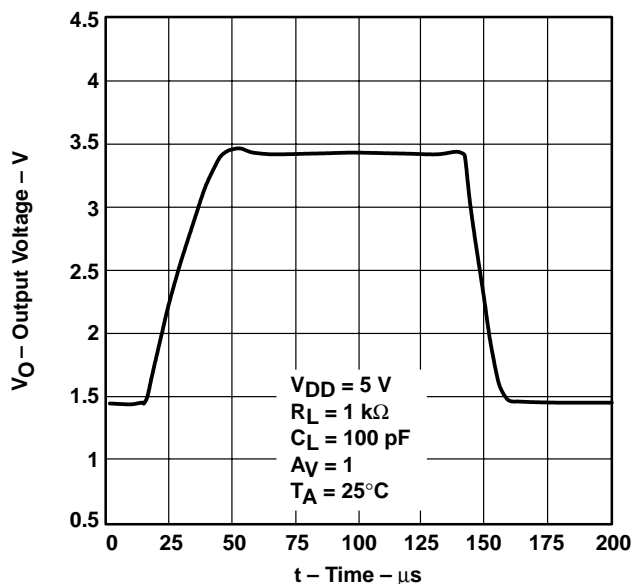


Figure 21

INVERTING SMALL-SIGNAL PULSE RESPONSE

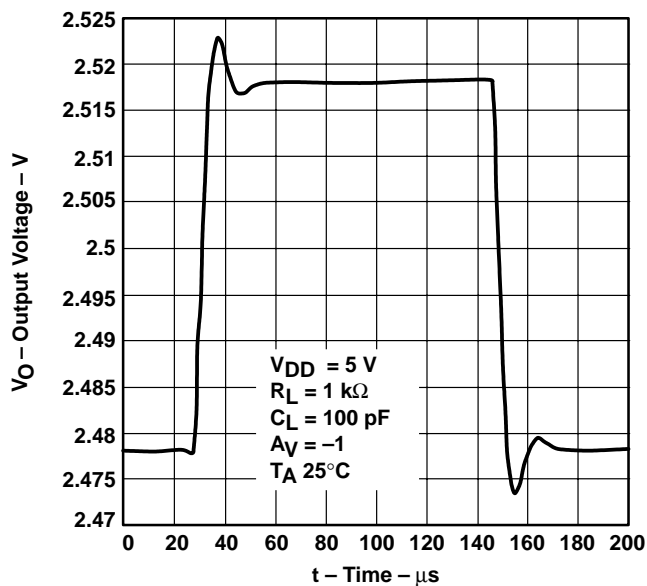


Figure 22

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

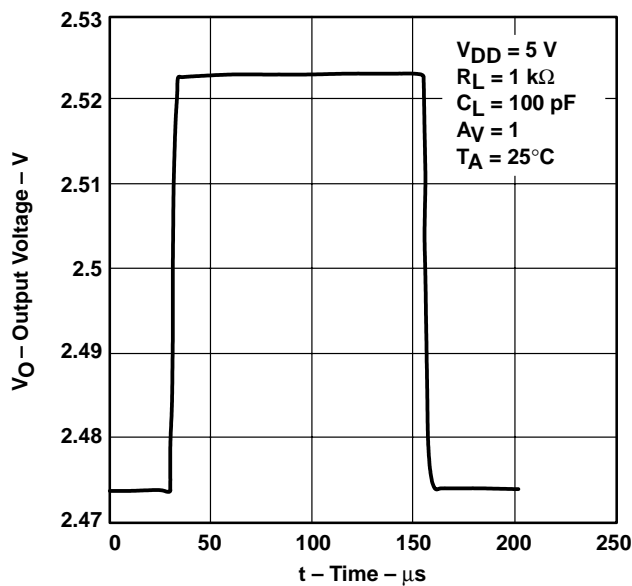


Figure 23

TYPICAL CHARACTERISTICS

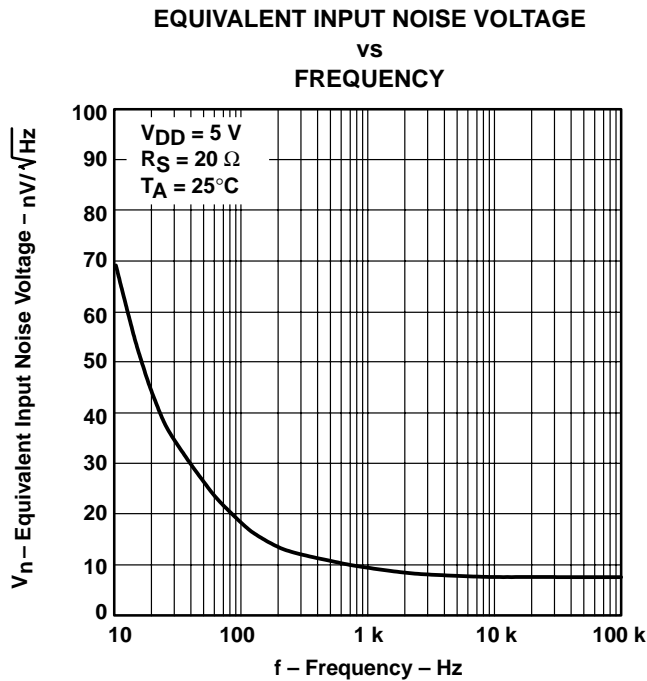


Figure 24

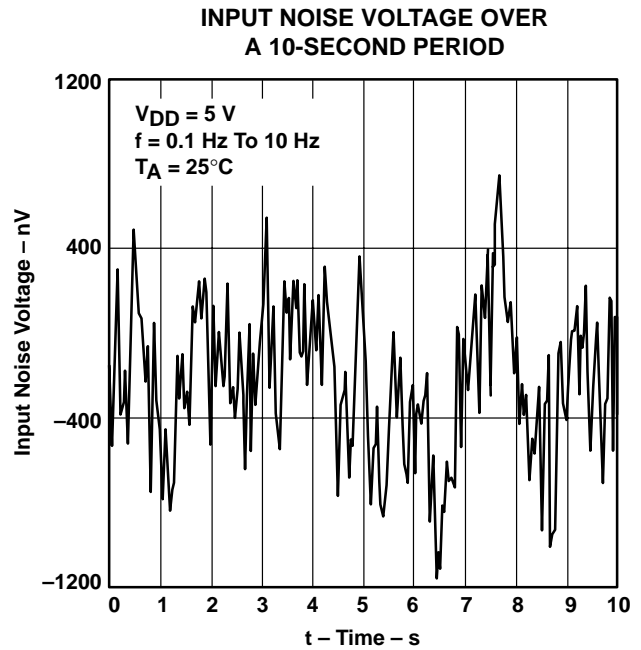


Figure 25

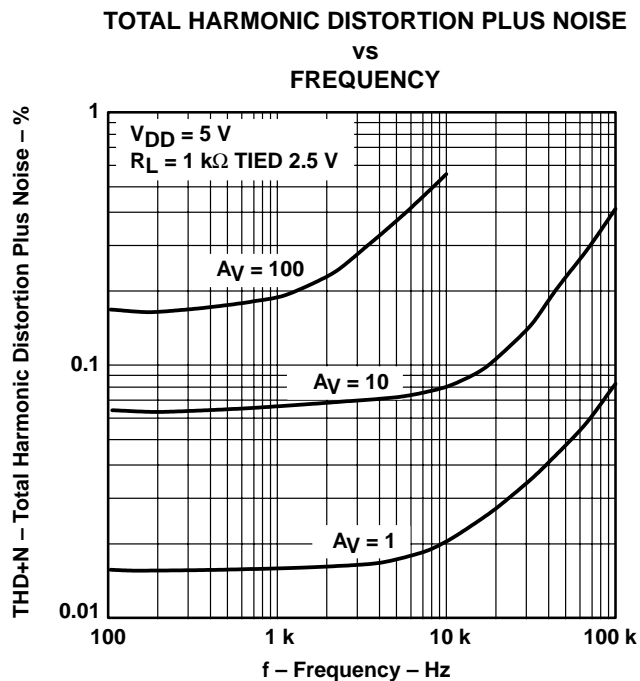


Figure 26

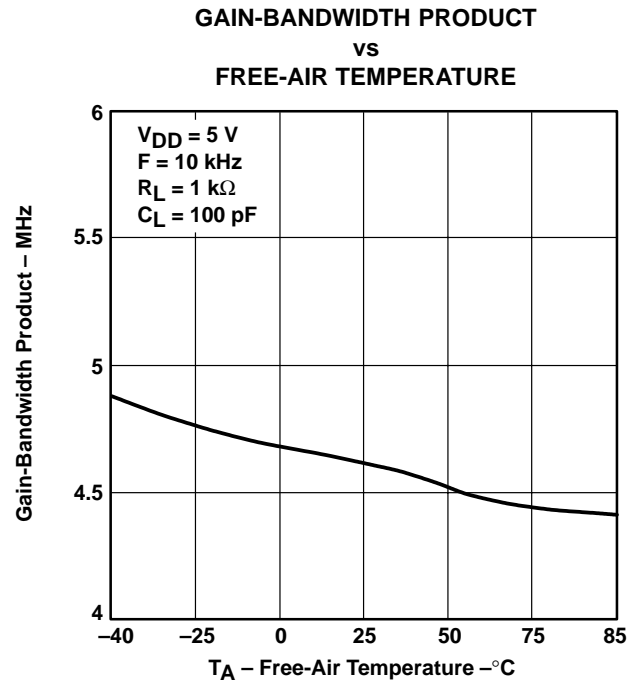


Figure 27

TLC4501, TLC4501A, TLC4502, TLC4502A
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TYPICAL CHARACTERISTICS

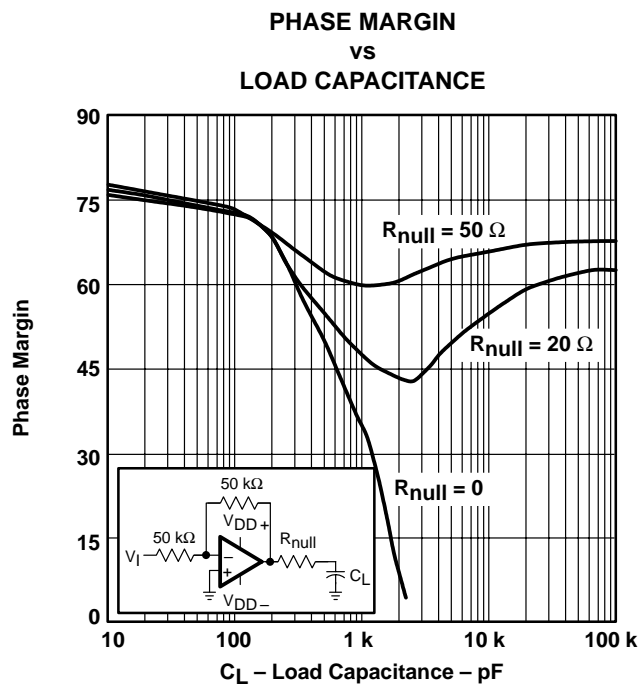


Figure 28

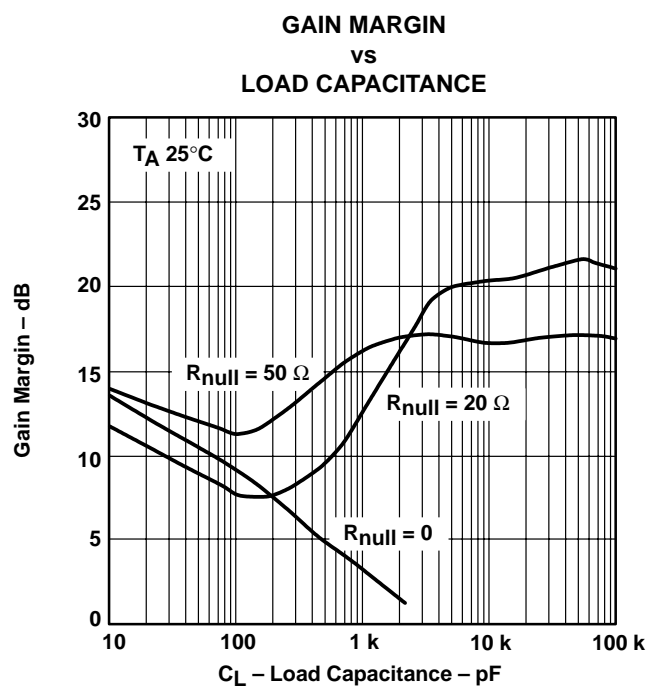


Figure 29

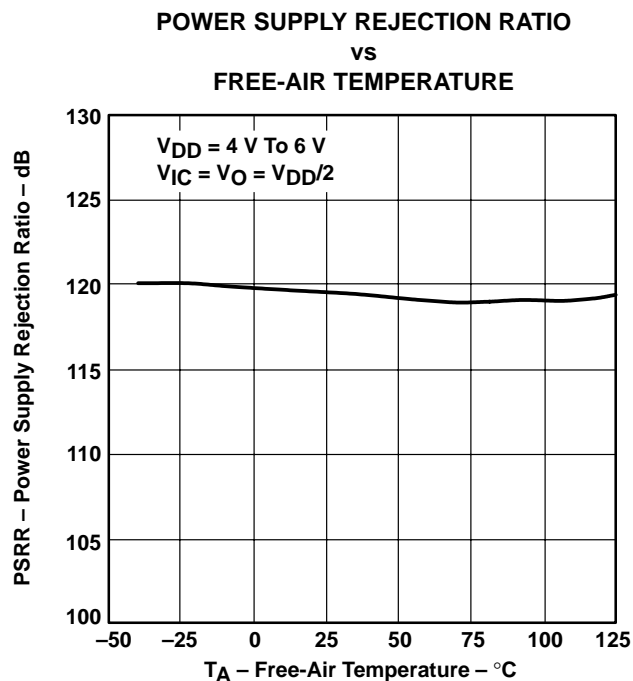


Figure 30

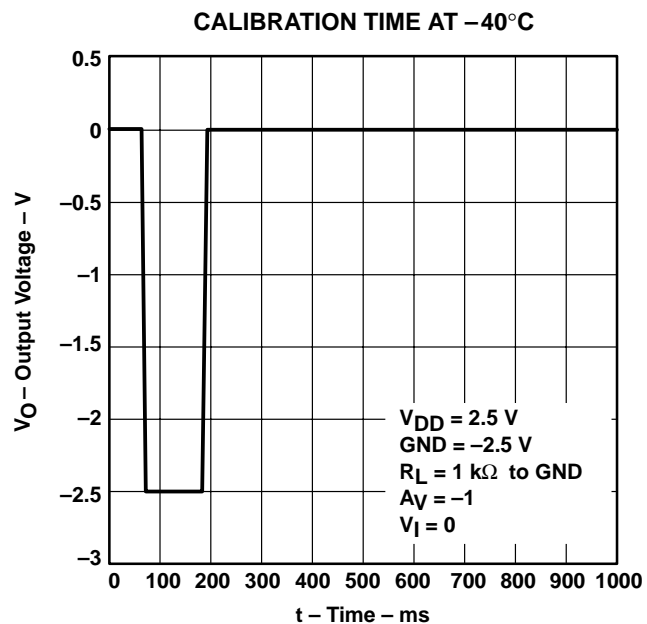


Figure 31

TYPICAL CHARACTERISTICS

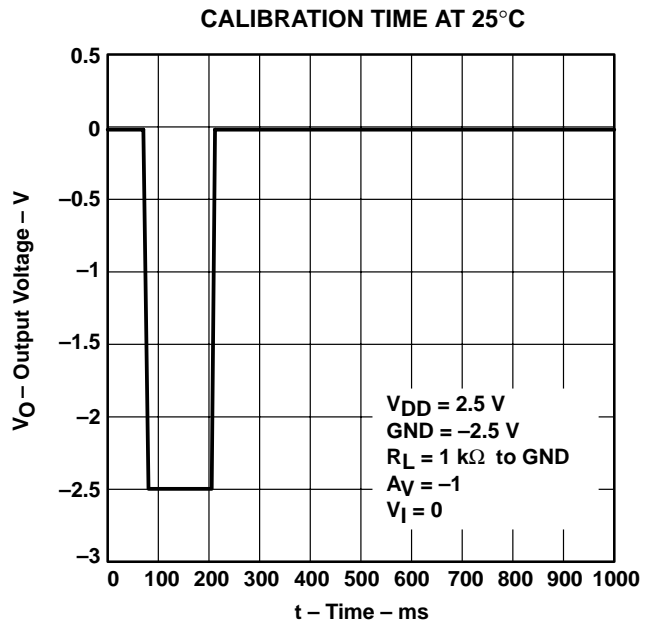


Figure 32

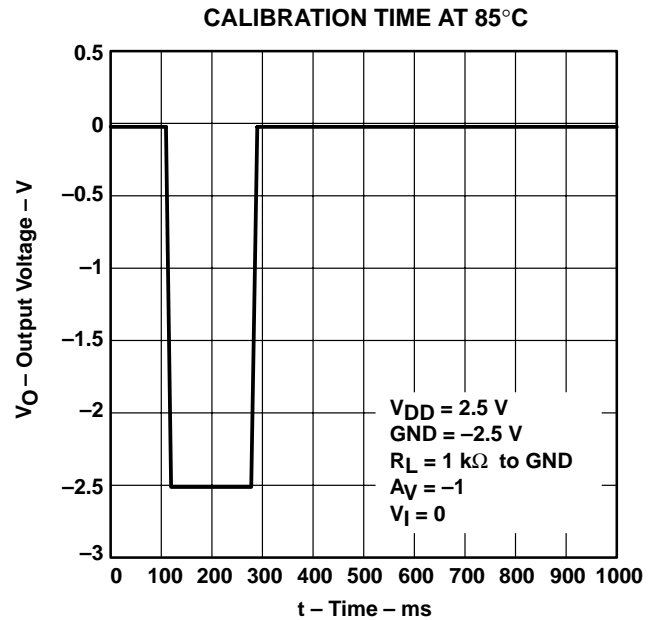


Figure 33

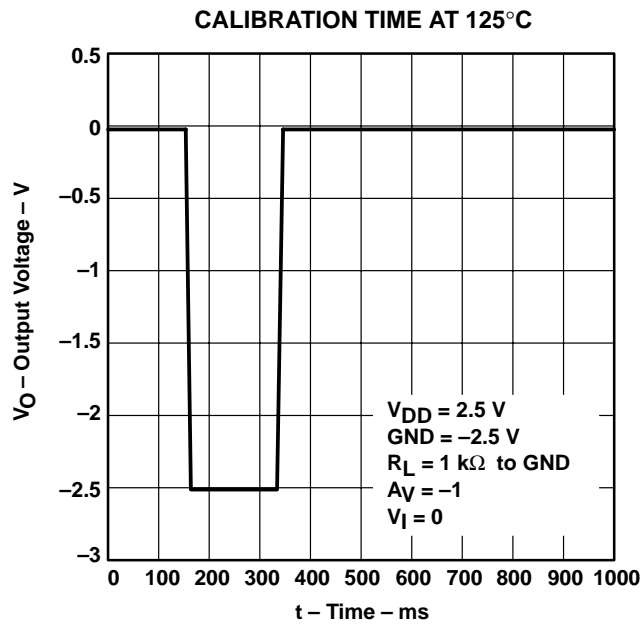


Figure 34

TLC4501, TLC4501A, TLC4502, TLC4502A
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APPLICATION INFORMATION

- The TLC4502 is designed to operate with only a single 5-V power supply, have true differential inputs, and remain in the linear mode with an input common-mode voltage of 0.
- The TLC4502 has a standard dual-amplifier pinout, allowing for easy design upgrades.
- Large differential input voltages can be easily accommodated and, as input differential-voltage protection diodes are not needed, no large input currents result from large differential input voltage. Protection should be provided to prevent the input voltages from going negative more than -0.3 V at 25°C . An input clamp diode with a resistor to the device input terminal can be used for this purpose.
- For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor can be used from the output of the amplifier to ground. This increases the class-A bias current and prevents crossover distortion. Where the load is directly coupled, for example in dc applications, there is no crossover distortion.
- Capacitive loads, which are applied directly to the output of the amplifier, reduce the loop stability margin. Values of 500 pF can be accommodated using the worst-case noninverting unity-gain connection. Resistive isolation should be considered when larger load capacitance must be driven by the amplifier.

The following typical application circuits emphasize operation on only a single power supply. When complementary power supplies are available, the TLC4502 can be used in all of the standard operational amplifier circuits. In general, introducing a pseudo-ground (a bias voltage of $V_I/2$ like that generated by the TLE2426) allows operation above and below this value in a single-supply system. Many application circuits shown take advantage of the wide common-mode input-voltage range of the TLC4502, which includes ground. In most cases, input biasing is not required and input voltages that range to ground can easily be accommodated.

description of calibration procedure

To achieve high dc gain, large bandwidth, high CMRR and PSRR, as well as good output drive capability, the TLC4502 is built around a 3-stage topology: two gain stages, one rail-to-rail, and a class-AB output stage. A nested Miller topology is used for frequency compensation.

During the calibration procedure, the operational amplifier is removed from the signal path and both inputs are tied to GND. Figure 35 shows a block diagram of the amplifier during calibration mode.



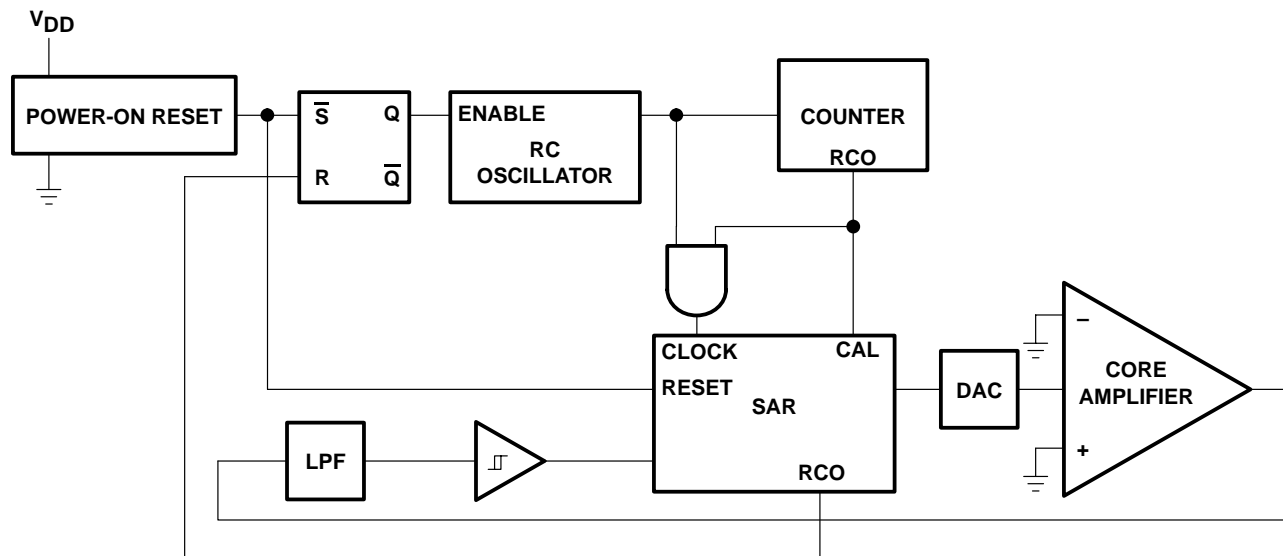


Figure 35. Block Diagram During Calibration Mode

The class AB output stage features rail-to-rail voltage swing and incorporates additional switches to put the output node into a high-impedance mode during the calibration cycle. Small-replica output transistors (matched to the main output transistors) provide the amplifier output signal for the calibration circuit. The TLC4502 also features built-in output short-circuit protection. The output current flowing through the main output transistors is continuously being sensed. If the current through either of these transistors exceeds the preset limit (60 mA – 70 mA) for more than about 1 μ s, the output transistors are shut down to approximately their quiescent operating point for approximately 5 ms. The device is then returned to normal operation. If the short circuit is still in place, it is detected in less than 1 μ s and the device is shut down for another 5 ms.

The offset cancellation uses a current-mode digital-to-analog converter (DAC), whose full-scale current allows for an adjustment of approximately ± 5 mV to the input offset voltage. The digital code producing the cancellation current is stored in the successive-approximation register (SAR).

During power up, when the offset cancellation procedure is initiated, an on-chip RC oscillator is activated to provide the timing of the successive-approximation algorithm. To prevent wide-band noise from interfering with the calibration procedure, an analog low-pass filter followed by a Schmitt trigger is used in the decision chain to implement an averaging process. Once the calibration procedure is complete, the RC oscillator is deactivated to reduce supply current and the associated noise.

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APPLICATION INFORMATION

The key operational-amplifier parameters CMRR, PSRR, and offset drift were optimized to achieve superior offset performance. The TLC4502 calibration DAC is implemented by a binary-weighted current array using a pseudo-R-2R MOSFET ladder architecture, which minimizes the silicon area required for the calibration circuitry, and thereby reduces the cost of the TLC4502.

Due to the performance (precision, PSRR, CMRR, gain, output drive, and ac performance) of the TLC4502, it is ideal for applications like:

- Data acquisition systems
- Medical equipment
- Portable digital scales
- Strain gauges
- Automotive sensors
- Digital audio circuits
- Industrial control applications

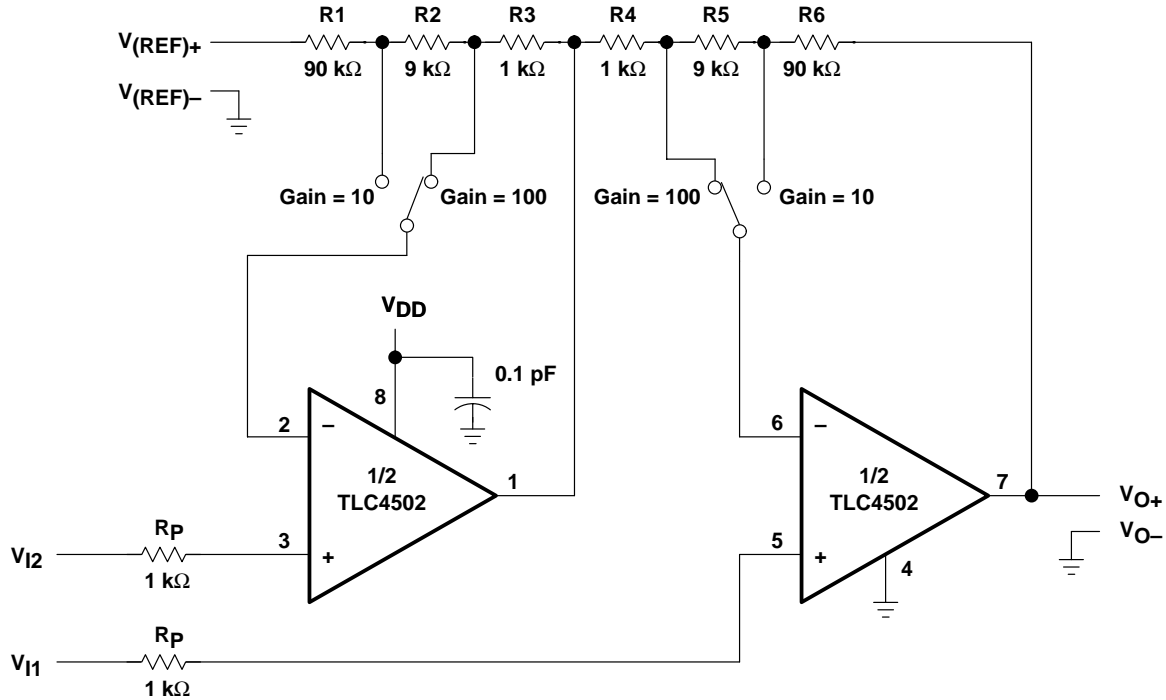
It is also ideal in circuits like:

- A precision buffer for current-to-voltage converters, a/d buffers, or bridge applications
- High-impedance buffers or preamplifiers
- Long term integration
- Sample-and-hold circuits
- Peak detectors

The TLC4502 self-calibrating operational amplifier is manufactured using Texas instruments LinEPIC process technology and is available in an 8-pin SOIC (D) Package. The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 125°C. The M-suffix devices are characterized for operation from –55°C to 125°C.



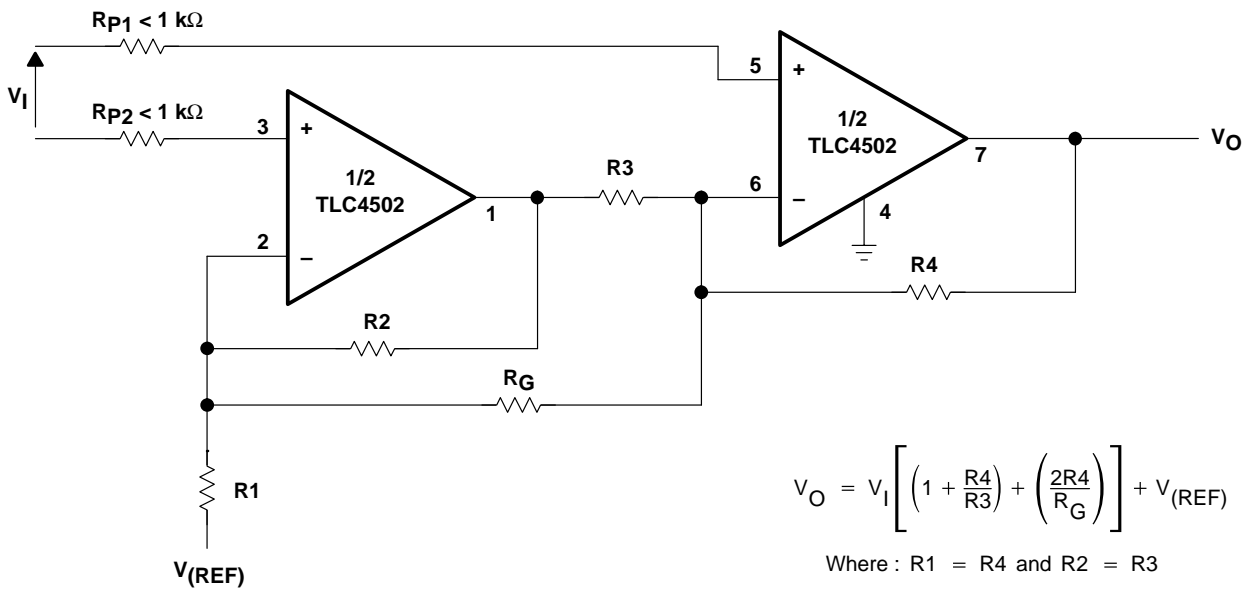
APPLICATION INFORMATION



$$(\text{Gain} = 10) \quad V_O = (V_{I1} - V_{I2}) \left(1 + \frac{R_6}{R_4 + R_5} \right) + V_{(REF)} \quad \text{Where } R_1 = R_6, R_2 = R_5, \text{ and } R_3 = R_4$$

$$(\text{Gain} = 100) \quad V_O = (V_{I1} - V_{I2}) \left(1 + \frac{R_5 + R_6}{R_4} \right) + V_{(REF)} \quad \text{Where } R_1 = R_6, R_2 = R_5, \text{ and } R_3 = R_4$$

Figure 36. Single-Supply Programmable Instrumentation Amplifier Circuit



$$V_O = V_I \left[\left(1 + \frac{R_4}{R_3} \right) + \left(\frac{2R_4}{R_G} \right) \right] + V_{(REF)}$$

Where : $R_1 = R_4$ and $R_2 = R_3$

Figure 37. Two Operational-Amplifier Instrumentation Amplifier Circuit

APPLICATION INFORMATION

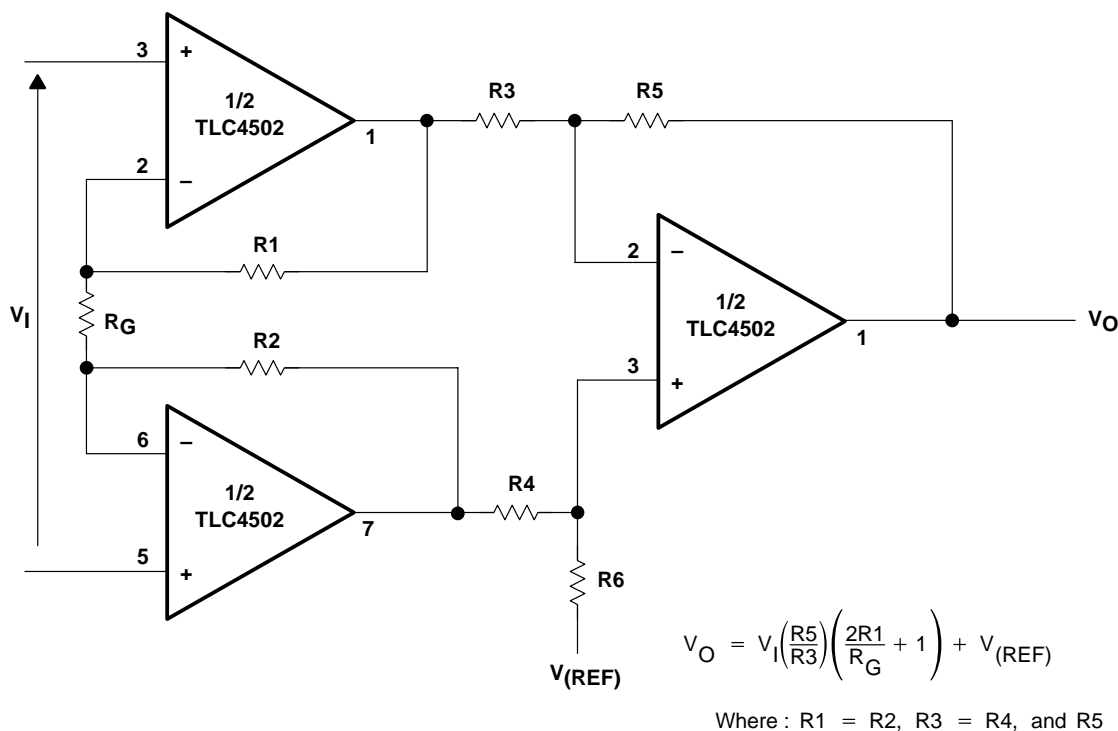


Figure 38. Three Operational-Amplifier Instrumentation Amplifier Circuit

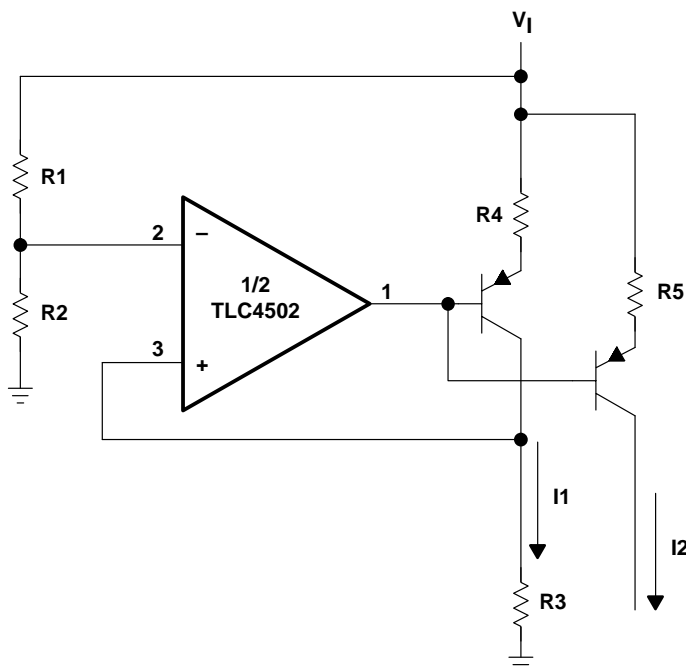


Figure 39. Fixed Current-Source Circuit

APPLICATION INFORMATION

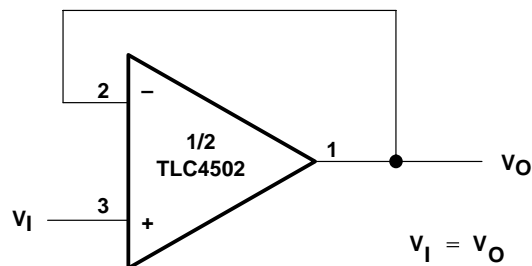


Figure 40. Voltage-Follower Circuit

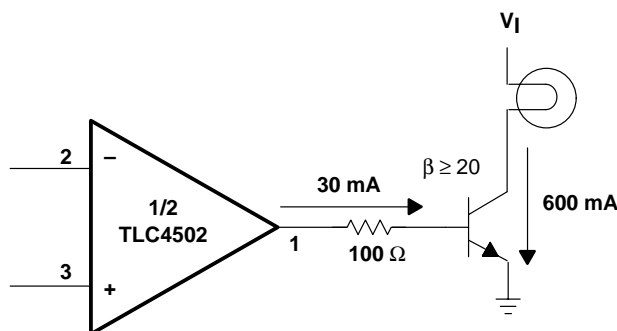


Figure 41. Lamp-Driver Circuit

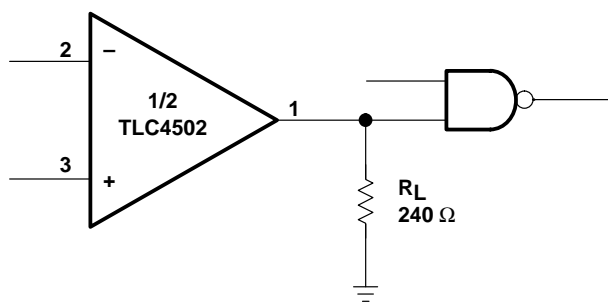


Figure 42. TTL-Driver Circuit

APPLICATION INFORMATION

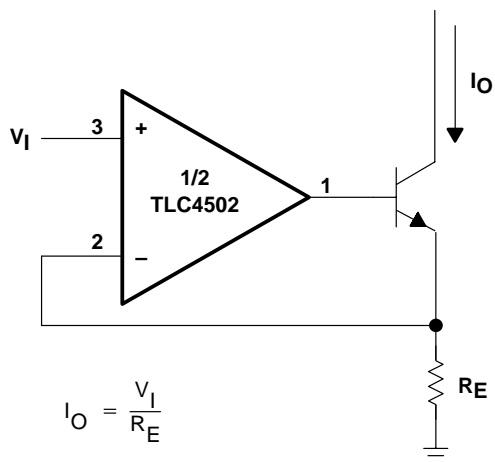


Figure 43. High-Compliance Current-Sink Circuit

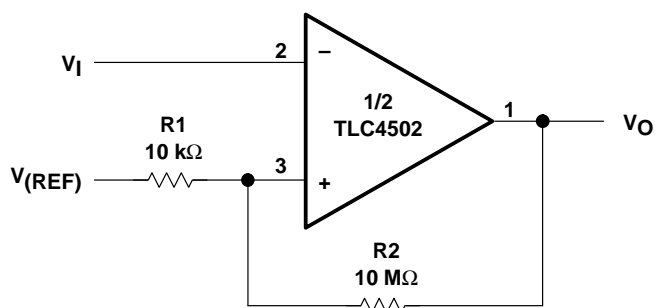


Figure 44. Comparator With Hysteresis Circuit

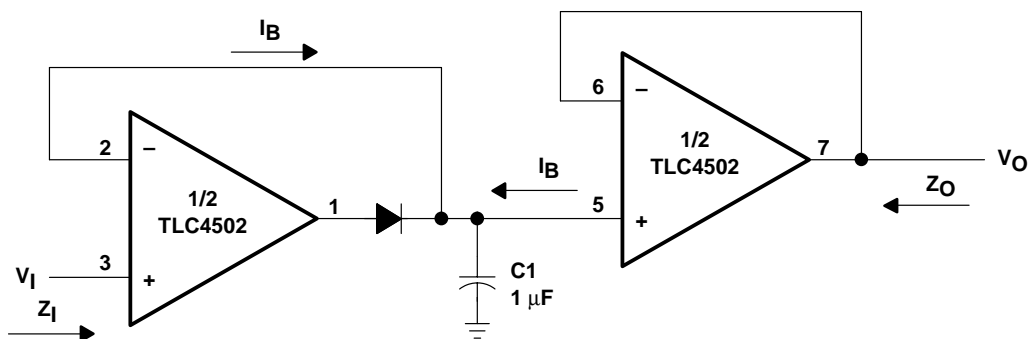


Figure 45. Low-Drift Detector Circuit

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 4) and subcircuit in Figure 46 are generated using the TLC4501 typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

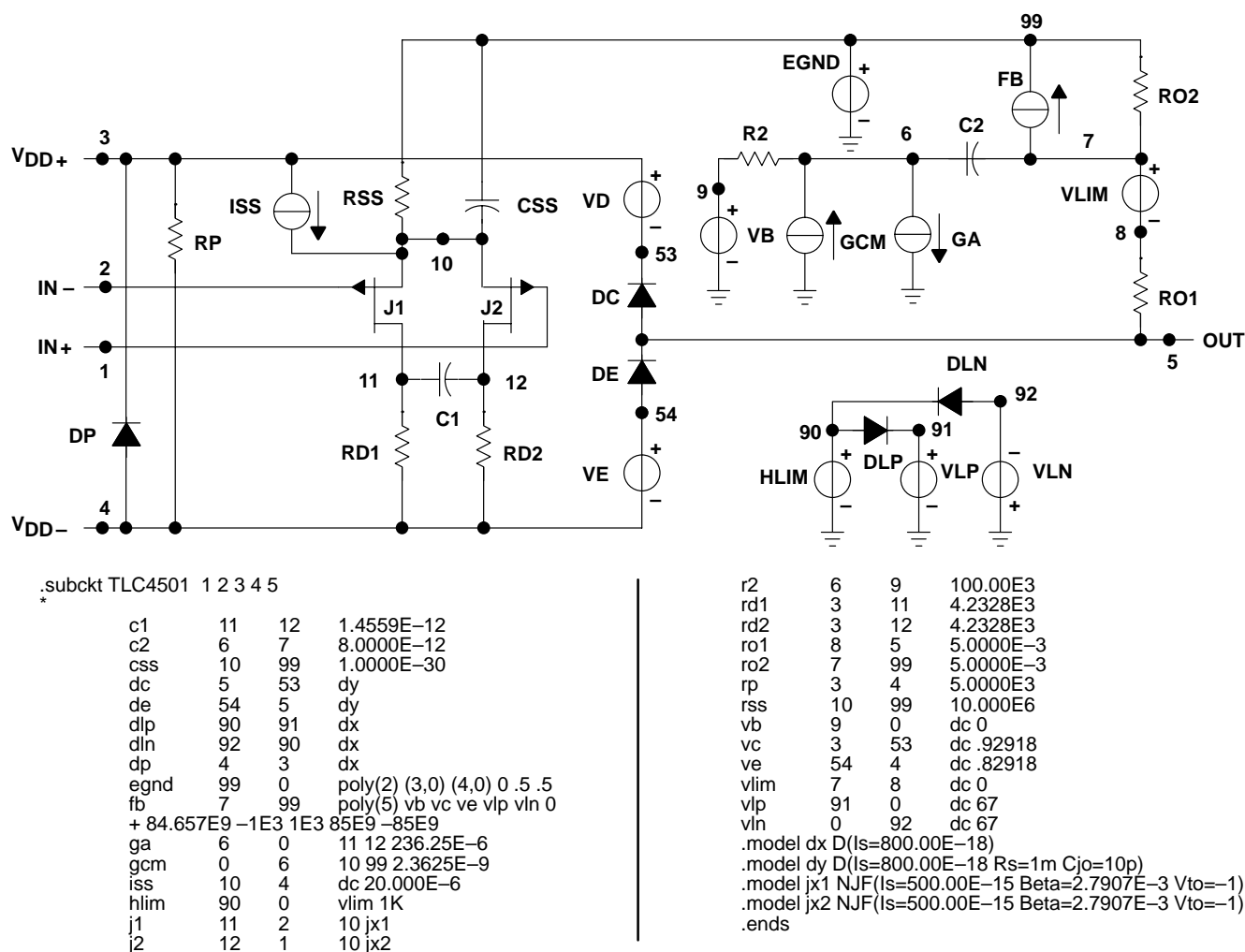


Figure 46. Boyle Macromodel and Subcircuit

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9753701Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9753701Q2A TLC4502 MFKB	Samples
5962-9753701QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9753701QHA TLC4502M	Samples
5962-9753701QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9753701QPA TLC4502M	Samples
5962-9753702Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9753702Q2A TLC4502 AMFKB	Samples
5962-9753702QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9753702QHA TLC4502AM	Samples
5962-9753702QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9753702QPA TLC4502AM	Samples
TLC4501ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4501AC	Samples
TLC4501AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4501AI	Samples
TLC4501AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4501AI	Samples
TLC4501AQD	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TLC4501AQDR	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TLC4501CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4501C	Samples
TLC4501CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4501C	Samples
TLC4501ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4501I	Samples
TLC4501IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4501I	Samples
TLC4501IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4501I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC4501IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4501I	Samples
TLC4501QD	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TLC4501QDR	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
TLC4502ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502AC	Samples
TLC4502ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502AC	Samples
TLC4502ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502AC	Samples
TLC4502ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502AC	Samples
TLC4502AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502AI	Samples
TLC4502AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502AI	Samples
TLC4502AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502AI	Samples
TLC4502AMD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	4502AM	Samples
TLC4502AMDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502AM	Samples
TLC4502AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9753702Q2A TLC4502 AMFKB	Samples
TLC4502AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9753702QPA TLC4502AM	Samples
TLC4502AMUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9753702QHA TLC4502AM	Samples
TLC4502AQD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	C4502A	
TLC4502AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C4502A	Samples
TLC4502AQDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	C4502A	
TLC4502AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C4502A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC4502CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502C	Samples
TLC4502CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502C	Samples
TLC4502CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502C	Samples
TLC4502CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502C	Samples
TLC4502ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502I	Samples
TLC4502IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502I	Samples
TLC4502IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502I	Samples
TLC4502IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502I	Samples
TLC4502MD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-55 to 125	4502M	
TLC4502MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		4502M	Samples
TLC4502MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9753701Q2A TLC4502 MFKB	Samples
TLC4502MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLC4502MJG	Samples
TLC4502MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9753701QPA TLC4502M	Samples
TLC4502MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9753701QHA TLC4502M	Samples
TLC4502QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C4502Q	Samples
TLC4502QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C4502Q	Samples
TLC4502QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	C4502Q	
TLC4502QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C4502Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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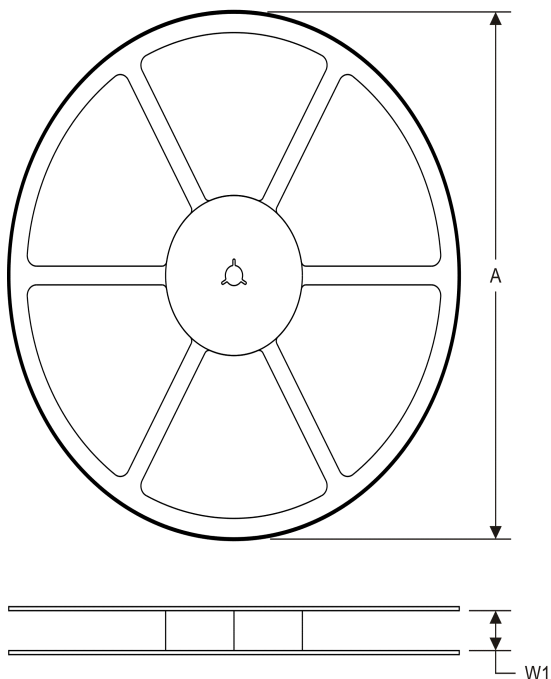
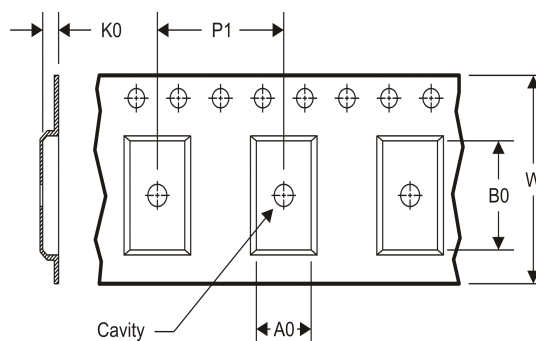
OTHER QUALIFIED VERSIONS OF TLC4502, TLC4502A, TLC4502AM, TLC4502M :

● Catalog: [TLC4502A](#), [TLC4502](#)

● Military: [TLC4502M](#), [TLC4502AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


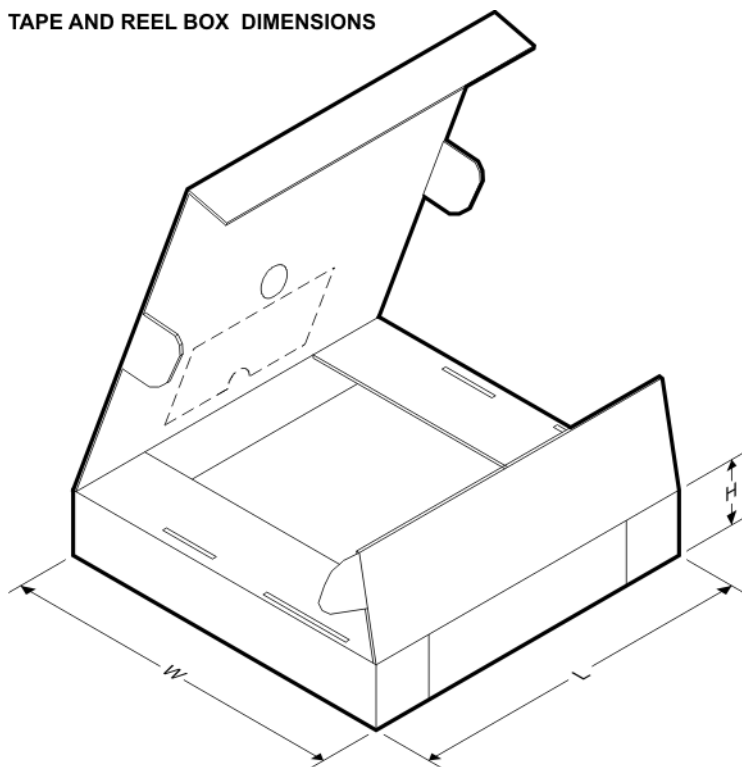
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC4501AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC4501IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC4502ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC4502AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC4502CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC4502IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

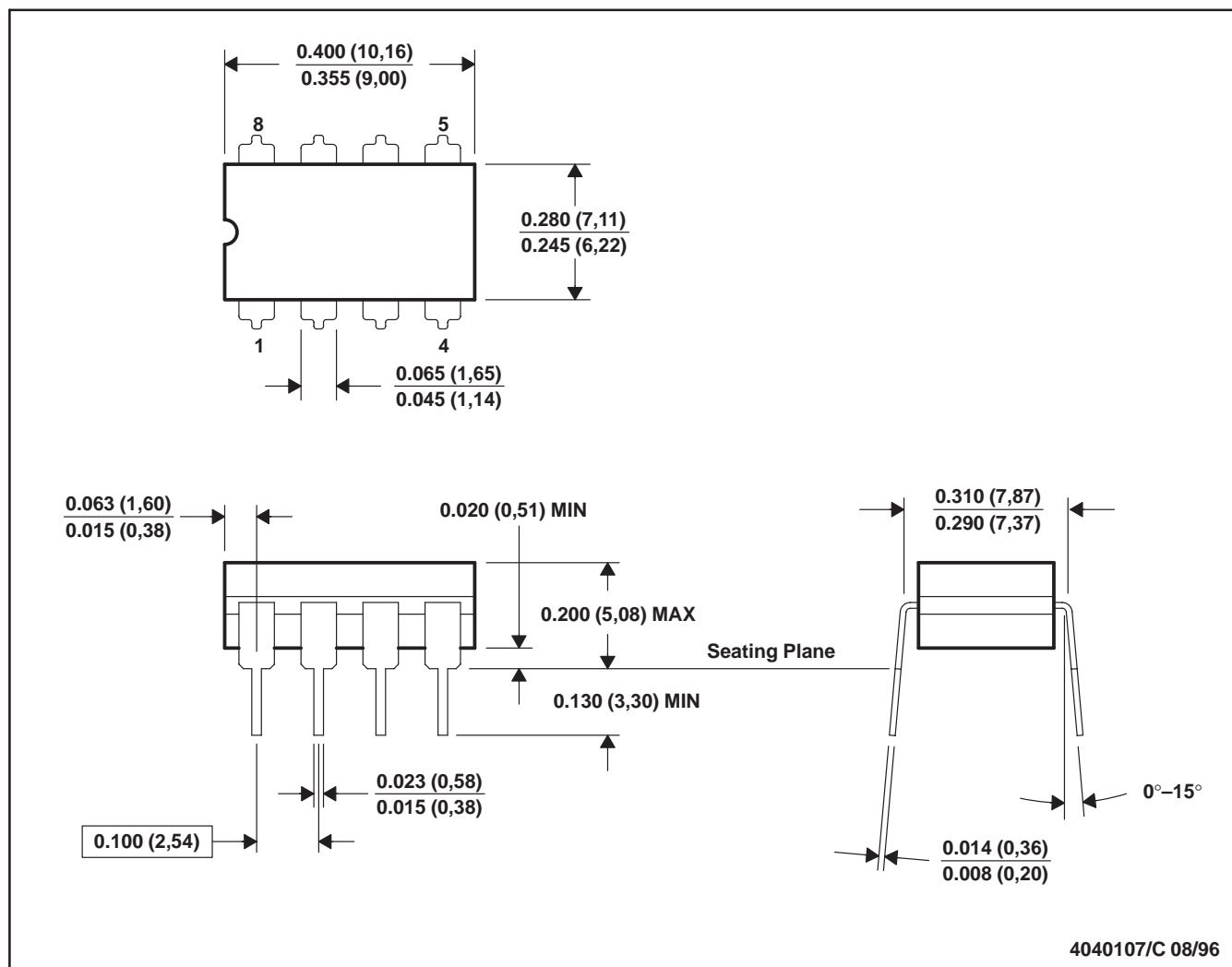


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC4501AIDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC4501IDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC4502ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC4502AIDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC4502CDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC4502IDR	SOIC	D	8	2500	367.0	367.0	35.0

JG (R-GDIP-T8)

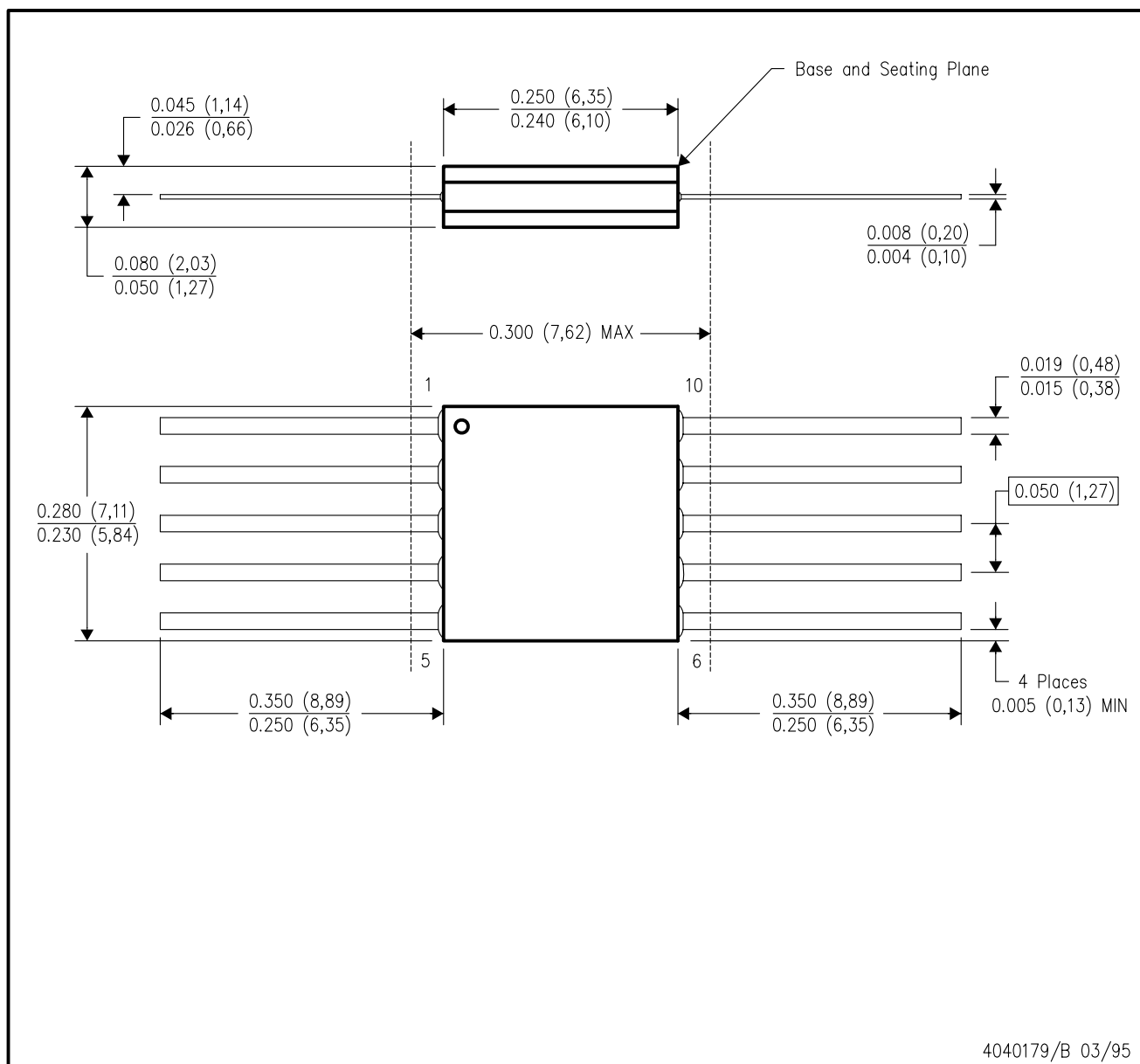
CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification.
 - E. Falls within MIL STD 1835 GDIP1-T8

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK

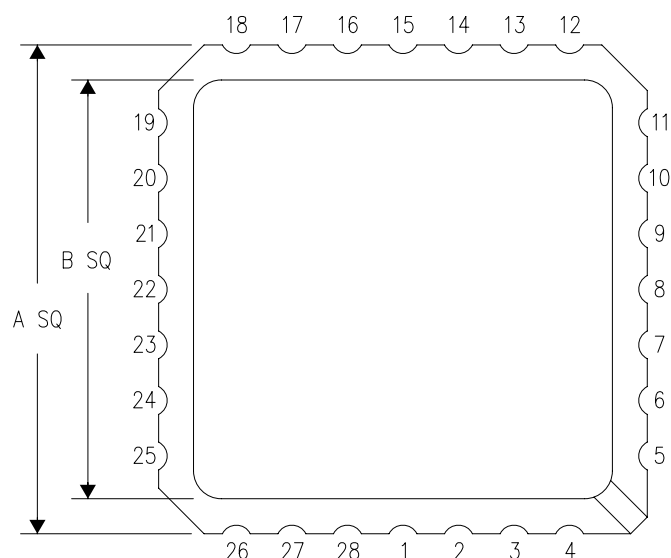


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

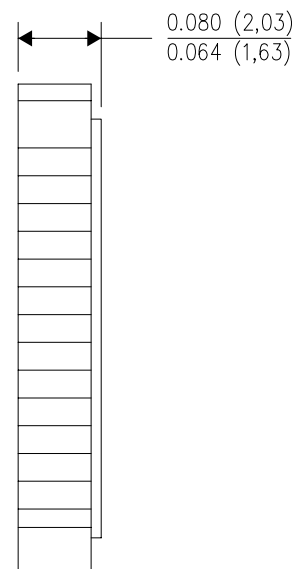
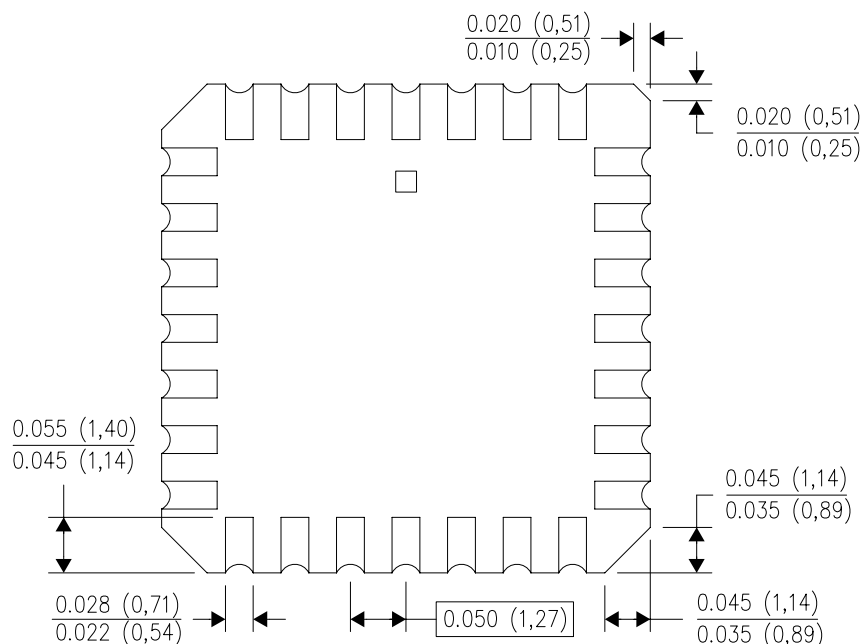
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

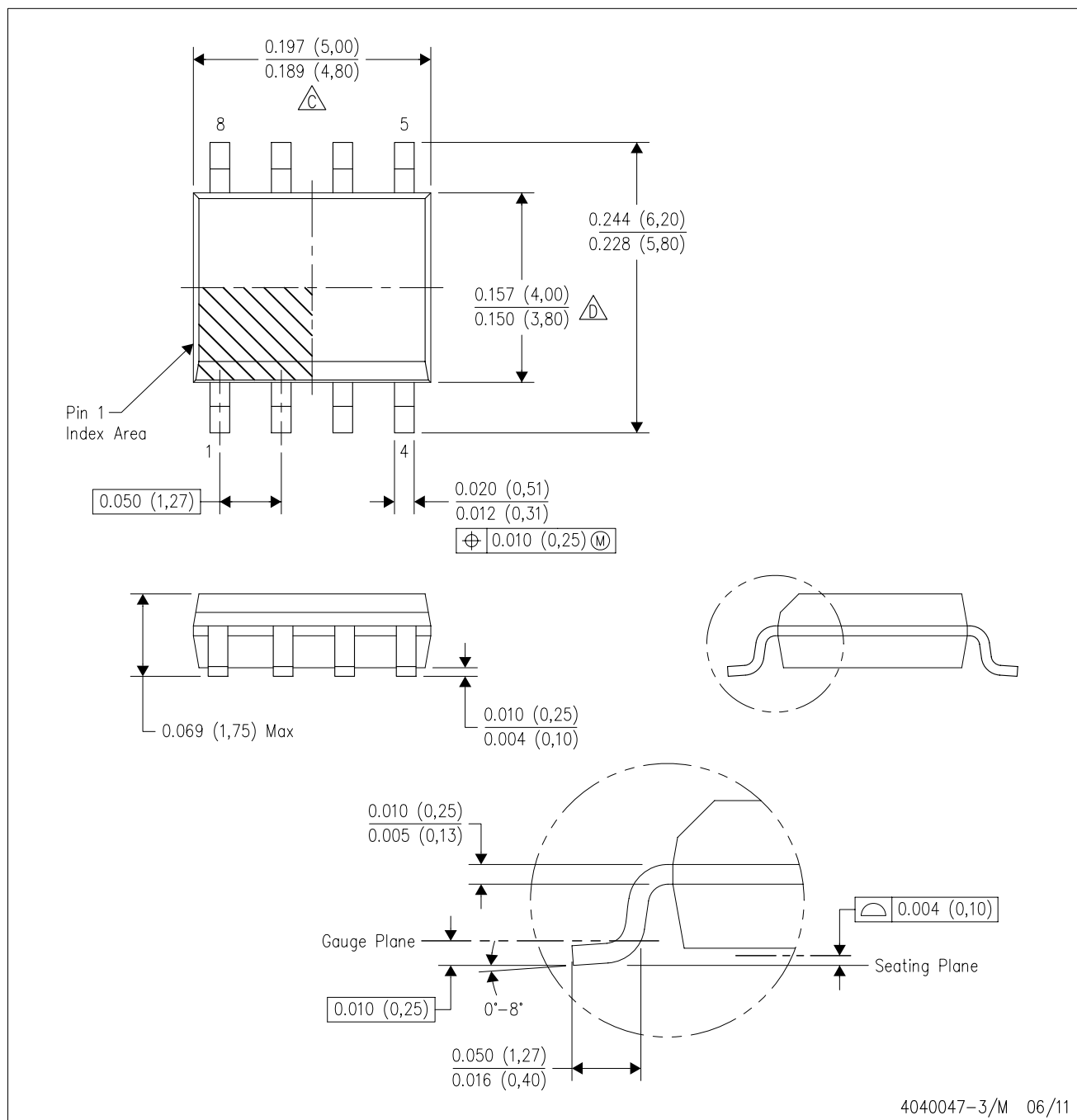


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

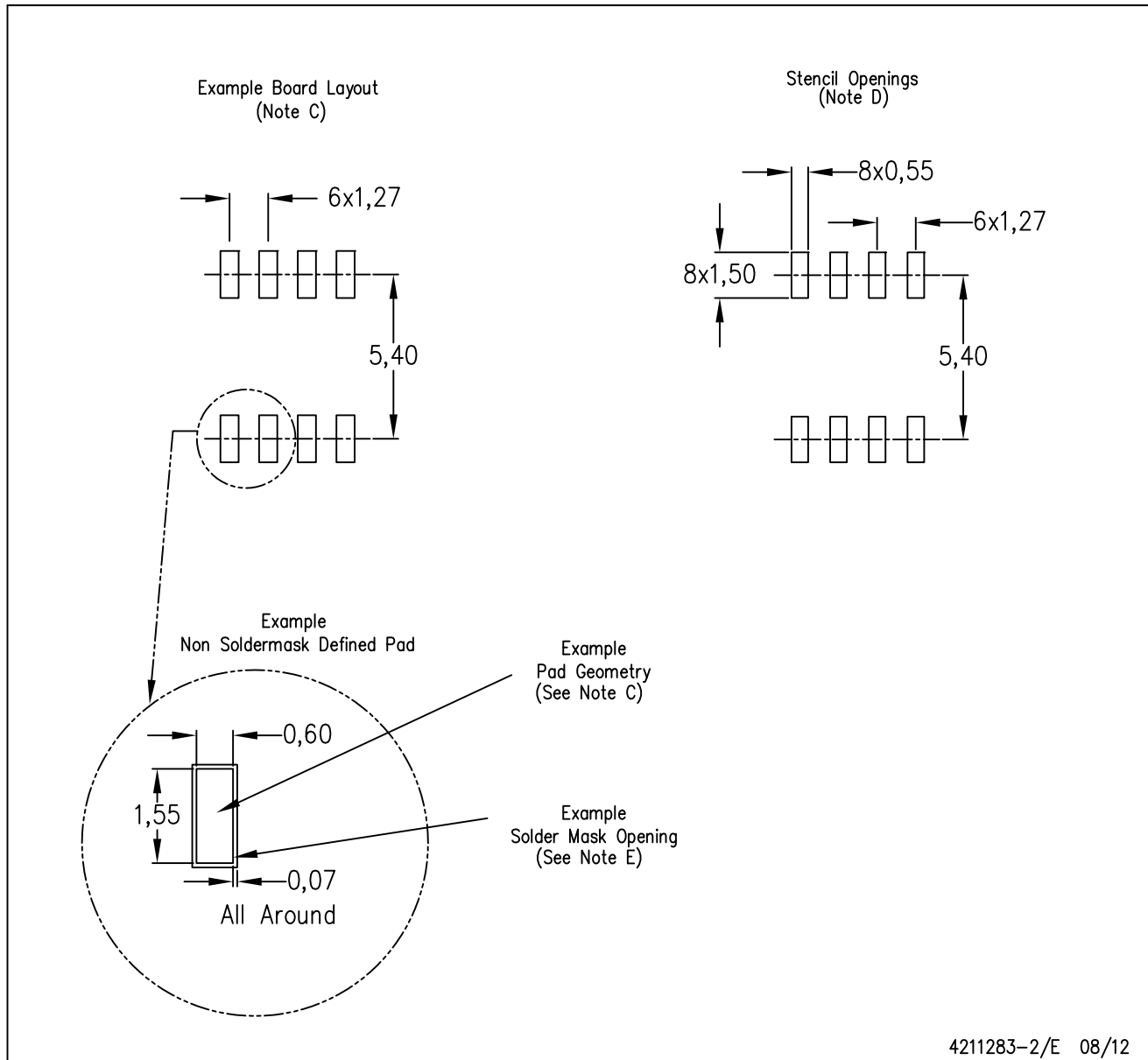


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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