



**QUAD/DUAL N-CHANNEL MATCHED MOSFET ARRAY**

**GENERAL DESCRIPTION**

The ALD1106/ALD1116 are monolithic quad/dual N-channel enhancement mode matched MOSFET transistor arrays intended for a broad range of precision analog applications. The ALD1106/ALD1116 offer high input impedance and negative current temperature coefficient. The transistor pairs are matched for minimum offset voltage and differential thermal response, and they are designed for switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. These MOSFET devices feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. The ALD1106/ALD1116 are building blocks for differential amplifier input stages, transmission gates, and multiplexer applications, current sources and many precision analog circuits.

**FEATURES**

- Low threshold voltage of 0.7V
- Low input capacitance
- Low Vos 2mV typical
- High input impedance -- 10<sup>14</sup>Ω typical
- Negative current (I<sub>DS</sub>) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain 10<sup>9</sup>
- Low input and output leakage currents

**ORDERING INFORMATION**

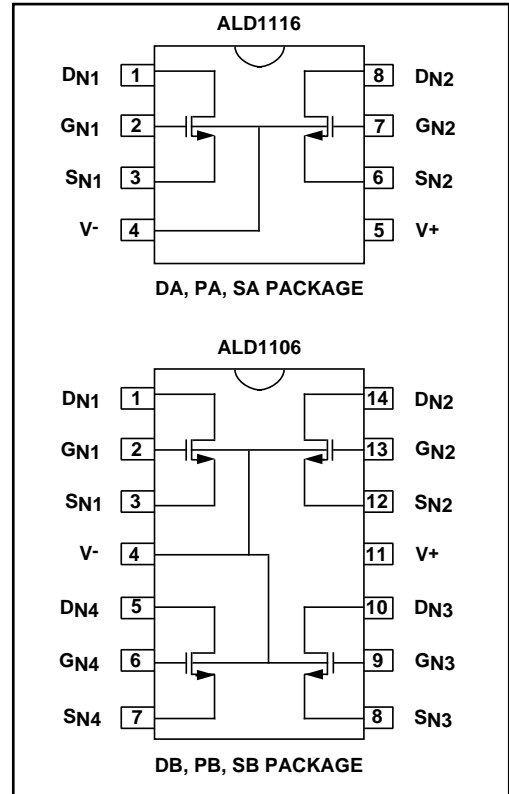
Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
8-Pin Cerdip Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD1116 DA	ALD1116 PA	ALD1116 SA
14-Pin Cerdip Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1106 DB	ALD1106 PB	ALD1106 SB

\* Contact factory for industrial temperature range.

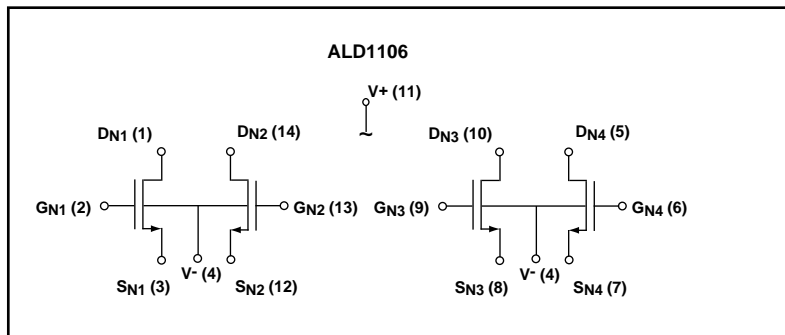
**APPLICATIONS**

- Precision current mirrors
- Precision current sources
- Voltage choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog signal processing

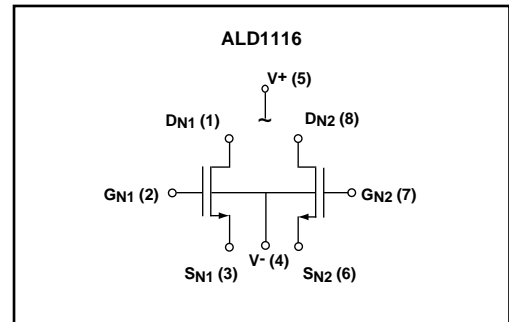
**PIN CONFIGURATION**



**BLOCK DIAGRAM**



**BLOCK DIAGRAM**



## ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, $V_{DS}$	13.2V
Gate-source voltage, $V_{GS}$	13.2V
Power dissipation	500 mW
Operating temperature range	PA, SA, PB, SB package 0°C to +70°C DA, DB package -55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature, 10 seconds	+260°C

## OPERATING ELECTRICAL CHARACTERISTICS

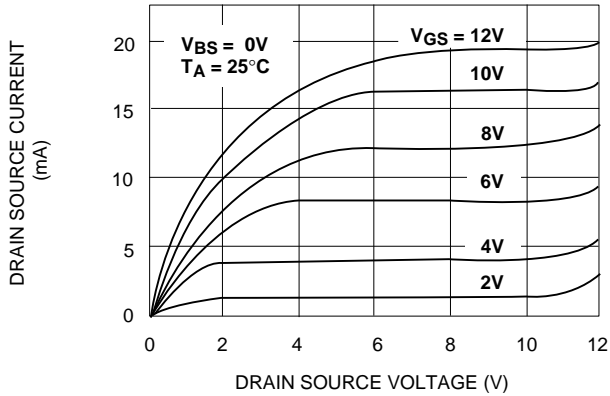
$T_A = 25^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	ALD1106			ALD1116			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Gate Threshold Voltage	$V_T$	0.4	0.7	1.0	0.4	0.7	1.0	V	$I_{DS} = 1.0\mu\text{A}$ $V_{GS} = V_{DS}$
Offset Voltage $V_{GS1} - V_{GS2}$	$V_{OS}$		2	10		2	10	mV	$I_{DS} = 10\mu\text{A}$ $V_{GS} = V_{DS}$
Gate Threshold Temperature Drift <sup>2</sup>	$TC_{VT}$		-1.2			-1.2		mV/°C	
On Drain Current	$I_{DS(ON)}$	3.0	4.8		3.0	4.8		mA	$V_{GS} = V_{DS} = 5V$
Transconductance	$G_{IS}$	1.0	1.8		1.0	1.8		mmho	$V_{DS} = 5V$ $I_{DS} = 10\text{mA}$
Mismatch	$\Delta G_{IS}$		0.5			0.5		%	
Output Conductance	$G_{OS}$		200			200		$\mu\text{mho}$	$V_{DS} = 5V$ $I_{DS} = 10\text{mA}$
Drain Source On Resistance	$R_{DS(ON)}$		350	500		350	500	$\Omega$	$V_{DS} = 0.1V$ $V_{GS} = 5V$
Drain Source On Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5			0.5		%	$V_{DS} = 0.1V$ $V_{GS} = 5V$
Drain Source Breakdown Voltage	$BV_{DSS}$	12			12			V	$I_{DS} = 1.0\mu\text{A}$ $V_{GS} = 0V$
Off Drain Current <sup>1</sup>	$I_{DS(OFF)}$		10	400 4		10	400 4	pA nA	$V_{DS} = 12V$ $V_{GS} = 0V$ $T_A = 125^\circ\text{C}$
Gate Leakage Current	$I_{GSS}$		0.1	10 1		0.1	10 1	pA nA	$V_{DS} = 0V$ $V_{GS} = 12V$ $T_A = 125^\circ\text{C}$
Input Capacitance <sup>2</sup>	$C_{ISS}$		1	3		1	3	pF	

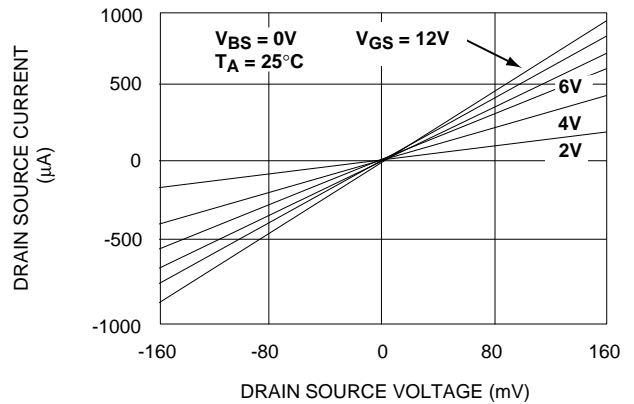
Notes: <sup>1</sup> Consists of junction leakage currents  
<sup>2</sup> Sample tested parameters

# TYPICAL PERFORMANCE CHARACTERISTICS

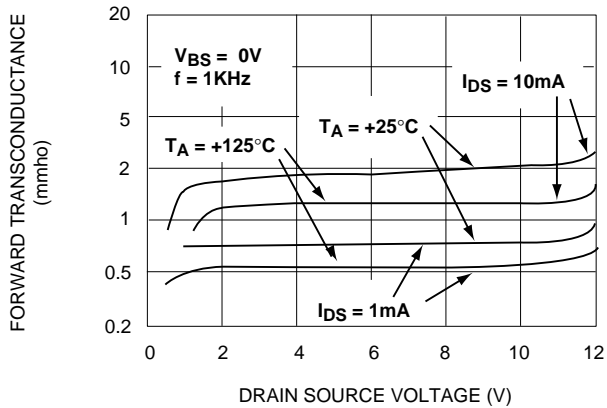
## OUTPUT CHARACTERISTICS



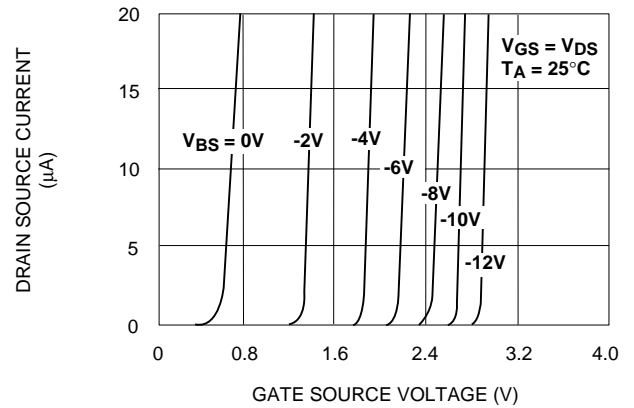
## LOW VOLTAGE OUTPUT CHARACTERISTICS



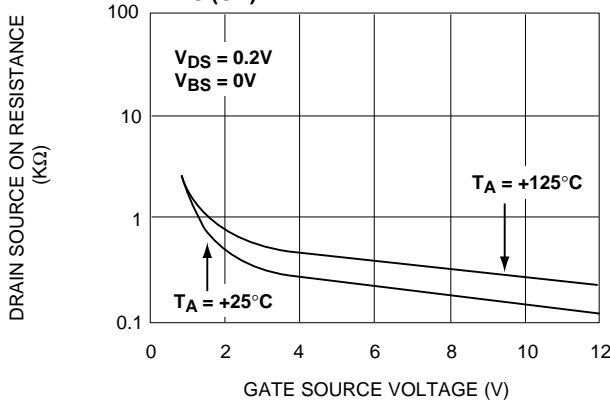
## FORWARD TRANSCONDUCTANCE vs. DRAIN SOURCE VOLTAGE



## TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



## DRAIN SOURCE ON RESISTANCE $R_{DS(ON)}$ vs. GATE SOURCE VOLTAGE



## OFF DRAIN CURRENT vs. AMBIENT TEMPERATURE

