

IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

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Thank you for your cooperation and understanding,

WeEn Semiconductors



BT134-600

4Q Triac

21 November 2013

Product data sheet

1. General description

Planar passivated four quadrant triac in a SOT82 plastic package intended for use in general purpose bidirectional switching and phase control applications.

2. Features and benefits

- Compact package
- High blocking voltage capability
- Less sensitive gate for improved noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	600	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25^\circ\text{C}$; $t_p = 20 \text{ ms}$; Fig. 4 ; Fig. 5		-	-	25	A
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_{mb} \leq 107^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3		-	-	4	A
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2+ G+; $T_j = 25^\circ\text{C}$; Fig. 7		-	5	35	mA
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2+ G-; $T_j = 25^\circ\text{C}$; Fig. 7		-	8	35	mA
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2- G-; $T_j = 25^\circ\text{C}$; Fig. 7		-	11	35	mA



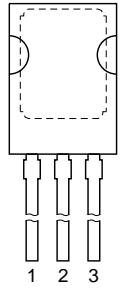
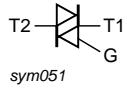
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$V_D = 12 \text{ V}$; $I_T = 0.1 \text{ A}$; T2- G+; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 7		-	30	70	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2	 SIP3 (SOT82)	

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT134-600	SIP3	plastic single-ended package; 3 leads (in-line)	SOT82

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C; Fig. 1 ; Fig. 2 ; Fig. 3		-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4 ; Fig. 5		-	25	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	27	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	3.1	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ μ s; T2+ G+		-	50	A/μ s
		$I_T = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ μ s; T2+ G-		-	50	A/μ s
		$I_T = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ μ s; T2- G-		-	50	A/μ s
		$I_T = 6$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/ μ s; T2- G+		-	10	A/μ s
I_{GM}	peak gate current			-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C

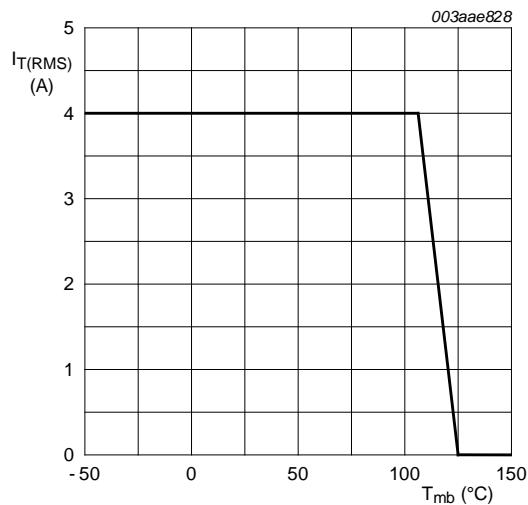
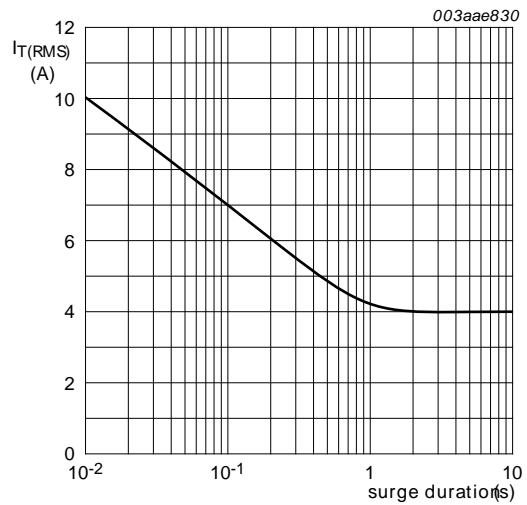
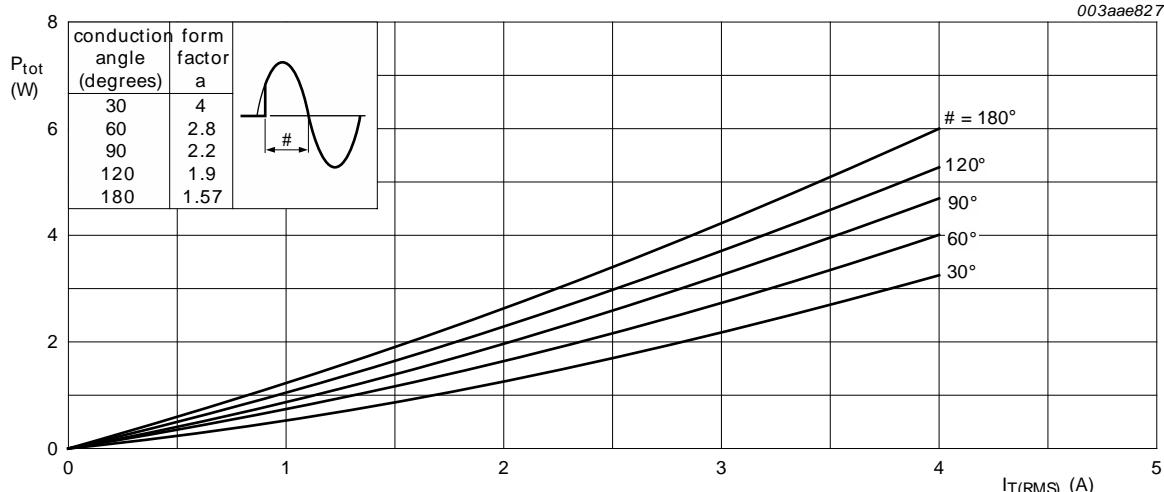


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



$f = 50$ Hz
 $T_{mb} \leq 107$ °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle
 a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

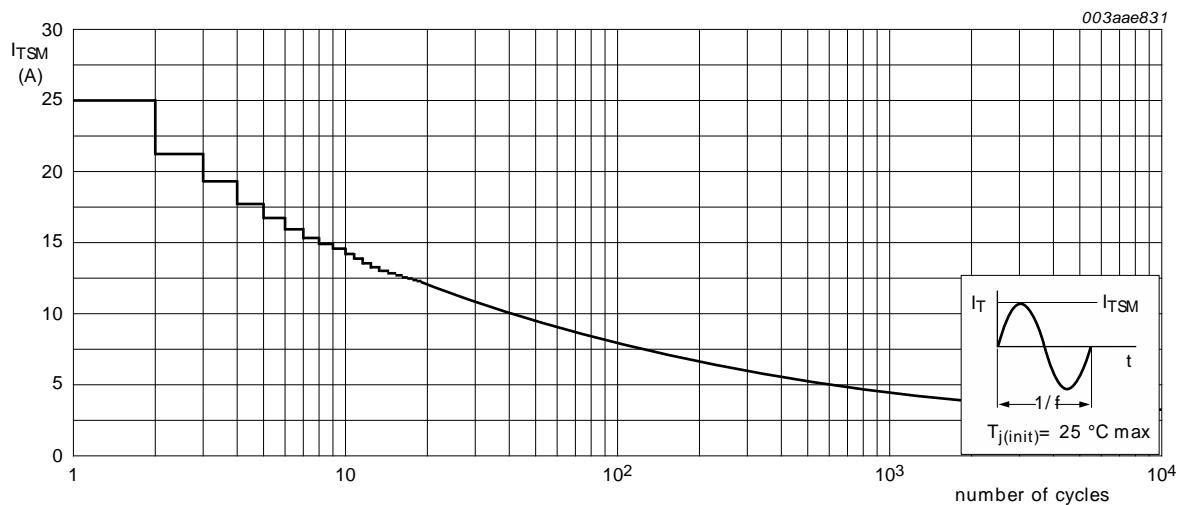


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

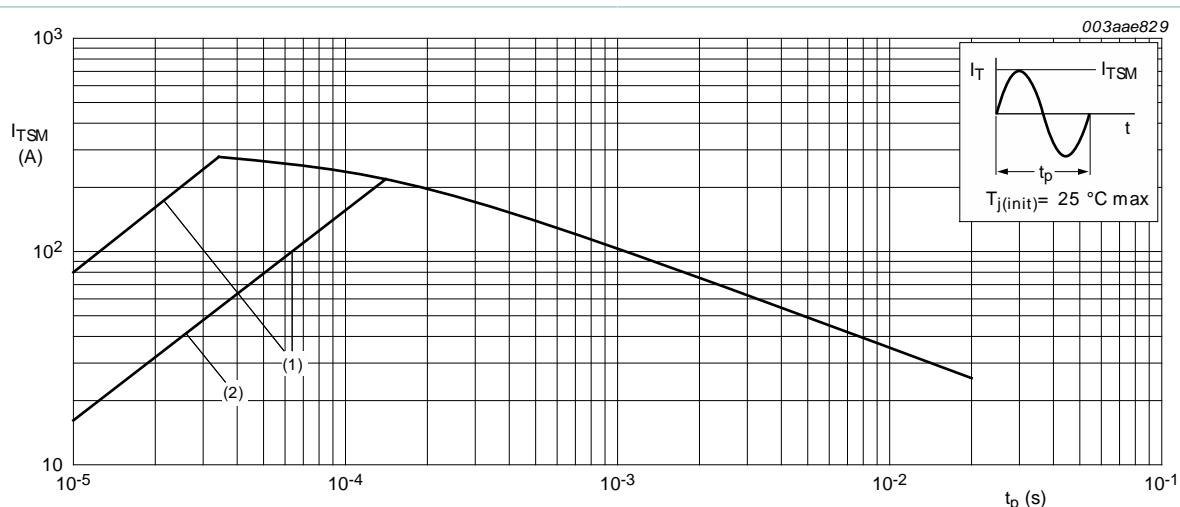


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	half cycle; Fig. 6	-	-	3.7	K/W
		full cycle; Fig. 6	-	-	3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	100	-	K/W

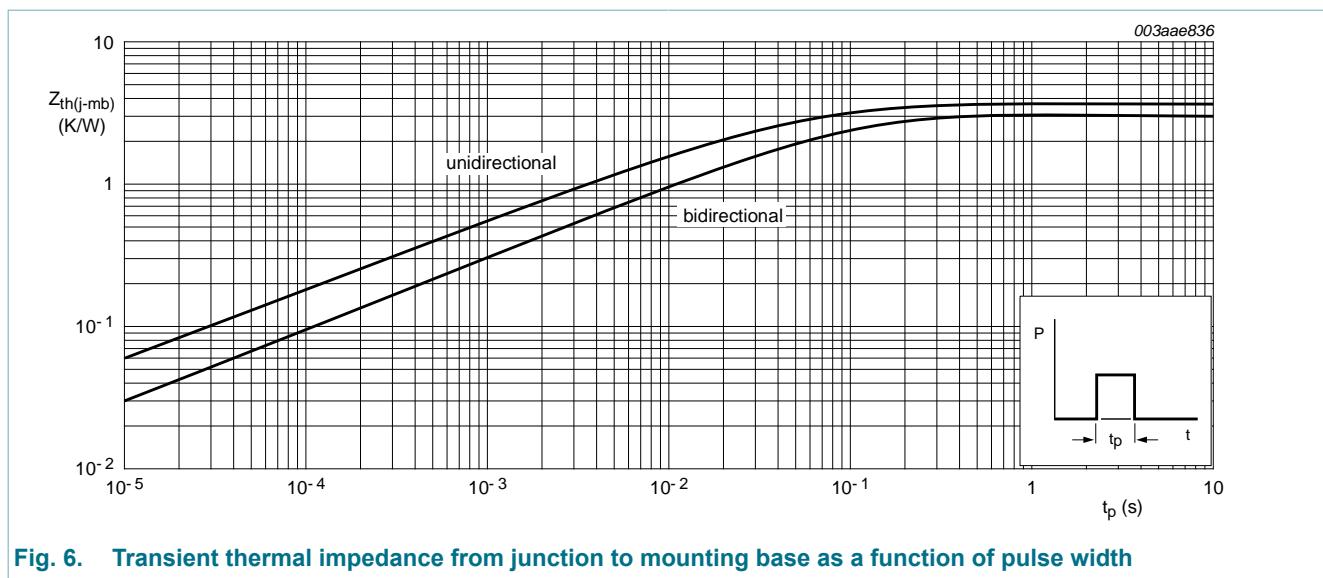


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7		-	5	35	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7		-	8	35	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7		-	11	35	mA
		V _D = 12 V; I _T = 0.1 A; T2- G+; T _j = 25 °C; Fig. 7		-	30	70	mA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 8		-	7	20	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 8		-	16	30	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 8		-	5	20	mA
		V _D = 12 V; I _G = 0.1 A; T2- G+; T _j = 25 °C; Fig. 8		-	7	30	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9		-	5	15	mA
V _T	on-state voltage	I _T = 5 A; T _j = 25 °C; Fig. 10		-	1.4	1.7	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11		-	0.7	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11		0.25	0.4	-	V
I _D	off-state current	V _D = 600 V; T _j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 402 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit		100	250	-	V/μs
dV _{com} /dt	rate of change of commutating voltage	V _D = 400 V; T _j = 95 °C; dI _{com} /dt = 1.8 A/ms; I _T = 4 A; gate open circuit		-	50	-	V/μs
t _{gt}	gate-controlled turn-on time	I _{TM} = 6 A; V _D = 600 V; I _G = 0.1 A; dI _G /dt = 5 A/μs		-	2	-	μs

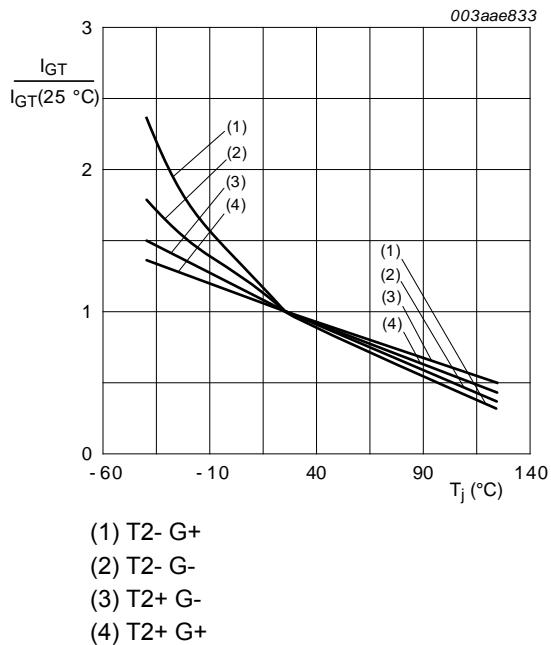


Fig. 7. Normalized gate trigger current as a function of junction temperature

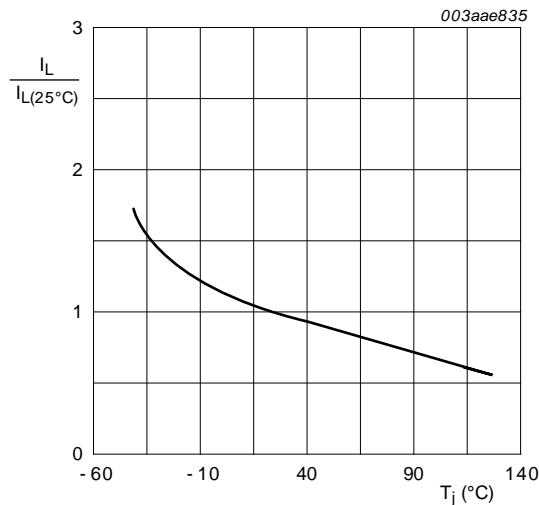


Fig. 8. Normalized latching current as a function of junction temperature

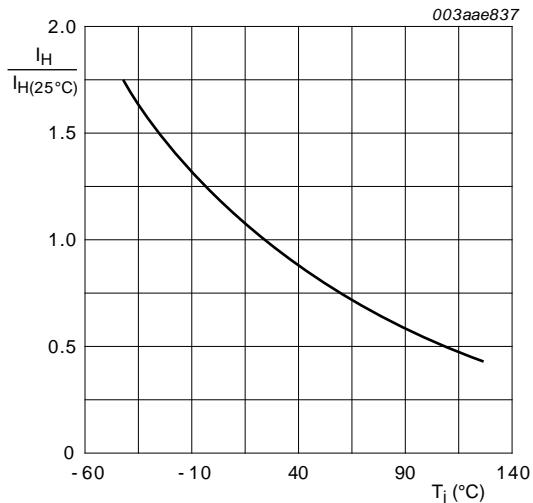


Fig. 9. Normalized holding current as a function of junction temperature

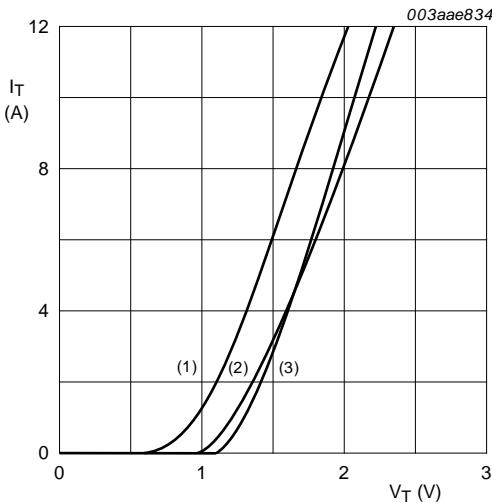


Fig. 10. On-state current as a function of on-state voltage

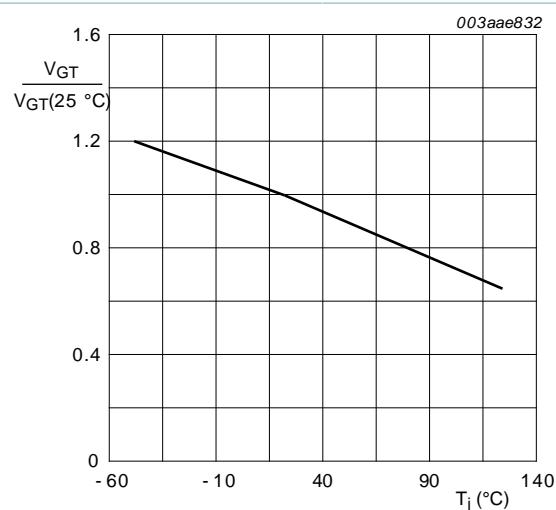
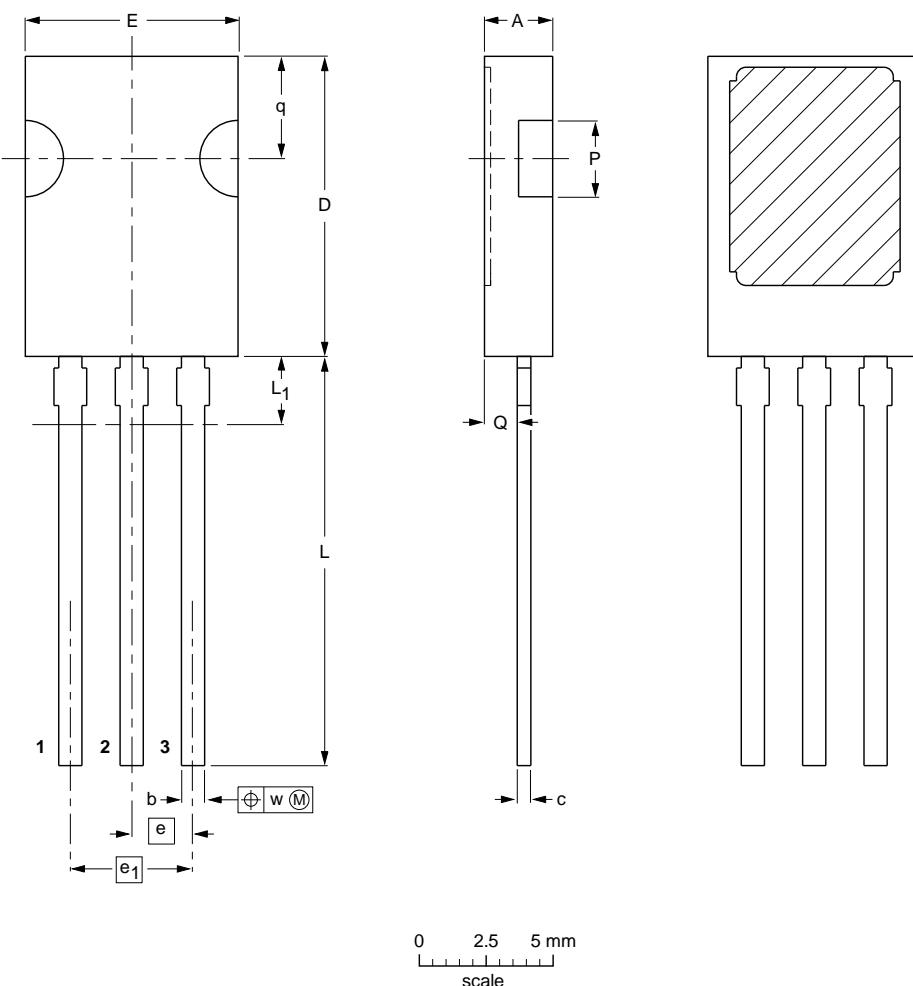


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

Plastic single-ended package; 3 leads (in-line)

SOT82



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	e ₁	L	L ₁ ⁽¹⁾ max.	P	Q	q	w
mm	2.8	0.88	0.58	11.1	7.8	2.29	4.58	16.5	2.54	3.1	1.5	3.9	0.254
	2.3	0.65	0.47	10.5	7.2			15.3	2.5	2.5	0.9	3.5	

Note

1. Terminal dimensions within this zone are uncontrolled to allow for body and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT82						97-06-11

Fig. 12. Package outline SIP3 (SOT82)

11. Legal information

11.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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