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FAIRCHILD
SEMICONDUCTOR™

January 1996
Revised March 2001

74LCX821
Low Voltage 10-Bit D-Type Flip-Flop
with 5V Tolerant Inputs and Outputs

General Description

The LCX821 consists of ten D-type Flip-Flops with 3-STATE outputs for bus organized system applications. The device is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX821 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

■ 5V tolerant inputs and outputs

■ 2.3V–3.6V V_{CC} specifications provided

■ 7.0 ns t_{PD} max (V_{CC} = 3.3V), 10 µA I_{CC} max

■ Power-down high impedance inputs and outputs

■ Supports live insertion/withdrawal (Note 1)

■ ±24 mA output drive (V_{CC} = 3.0V)

■ Implements patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 500 mA

■ ESD performance:
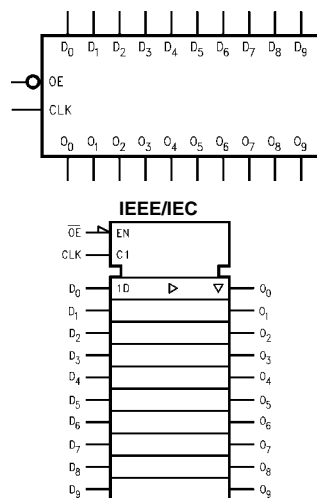   Human Body Model > 2000V
   Machine Model > 200V

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX821WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74LCX821MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX821MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix "X" to the ordering code.

Logic Symbols

IEEE/IEC

Connection Diagram

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Pin Descriptions

Pin Names	Description
D_0–D_9	Data Inputs
CLK	Clock Input
$\overline{OE}$	Output Enable Input
O_0–O_9	3-STATE Latch Outputs

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CLK	D	Q	O_n	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	╱	L	L	Z	Load
H	╱	H	H	Z	Load
L	╱	L	L	L	Data Available
L	╱	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impendance
╱ = LOW-to-HIGH Transition
NC = No Change

Functional Description

The LCX821 consists of ten edge-triggered flip-flops with individual D-type inputs with 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The ten flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CLK) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the ten flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram
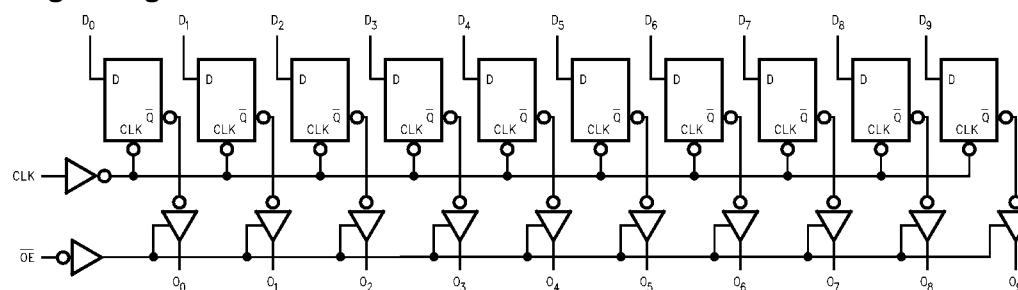
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24	mA
		V_{CC} = 2.7V – 3.0V		±12	
		V_{CC} = 2.3V – 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V – 2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.3 – 3.6	V_{CC} − 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.3 – 3.6		0.2	V
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 5.5V	2.3 – 3.6		±5.0	μA
		V_I = V_{IH} or V_{IL}				
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_CC (V)	T_A = −40°C to +85°C		Units
				Min	Max	
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 – 3.6		10	μA
		$3.6V \leq V_I$, $V_O \leq 5.5V$ (Note 5)	2.3 – 3.6		±10	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3 – 3.6		500	μA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

| Symbol	Parameter	T_A = −40°C to +85°C, R_L = 500Ω						Units
		V_CC = 3.3V ± 0.3V		V_CC = 2.7V		V_CC = 2.5V ± 0.2V		
		C_L = 50 pF		C_L = 50 pF		C_L = 30 pF		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150						MHz
t_{PHL}	Propagation Delay	1.5	7.0	1.5	7.5	1.5	8.4	ns
t_{PLH}	CLK to O_n	1.5	7.0	1.5	7.5	1.5	8.4	
t_{PZL}	Output Enable Time	1.5	7.5	1.5	8.0	1.5	9.8	ns
t_{PZH}		1.5	7.5	1.5	8.0	1.5	9.8	
t_{PLZ}	Output Disable Time	1.5	6.5	1.5	7.0	1.5	7.8	ns
t_{PHZ}		1.5	6.5	1.5	7.0	1.5	7.8	
t_{OSHL}	Output to Output Skew		1.0					ns
t_{OSLH}	(Note 6)		1.0					
t_S	Setup Time, D_n to CLK	2.5		2.5		4.0		ns
t_H	Hold Time, D_n to CLK	1.5		1.5		2.0		ns
t_W	CLK Pulse Width	3.3		3.3		4.0		ns

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_CC (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.6	

Capacitance

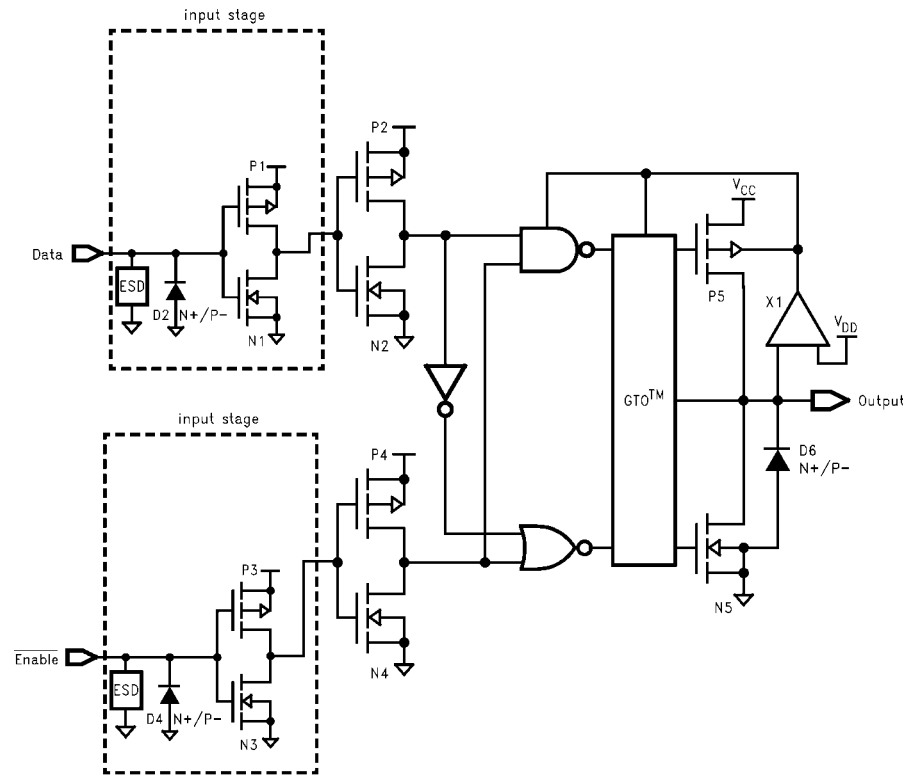| Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_O	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family
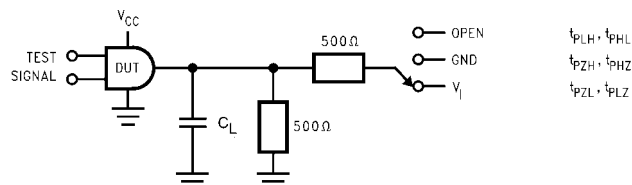
FIGURE 1. AC Test Circuit (C$_L$ includes probe and jig capacitance)

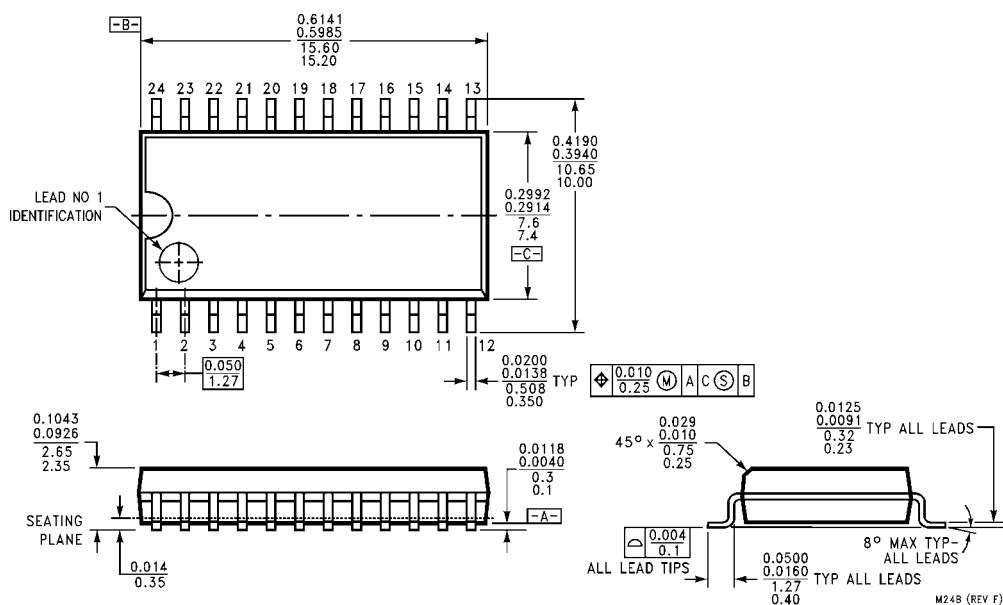| Test	Switch
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 ± 0.3V V$_{CC}$ x 2 at V$_{CC}$ = 2.5 ± 0.2V
t$_{PZH}$, t$_{PHZ}$	GND
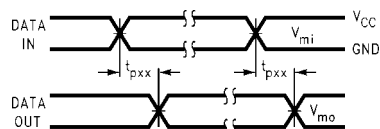
Waveform for Inverting and Non-Inverting Functions
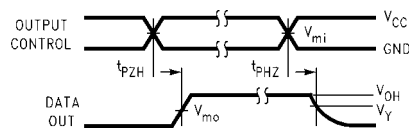
3-STATE Output High Enable and
Disable Times for Logic
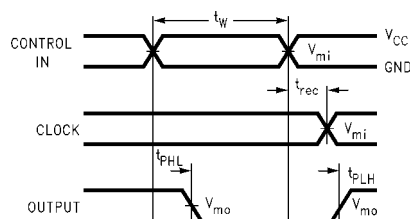
Propagation Delay. Pulse Width and t$_{rec}$ Waveforms
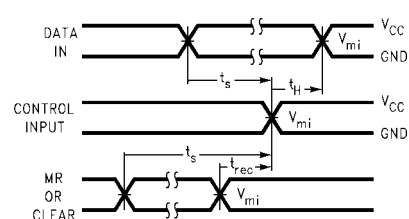
Setup Time, Hold Time and Recovery Time for Logic
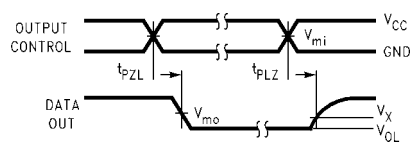
3-STATE Output Low Enable and
Disable Times for Logic

t$_{rise}$ and t$_{fall}$
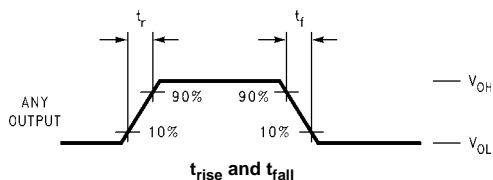
FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t$_r$ = t$_f$ = 3ns)

Symbol	V$_{CC}$		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V$_{mi}$	1.5V	1.5V	V$_{CC}$/2
V$_{mo}$	1.5V	1.5V	V$_{CC}$/2
V$_x$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V
V$_y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V

Schematic Diagram Generic for LCX Family

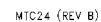# Physical Dimensions inches (millimeters) unless otherwise noted

-B-

0.6141
0.5985
15.60
15.20

24 23 22 21 20 19 18 17 16 15 14 13

0.4190
0.3940
10.65
10.00

LEAD NO 1
IDENTIFICATION

0.2992
0.2914
7.6
7.4
-C-

1 2 3 4 5 6 7 8 9 10 11 12

0.050
1.27

0.0200
0.0138
0.508
0.350 TYP

⊕ | 0.010 Ⓜ | A | C Ⓢ | B
0.25

0.1043
0.0926
2.65
2.35

0.0118
0.0040
0.3
0.1

0.029
45° x 0.010
0.75
0.25

0.0125
0.0091
0.32 TYP ALL LEADS
0.23

SEATING
PLANE

-A-

⌂ | 0.004
0.1

ALL LEAD TIPS

0.014
0.35

8° MAX TYP
ALL LEADS

0.0500
0.0160
1.27 TYP ALL LEADS
0.40

M24B (REV F)

24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

24   13

1.50

Ø1.2

1   12

2.85

8.40 MAX
8.20 ± 0.05
-A-

0.53 ± 0.12

1.80 ± 0.05
0.800 ± 0.025

0.30 ± 0.10 TYP

0.65 TYP

0.15 +0.05
−0.10 TYP

⌂ | 0.10
-C-

⊕ | 0.12 Ⓜ | C | A Ⓢ | B Ⓢ

7.90 ± 0.20
5.30 ± 0.05
-B-

0.20 ± 0.05
L/F THICKNESS

4° ± 3°
TYP

0.60 ± 0.15
TYP

MSA24 (REV A)
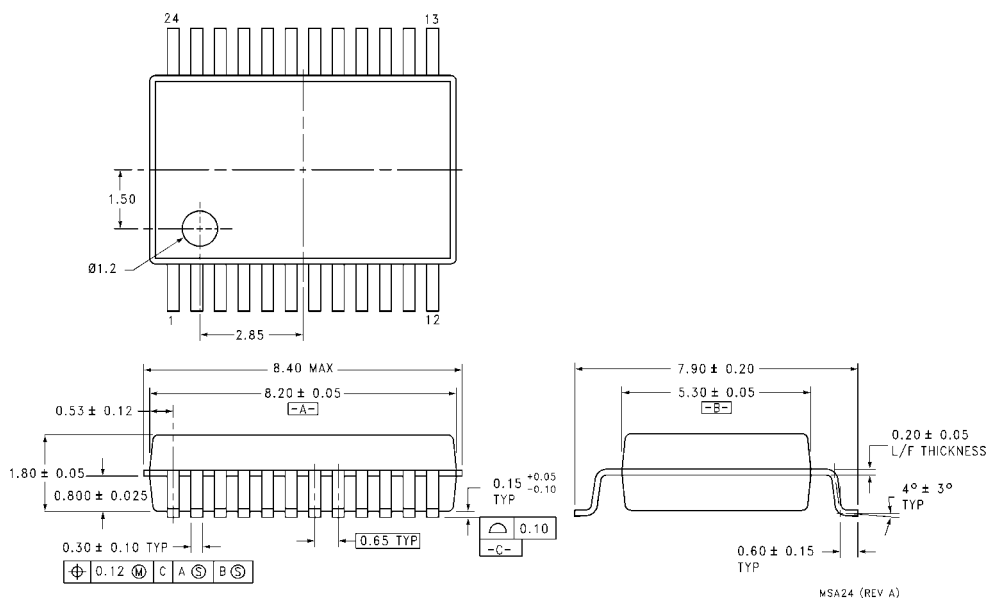
24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA24

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

7.72

4.16

(1.78 TYP)

0.42 TYP

0.65 TYP

LAND PATTERN RECOMMENDATION

7.8 ± 0.1

-A-

24   13

6.4

3.2

4.4 ± 0.1

-B-

1   12

0°–8°

☐ 0.2 C B A
ALL LEAD TIPS

GAGE PLANE

0.25

SEATING PLANE

0.6 ± 0.1

DETAIL A
TYPICAL

SEE DETAIL D

☐ 0.1 C
ALL LEAD TIPS

-C-

0.65 TYP

0.19 – 0.30 TYP

(0.90)

1.1 MAX

0.10 ± 0.05 TYP

0.09–0.20 TYP

⊕ 0.13 Ⓜ A B Ⓢ C Ⓢ

MTC24 (REV B)

**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24**

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PUBLICATION ORDERING INFORMATION

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