M66238FP

Standard Clock Generator with PLL Frequency Synthesizer

REJ03F0268-0200
Rev.2.00
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Description

The M66238 is a LSI that incorporates a PLL synthesizer and a sync clock generator in it. The PLL synthesizer covers the range of 25 MHz to 50 MHz at the minimum steps of 3 kHz.

The sync circuit outputs a clock and a one-shot pulse which are synchronized with an external trigger signal. Setting a dividing ratio allows acquisition of sync clock outputs within the range of 0.78 MHz to 25 MHz.

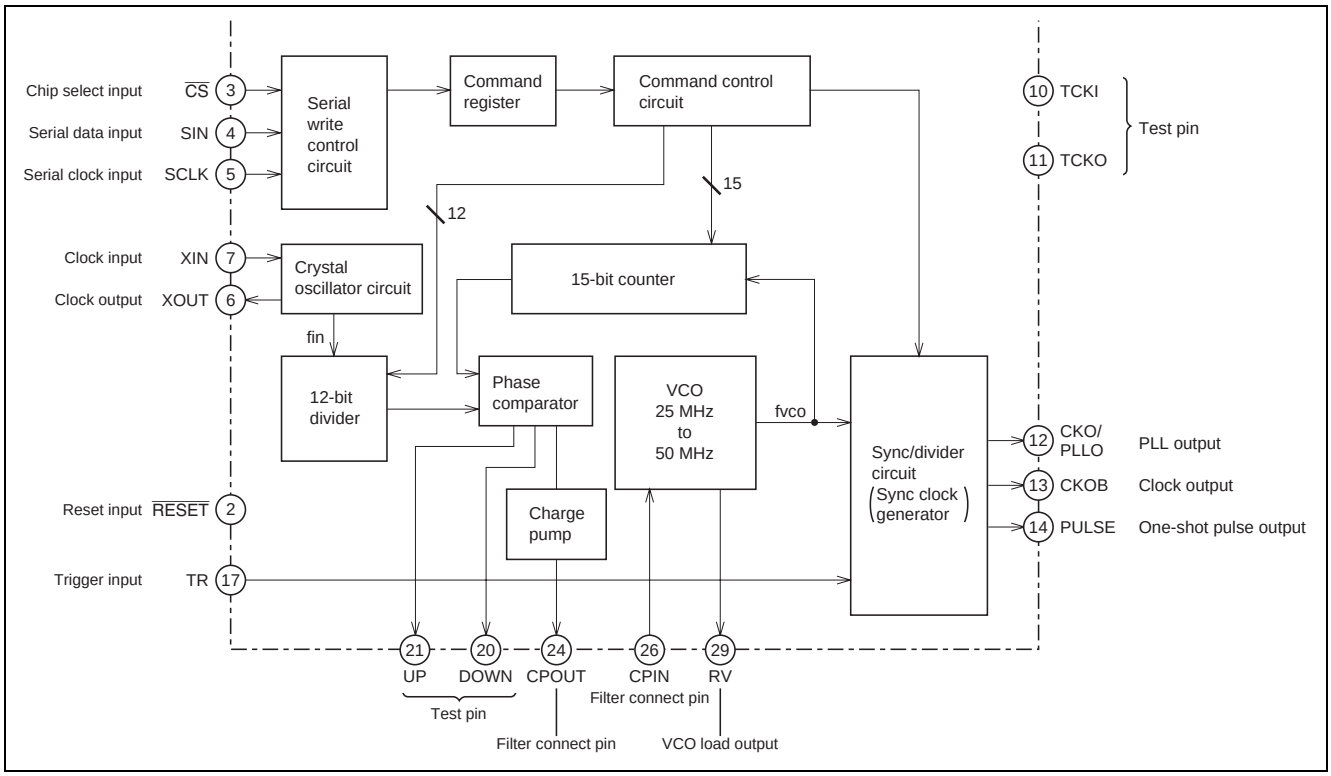
Features

- Sync clock output frequency range: 1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of 25 to 50 MHz
- Sync accuracy (jitter): ±3 ns
- Trigger input: Polarity selectable
- One-shot pulse output: Polarity and width selectable
- 5 V power supply

Application

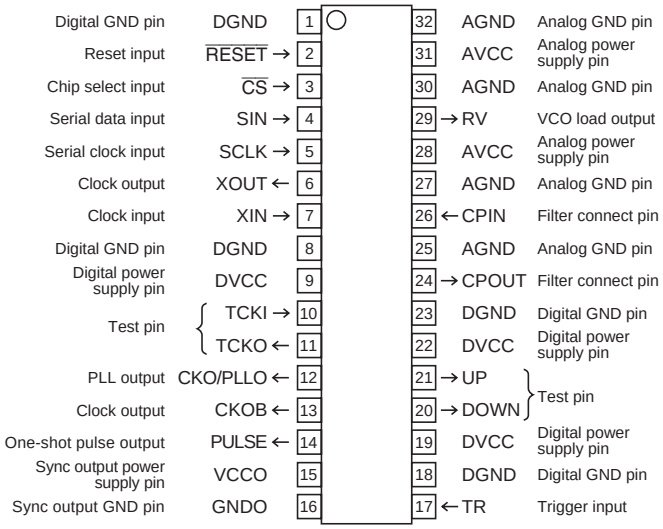
Pixel clock generator

Block Diagram



Pin Arrangement

M66238FP



(Top view)

Outline: 32P2W-A

Pin Description

Pin Name	Name	I/O	Function
$\overline{\text{RESET}}$	Reset input	Input	Initialize M66238 internal status.
$\overline{\text{CS}}$	Chip select input	Input	Transfer serial data when $\overline{\text{CS}}$ = "L".
SIN	Serial data input	Input	Synchronize 32-bit serial data from MCU with SCK, and enter.
SCLK	Serial clock input	Input	Enter a sync clock for writing 32-bit serial data.
XIN	Clock input	Input	Used by connecting crystal oscillator between XIN and XOUT. When using an external clock signal, connect the clock oscillator to XIN pin and open XOUT pin.
XOUT	Clock output	Output	
TR	Trigger input	Input	Trigger input for clock sync.
CKOB	Clock output	Output	Output an inverted CKO signal.
CKO/PLLO	PLL output	Output	CKO outputs a clock synchronized with a trigger signal and PLLO outputs a PLL oscillator clock as it is.
PULSE	One-shot pulse output	Output	Output a one-shot pulse synchronized with a CKO signal.
CPOUT	Filter connect pin	Output	Connect a low pass filter to charge pump output.
CPIN	Filter connect pin	Input	Low pass filter input pin.
RV	VCO load output	Output	Connect a load resistor for VCO circuit operation between RV and GND.
TCKI	Test pin	Input	Shipping test pin. Connect to GND when use.
TCKO	Test pin	Output	Shipping test pin. Keep open when use.
UP	Test pin	Output	Shipping test pin. Keep open when use.
DOWN	Test pin	Output	Shipping test pin. Keep open when use.
DVCC	Digital power supply pin	—	Digital power supply pin.
DGND	Digital GND pin	—	Digital GND pin.
VCCO	Sync output power supply pin	—	Power supply pin for sync output.
GNDO	Sync output GND pin	—	GND pin for sync output.
AVCC	Analog power supply pin	—	Analog power supply pin.
AGND	Analog GND pin	—	Analog GND pin.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	Vcc	–0.5 to +7.0	V
Input voltage	Vi	–0.5 to Vcc + 0.5	V
Output voltage	Vo	–0.5 to Vcc + 0.5	V
Power dissipation*[1]	Pd	650	mW
Storage temperature	Tstg	–65 to +150	°C

Note: 1. When board is mounted
All voltages adopt the GND pin of the circuit as the base (0 V) and absolute values are displayed for maximum and minimum values.

Recommended Operating Conditions

(Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.75	5	5.25	V
Supply voltage	GND	—	0	—	V
Input voltage	Vi	0	—	Vcc	V
Output voltage	Vo	0	—	Vcc	V
Operating ambient temperature	Topr	0	—	70	°C

Note: The direction of current flowing into a circuit is defined to be positive (no sign) and the direction of current flowing out is defined to be negative (–sign).
Absolute values are displayed for maximum and minimum values.

Electrical Characteristics

(Ta = 0 to 70°C, Vcc = 5 V ± 5%, GND = 0 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
High-level input voltage	VIH	2	—	—	V	TR
Low-level input voltage	VIL	—	—	0.8	V	
High-level input voltage	VIH	0.8 × Vcc	—	—	V	XIN
Low-level input voltage	VIL	—	—	0.2 × Vcc	V	
High-level output voltage	VOH	Vcc – 0.8	—	—	V	GND = 0 V, IOH = –4 mA
Low-level output voltage	VOL	—	—	0.55	V	GND = 0 V, IOL = 4 mA
Supply current (at time of standstill)	Icc (s)	—	—	50	μA	GND = 0 V, VI = Vcc or GND
Supply current (at time of operation)	Icc (a)	—	—	120	mA	GND = 0 V, CKO = 50 MHz VI = Vcc or GND
High-level input current	IIH	—	—	10	μA	GND = 0 V, VI = Vcc
Low-level input current	IIL	—	—	–10	μA	GND = 0 V, VI = 0 V
Input capacitance	CI	—	—	10	pF	

Note: Measurement circuit; The direction of current flowing to the circuit is specified to be positive (no sign).

Timing Requirements

(Ta = 0 to 70°C, Vcc = 5 V ± 5%, GND = 0 V)

Item	Symbol	Min	Typ	Max	Unit
CS width	tw ($\overline{CS}$)	1	—	—	µs
CS set up time	tsu ($\overline{CS}$-SCK)	50	—	—	ns
CS hold time	th (SCK-$\overline{CS}$)	50	—	—	ns
SCK width	tw (SCK)	25	—	—	ns
SIN set up time	tsu (SIN-SCK)	25	—	—	ns
SIN hold time	th (SCK-SIN)	25	—	—	ns
Clock input frequency	fin	7	—	12	MHz
Clock input duty	fiDUTY	40	—	60	%
Trigger input "H" pulse width	tw (TR)	200	—	—	ns
Clock input rising time	tr	—	—	5	ns
Clock input falling time	tf	—	—	5	ns

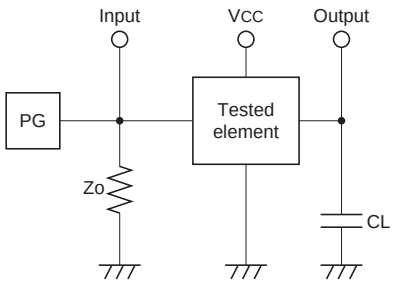
Switching Characteristics

(Ta = 0 to 70°C, Vcc = 5 V ± 5%, GND = 0 V, CL = 15 pF)

Item	Symbol	Min	Typ	Max	Unit
VCO oscillation frequency	fvco	25	—	50	MHz
Synchronous output frequency	fout	—	—	50	MHz
Synchronous accuracy (jitter)	Δt	—	—	±3	ns
Synchronous clock output start	tss (CKO)	—	—	tlp + 200	ns
Synchronous clock reversible output start	tss (CKOB)	—	—	tlp + 200	ns
One-shot pulse output start	tss (PULSE)	—	—	tlp + 200	ns
Synchronous clock output stop	tsp (CKO)	—	—	40	ns
Synchronous clock reversible output stop	tsp (CKOB)	—	—	40	ns
One-shot pulse output width	tw (PULSE)	n • tp – 10	—	n • tp + 10	ns
Synchronous clock output duty	fo_{DUTY} (CKO)	40	—	60	%
Synchronous clock reversible output duty	fo_{DUT} (CKOB)	40	—	60	%

Note: tp = 1 / fout, tlp = tp × (100 – fvcoduty) / 100
The n value of one-shot pulse output width is set in the register.

Measurement Circuit

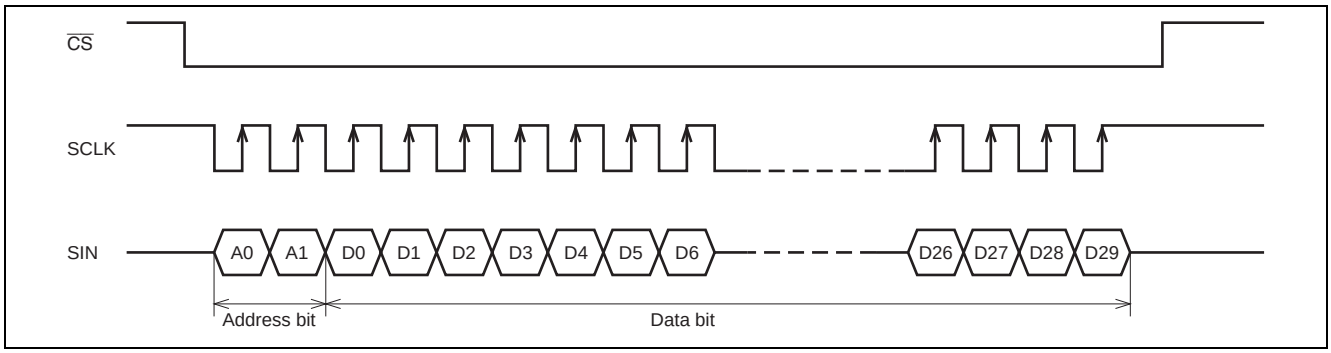


Notes:
- Waveform for switching test
  - Input pulse level XIN: 0 to Vcc, TR: 0 to 3 V
  - Input pulse rising time: 3 ns
  - Input pulse falling time: 3 ns
  - Zo: 50 Ω
  - Decision voltage — Input voltage: XIN: Vcc/2, Tr: 1.3 V
  - Output voltage: All outputs: Vcc/2
- Electrostatic capacitance: CL includes floating capacitance of connection and probe input capacitance.

List of Register Setting Commands

A1	A0	Setting
0	0	Setting of CKO/PLLO dividing ratio, PLL synthesizer 15-bit generation dividing ratio and reference clock generation 12-bit dividing ratio.
1	0	Setting of one-shot pulse polarity and width, setting of trigger edge, HALT of entire M66238, HALT of charge pump and VCO, phase comparator output UP/DOWN, CKO/PLLO switching.
1	1	Dummy trigger generation command

Serial Data Write Timing



Register Configuration

1. Clock frequency setting command
   Reference clock generation 12-bit division ratio, PLL synthesizer 15-bit division ratio and CKO/PLLO division ratio are set at address (A1, A0) = (0, 0).

Data Bit		Description	Default
D0	0	12-bit reference clock dividing ratio is set. D11 and D0 correspond to MSB and LSB, respectively. $K = \sum_{k=0}^{11} (Dk \times 2^k)$ K: Reference clock dividing ratio	0
	1		
D1	0		1
	1		
D2	0		0
	1		
D3	0		1
	1		
D4	0		0
	1		
D5	0		0
	1		
D6	0		0
	1		
D7	0		0
	1		
D8	0		1
	1		
D9	0		0
	1		
D10	0		0
	1		
D11	0		0
	1		
D12	0	15-bit PLL synthesizer dividing ratio is set. D26 and D12 correspond to MSB and LSB, respectively. $N = \sum_{n=12}^{26} (Dn \times 2^{n-12})$ N: PLL synthesizer dividing ratio	0
	1		
D13	0		0
	1		
D14	0		0
	1		
D15	0		1
	1		
D16	0		0
	1		
D17	0		1
	1		
D18	0		1
	1		
D19	0		1
	1		
D20	0		1
	1		
D21	0		1
	1		
D22	0		0
	1		
D23	0		0
	1		
D24	0		0
	1		
D25	0		0
	1		
D26	0		0
	1		

<table>
<tr><th>Data Bit</th><th></th><th>Description</th><th>Default</th></tr>
<tr><td rowspan="2">D27</td><td>0</td><td rowspan="6">Setting of CKO/PLLO dividing ratios
<table><tr><th>Dividing Ratio</th><th>D29</th><th>D28</th><th>D27</th><th>PLLO/CKO Oscillator Frequency</th></tr><tr><td>1/1</td><td>0</td><td>0</td><td>0</td><td>25 MHz to 50 MHz</td></tr><tr><td>1/2</td><td>0</td><td>0</td><td>1</td><td>12.5 MHz to 25 MHz</td></tr><tr><td>1/4</td><td>0</td><td>1</td><td>0</td><td>6.25 MHz to 12.5 MHz</td></tr><tr><td>1/8</td><td>0</td><td>1</td><td>1</td><td>3.125 MHz to 6.25 MHz</td></tr><tr><td>1/16</td><td>1</td><td>0</td><td>0</td><td>1.563 MHz to 3.125 MHz</td></tr><tr><td>1/32</td><td>1</td><td>0</td><td>1</td><td>0.781 MHz to 1.563 MHz</td></tr></table></td><td rowspan="2">0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D28</td><td>0</td><td rowspan="2">1</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D29</td><td>0</td><td rowspan="2">0</td></tr>
<tr><td>1</td></tr>
</table>

2. Operating mode setting commands
   Address (A1, A0) = (1, 0) allows setting of one-shot pulse polarity and width, trigger edge, M66238 entire halt, charge pump and VCO halt, phase comparator UP/DOWN output, LPF cutoff, CKO/PLLO switching, VCO switching and charge pump switching.

<table>
<tr><th>Data Bit</th><th></th><th>Description</th><th>Default</th></tr>
<tr><td>D0</td><td>0
1</td><td>Setting of trigger edge
<table><tr><th>D1</th><th>D0</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>Synchronizes with TR ↓ CKO is stopped when TR = "H"</td></tr><tr><td>0</td><td>1</td><td>Synchronizes with TR ↑ CKO is stopped when TR = "L"</td></tr><tr><td>1</td><td>0</td><td>Synchronizes with TR ↑ CKO is output when TR = "H"</td></tr><tr><td>1</td><td>1</td><td>Synchronizes with TR ↓ CKO is output when TR = "L"</td></tr></table></td><td>0</td></tr>
<tr><td>D1</td><td>0
1</td><td></td><td>0</td></tr>
<tr><td>D2</td><td>0</td><td>When trigger occurs: spike of sync clock is not eliminated.</td><td>0</td></tr>
<tr><td></td><td>1</td><td>When trigger occurs: spike of sync clock is eliminated (disabled when D1 = 1).</td><td></td></tr>
<tr><td>D3</td><td>0</td><td>Polarity of one-shot pulse: Negative pulse</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Polarity of one-shot pulse: Positive pulse</td><td></td></tr>
<tr><td>D4</td><td>0
1</td><td>Setting of one-shot pulse width
<table><tr><th>D5</th><th>D4</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>CKO 2-cycle width</td></tr><tr><td>0</td><td>1</td><td>CKO 4-cycle width</td></tr><tr><td>1</td><td>0</td><td>CKO 8-cycle width</td></tr><tr><td>1</td><td>1</td><td>CKO 16-cycle width</td></tr></table></td><td>0</td></tr>
<tr><td>D5</td><td>0
1</td><td></td><td>0</td></tr>
<tr><td>D6</td><td>0</td><td>CKO/PLLO pin: CKO output</td><td>0</td></tr>
<tr><td></td><td>1</td><td>CKO/PLLO pin: PLLO output</td><td></td></tr>
<tr><td>D7</td><td>0</td><td>Entire M66238: Operating state</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Entire M66238: Halt state</td><td></td></tr>
<tr><td>D8</td><td>0</td><td>VCO: Operating state</td><td>0</td></tr>
<tr><td></td><td>1</td><td>VCO: Halt state</td><td></td></tr>
<tr><td>D9</td><td>0</td><td>Charge pump: ON</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Charge pump: OFF</td><td></td></tr>
<tr><td>D10</td><td>0</td><td>Low pass filter: Operating state</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Low pass filter: Separated</td><td></td></tr>
<tr><td>D11</td><td>0</td><td>Normal use: Not output to outside</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Phase comparator UP/DOWN output enable</td><td></td></tr>
<tr><td>D12</td><td>0</td><td>Normal use</td><td>0</td></tr>
<tr><td></td><td>1</td><td>VCO test circuit set</td><td></td></tr>
<tr><td>D13</td><td>0</td><td>Normal use</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Charge pump test circuit set</td><td></td></tr>
<tr><td>D14</td><td>0</td><td>Normal use</td><td>0</td></tr>
<tr><td></td><td>1</td><td>15-bit counter test clock enable</td><td></td></tr>
<tr><td>D15</td><td>0</td><td>Normal use</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Sync clock generator test clock enable</td><td></td></tr>
<tr><td>D16</td><td>0</td><td>Normal use</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Sync clock generator test input enable</td><td></td></tr>
<tr><td>D17</td><td>0</td><td>Normal use</td><td>0</td></tr>
<tr><td></td><td>1</td><td>12-bit counter test output enable</td><td></td></tr>
<tr><td>D18</td><td>0</td><td>Normal use</td><td>0</td></tr>
<tr><td></td><td>1</td><td>15-bit counter test output enable</td><td></td></tr>
<tr><td>D19</td><td>0</td><td>Normal use</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Sync clock generator trigger test output enable</td><td></td></tr>
<tr><td>D20</td><td>0</td><td>Normal use</td><td>0</td></tr>
<tr><td></td><td>1</td><td>Sync clock generator test output enable</td><td></td></tr>
<tr><td>D21
:
D29</td><td></td><td>In normal use: "0" set</td><td>0
:
0</td></tr>
</table>

3. Dummy trigger generating command

The internal status of sync clock generator becomes unstable and a stable sync clock output (CKO) is not obtained after the power is turned on, after a reset is cleared or after an internal VCO oscillator frequency is set. To obtain a stable sync clock output, enter a trigger signal from the TR input after VCO oscillator becomes stable, or enter a dummy trigger generating command from the MCU. The PLL synthesizer oscillator frequency after the cancellation of a reset depends on a default (See the register configuration).

Set the command for address (A1, A0) = (1, 1).

Data Bit		Description	Default
D0	0	The command must be stored two times continuously when a dummy trigger is generated. For the first time, set the dummy trigger generating command with D0 = 1. For the second time, set the dummy trigger generating command with D0 = 0. The second setting becomes a sync edge and a clock begins to be output from CKO. After the first setting, CKO is in the halt state.	0
	1		
D1	0	In normal use: "0"	0
	1		
↓			↓
D29	0		0
	1		

Operating Timing

1. Sync Clock Spike Non-removal Mode upon Occurrence of Trigger

1.1 Setting of Trigger Edge when D1 = 0

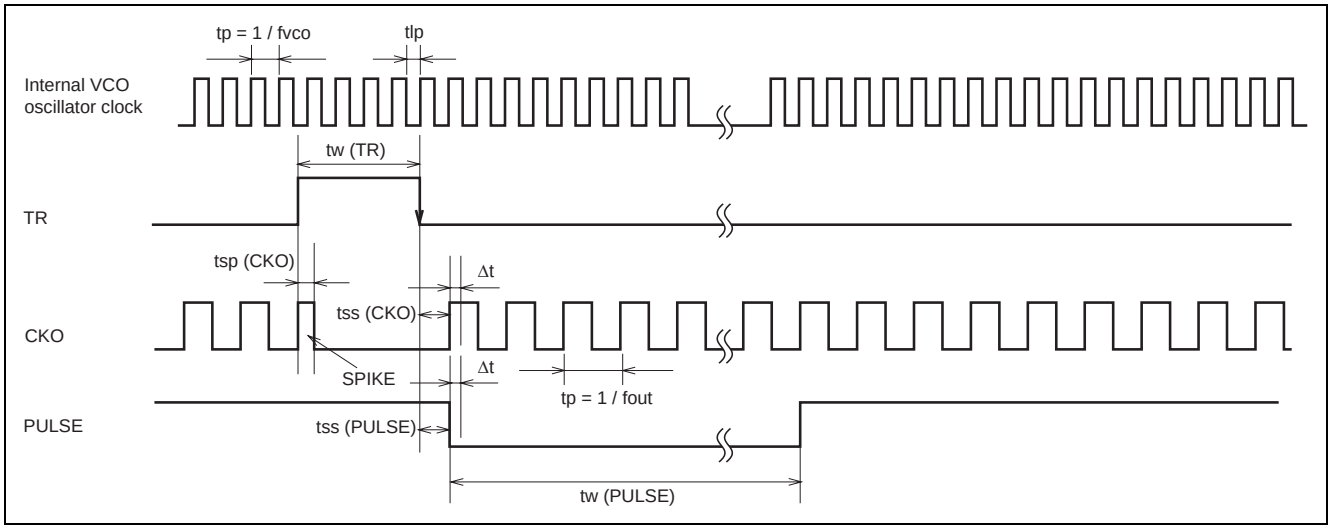
One-shot pulse start timing: 1st leading edge of CKO after TR fall

One-shot pulse polarity: Negative pulse

One-shot pulse width: 16 cycles of CKO

CKO output dividing ratio: 1/2 division

An example set for the condition of address (A1, A0) = (1, 0), data (D6, D5, D4, D3, D2, D1, D0) = (0, 1, 1, 0, 0, 0, 0) is shown below. CKO is a clock output synchronized by TR and PULSE is a one-shot pulse synchronized with the rise of CKO.



1.2 Setting of Trigger Edge when D1 = 1

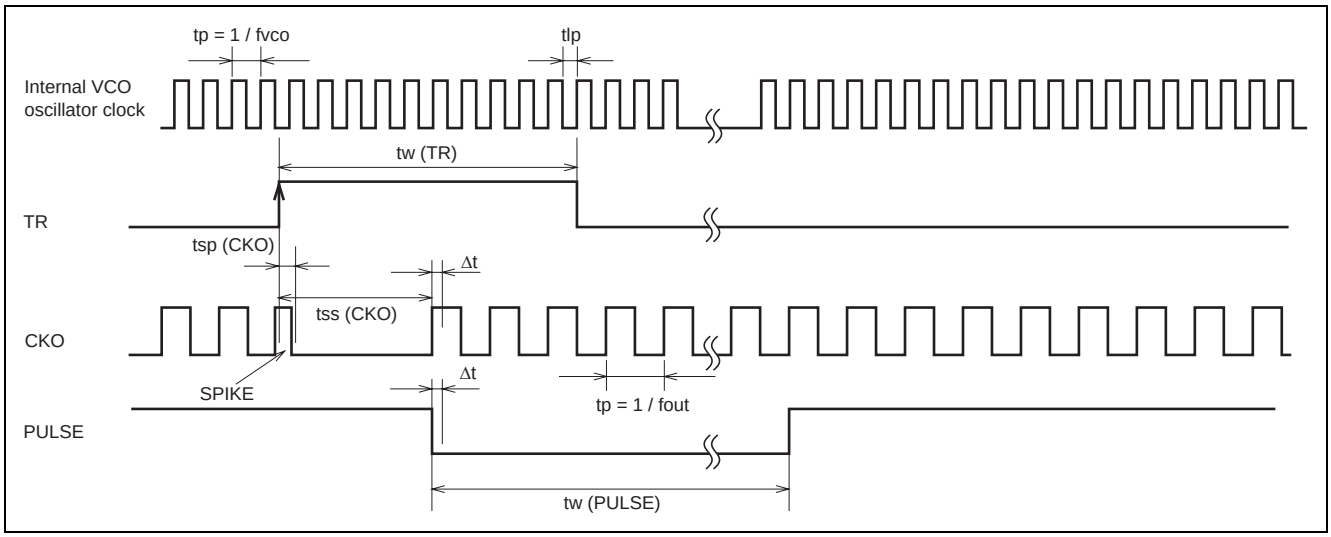
One-shot pulse start timing: 1st leading edge of CKO after TR rise
(except the rise of a spike which occurs when CKO is stopped).

One-shot pulse polarity: Negative pulse

One-shot pulse width: 16 cycles of CKO

CKO output dividing ratio: 1/2 division

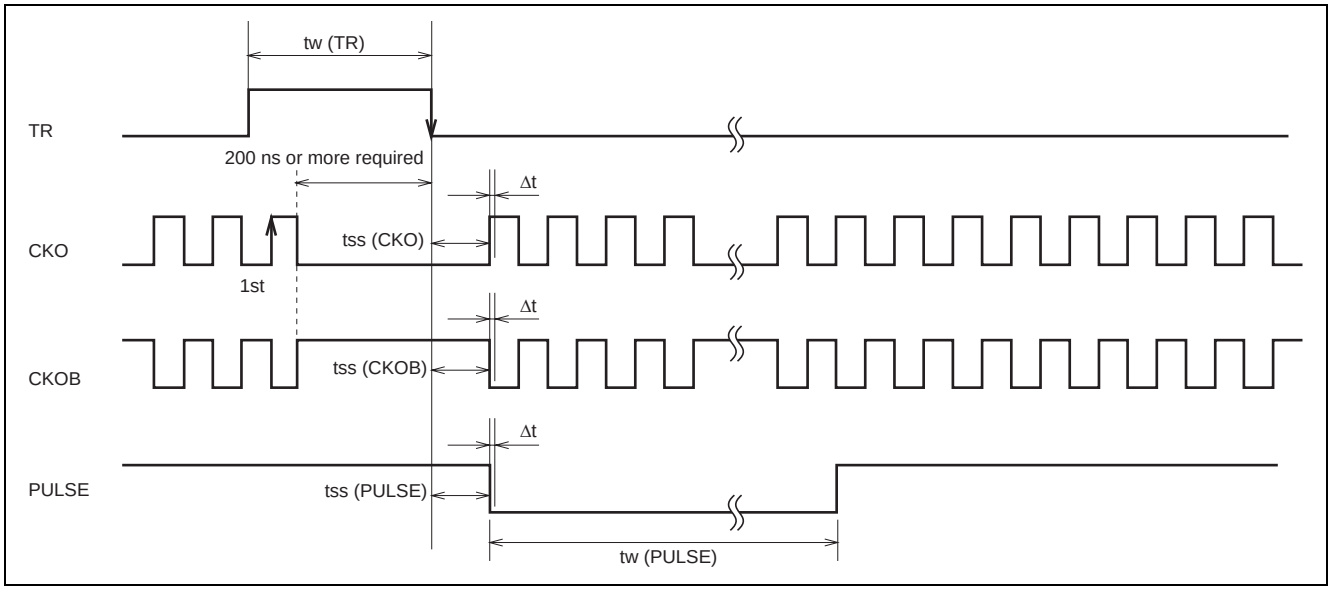
An example set for the condition of address (A1, A0) = (1, 0), data (D6, D5, D4, D3, D2, D1, D0) = (0, 1, 1, 0, 0, 1, 0) is shown below. CKO is a clock output synchronized by TR and PULSE is a one-shot pulse synchronized with the rise of CKO.



2. Sync Clock Spike Removal Mode upon Occurrence of Trigger

When address (A1, A0) = (1, 0) and data (D6, D5, D4, D3, D2, D1, D0) = (0, 1, 1, 0, 1, 0, 0), CKO with the first rise after occurrence of a trigger is output and then CKO stops.

However, this mode is not available when D1 = 1 in trigger edge setting. Set a wide TR so that TR sync edge is entered 200 ns or more after CKO stops.



Notes: 1. 200 ns or more required
2. tss (CKO, CKOB, PULSE) is defined by input clock width "L" + α. In addition, the value of α denotes IC internal delay, and the values of α and tss are definite unless temperature, Vcc, etc. are changed, and tss variations at that time is defined as Δt (sync accuracy: jitter).

CKO/PLLO Output Frequency Range

The M66238 requires an internal VCO oscillator frequency of 25 MHz to 50 MHz.

Settings of dividing ratio K of 12-bit divider and dividing ratio N of 15-bit counter are required in order to determine the internal VCO oscillator frequency. The relation between the settings and the internal VCO oscillator frequency is shown below.

Oscillator frequency $f_{VCO} = \frac{fin \times N}{K}$ (MHz)

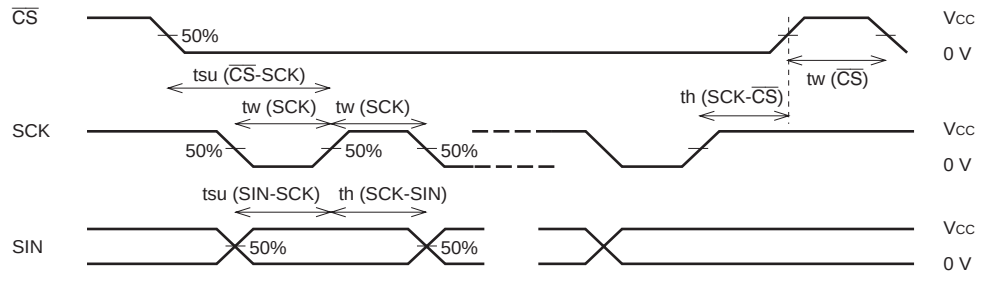
$$K = \sum_{k=0}^{11} (D_k \times 2^k)$$

$$N = \sum_{n=12}^{26} (D_n \times 2^{n-12})$$

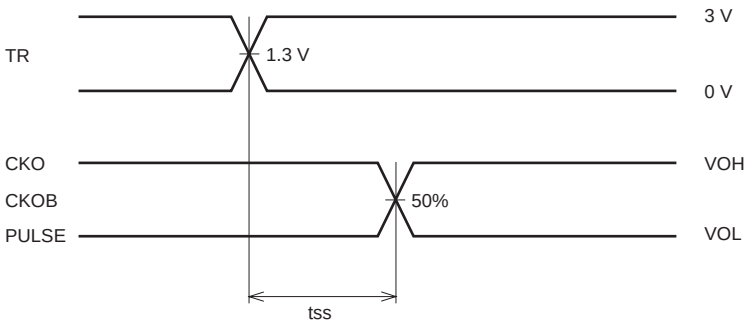
Note: 3. Setting of fin / K ≥ 100 kHz is recommended in consideration of the frequency accuracy characteristics of PLL output.
Therefore, set the division ratio K of the 12-bit divider and the division ratio N of the 15-bit counter to meet the following conditions:
25 MHz ≤ fvco ≤ 50 MHz
In addition, for PLLO and CKO, setting the division ratios of the sync/division circuit (synchronous clock generating area) to 1/1, 1/2, 1/4, 1/8, 1/16, 1/32 will allow the frequencies of 0.78 Hz to 50 MHz to be accommodated.

Input Timing

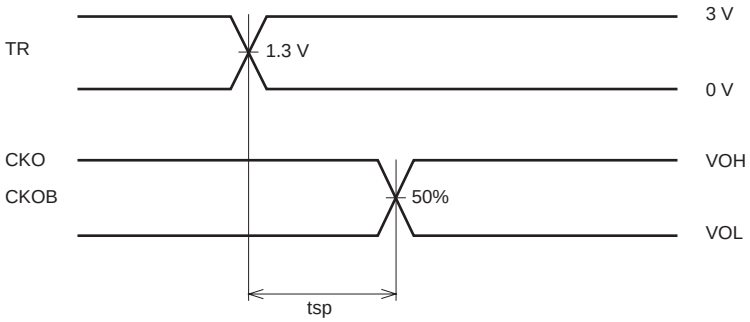
(1) Register Setting



(2) Clock from Trigger Input and One-shot Pulse Output

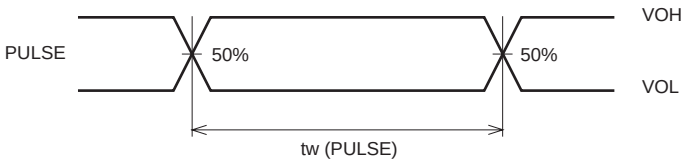


(3) Stop of Clock from Trigger Input

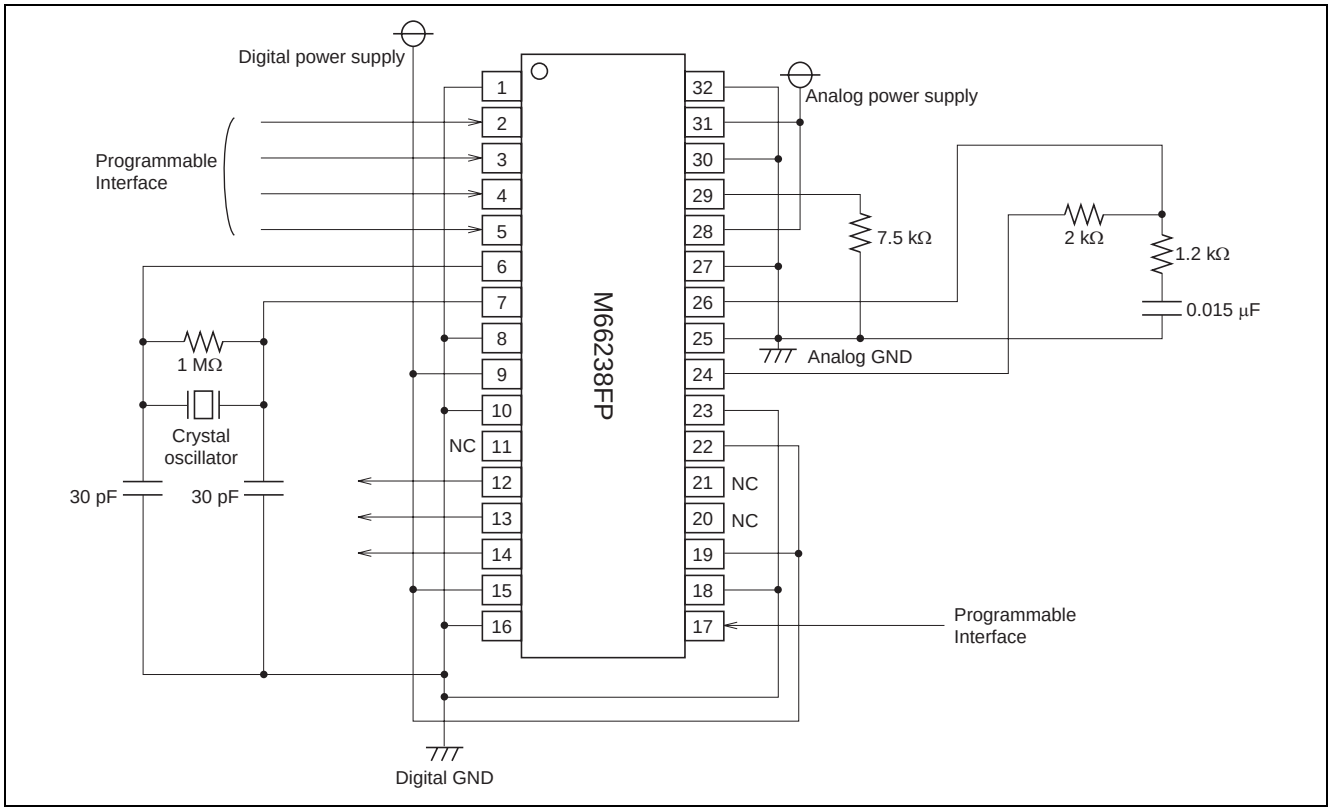


(4) Trigger Input Width

(5) One-shot Pulse Width



Application Circuit Example

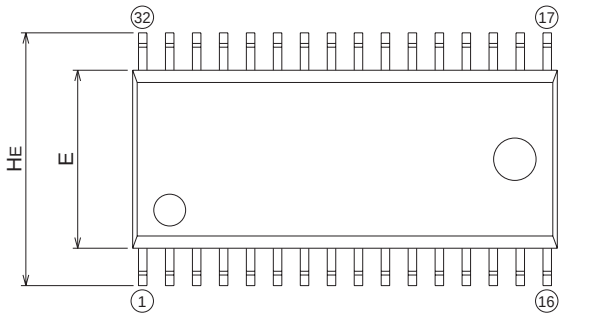


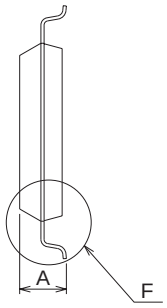
Package Dimensions

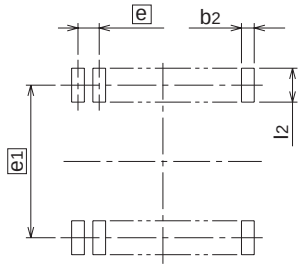
32P2W-A

Plastic 32pin 450mil SOP

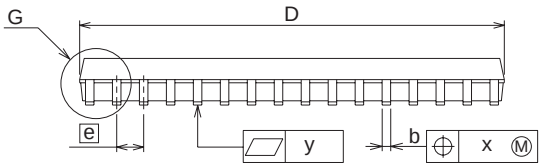
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP32-P-450-1.27	—	0.67	Alloy 42

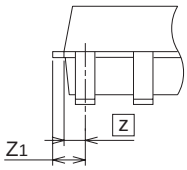




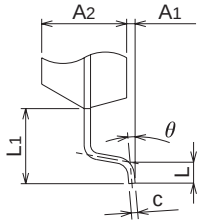


Recommended Mount Pad





Detail G



Detail F

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A_1	0.05	—	—
A_2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	19.8	20.0	20.2
E	8.2	8.4	8.6
e	—	1.27	—
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	—	1.765	—
z	—	0.475	—
Z_1	—	—	0.625
x	—	—	0.25
y	—	—	0.15
θ	0°	—	10°
b_2	—	0.76	—
e1	—	11.43	—
l_2	1.27	—	—

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Colophon .7.2