

M66238FP

Standard Clock Generator with PLL Frequency Synthesizer

REJ03F0268-0200

Rev.2.00

Mar 18, 2008

Description

The M66238 is a LSI that incorporates a PLL synthesizer and a sync clock generator in it. The PLL synthesizer covers the range of 25 MHz to 50 MHz at the minimum steps of 3 kHz.

The sync circuit outputs a clock and a one-shot pulse which are synchronized with an external trigger signal. Setting a dividing ratio allows acquisition of sync clock outputs within the range of 0.78 MHz to 25 MHz.

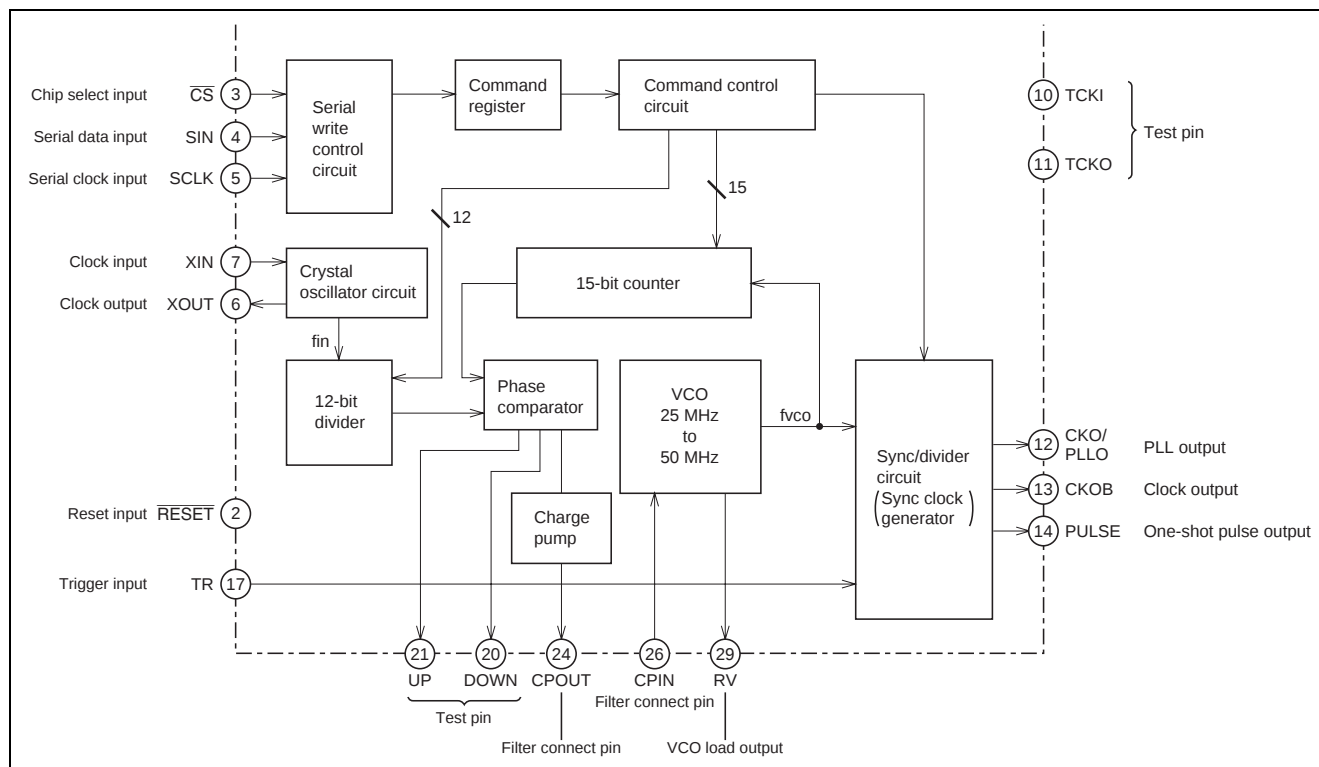
Features

- Sync clock output frequency range: 1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of 25 to 50 MHz
- Sync accuracy (jitter): ± 3 ns
- Trigger input: Polarity selectable
- One-shot pulse output: Polarity and width selectable
- 5 V power supply

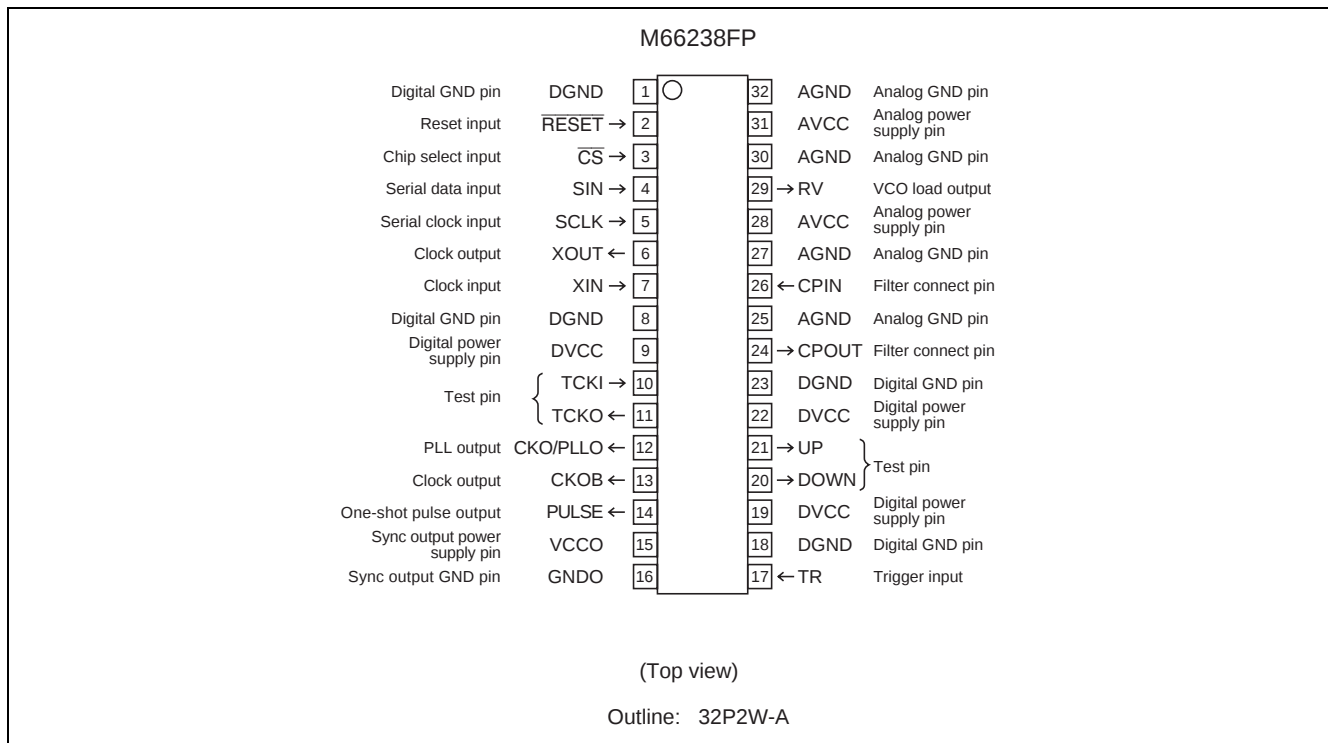
Application

Pixel clock generator

Block Diagram



Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{cc}	−0.5 to +7.0	V
Input voltage	V _i	−0.5 to V _{cc} + 0.5	V
Output voltage	V _o	−0.5 to V _{cc} + 0.5	V
Power dissipation* ¹	P _d	650	mW
Storage temperature	T _{stg}	−65 to +150	°C

Note: 1. When board is mounted

All voltages adopt the GND pin of the circuit as the base (0 V) and absolute values are displayed for maximum and minimum values.

Recommended Operating Conditions

(T_a = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{cc}	4.75	5	5.25	V
Supply voltage	GND	—	0	—	V
Input voltage	V _i	0	—	V _{cc}	V
Output voltage	V _o	0	—	V _{cc}	V
Operating ambient temperature	T _{opr}	0	—	70	°C

Note: The direction of current flowing into a circuit is defined to be positive (no sign) and the direction of current flowing out is defined to be negative (−sign).

Absolute values are displayed for maximum and minimum values.

Electrical Characteristics

(T_a = 0 to 70°C, V_{cc} = 5 V ± 5%, GND = 0 V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
High-level input voltage	V _{IH}	2	—	—	V	TR
Low-level input voltage	V _{IL}	—	—	0.8	V	
High-level input voltage	V _{IH}	0.8 × V _{cc}	—	—	V	XIN
Low-level input voltage	V _{IL}	—	—	0.2 × V _{cc}	V	
High-level output voltage	V _{OH}	V _{cc} − 0.8	—	—	V	GND = 0 V, I _{OH} = −4 mA
Low-level output voltage	V _{OL}	—	—	0.55	V	GND = 0 V, I _{OL} = 4 mA
Supply current (at time of standstill)	I _{cc} (s)	—	—	50	μA	GND = 0 V, V _I = V _{cc} or GND
Supply current (at time of operation)	I _{cc} (a)	—	—	120	mA	GND = 0 V, CKO = 50 MHz V _I = V _{cc} or GND
High-level input current	I _{IH}	—	—	10	μA	GND = 0 V, V _I = V _{cc}
Low-level input current	I _{IL}	—	—	−10	μA	GND = 0 V, V _I = 0 V
Input capacitance	C _I	—	—	10	pF	

Note: Measurement circuit; The direction of current flowing to the circuit is specified to be positive (no sign).

Timing Requirements

(Ta = 0 to 70°C, Vcc = 5 V ± 5%, GND = 0 V)

Item	Symbol	Min	Typ	Max	Unit
CS width	tw ($\overline{\text{CS}}$)	1	—	—	μs
CS set up time	tsu ($\overline{\text{CS}}$ -SCK)	50	—	—	ns
CS hold time	th (SCK- $\overline{\text{CS}}$)	50	—	—	ns
SCK width	tw (SCK)	25	—	—	ns
SIN set up time	tsu (SIN-SCK)	25	—	—	ns
SIN hold time	th (SCK-SIN)	25	—	—	ns
Clock input frequency	f _{in}	7	—	12	MHz
Clock input duty	f _i DUTY	40	—	60	%
Trigger input "H" pulse width	tw (TR)	200	—	—	ns
Clock input rising time	tr	—	—	5	ns
Clock input falling time	tf	—	—	5	ns

Switching Characteristics

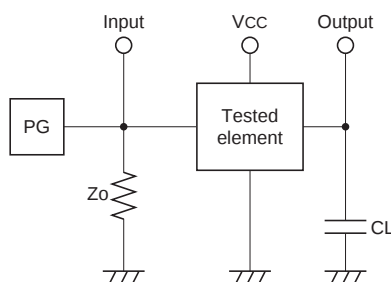
(Ta = 0 to 70°C, Vcc = 5 V ± 5%, GND = 0 V, CL = 15 pF)

Item	Symbol	Min	Typ	Max	Unit
VCO oscillation frequency	f _{vco}	25	—	50	MHz
Synchronous output frequency	f _{out}	—	—	50	MHz
Synchronous accuracy (jitter)	Δt	—	—	±3	ns
Synchronous clock output start	tss (CKO)	—	—	t _{lp} + 200	ns
Synchronous clock reversible output start	tss (CKOB)	—	—	t _{lp} + 200	ns
One-shot pulse output start	tss (PULSE)	—	—	t _{lp} + 200	ns
Synchronous clock output stop	tsp (CKO)	—	—	40	ns
Synchronous clock reversible output stop	tsp (CKOB)	—	—	40	ns
One-shot pulse output width	tw (PULSE)	n • t _p – 10	—	n • t _p + 10	ns
Synchronous clock output duty	f _o DUTY (CKO)	40	—	60	%
Synchronous clock reversible output duty	f _o DUT (CKOB)	40	—	60	%

Note: t_p = 1 / f_{out}, t_{lp} = t_p × (100 – f_{vco}duty) / 100

The n value of one-shot pulse output width is set in the register.

Measurement Circuit



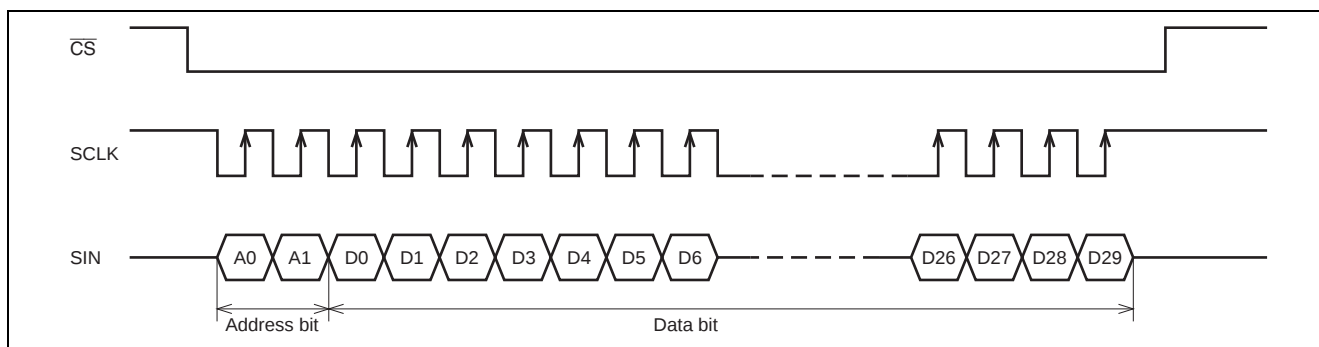
Notes:

- Waveform for switching test
 - Input pulse level XIN: 0 to Vcc, TR: 0 to 3 V
 - Input pulse rising time: 3 ns
 - Input pulse falling time: 3 ns
 - Zo: 50 Ω
 - Decision voltage Input voltage XIN: Vcc/2, Tr: 1.3 V
 - Output voltage All outputs: Vcc/2
- Electrostatic capacitance: CL includes floating capacitance of connection and probe input capacitance.

List of Register Setting Commands

A1	A0	Setting
0	0	Setting of CKO/PLLO dividing ratio, PLL synthesizer 15-bit generation dividing ratio and reference clock generation 12-bit dividing ratio.
1	0	Setting of one-shot pulse polarity and width, setting of trigger edge, HALT of entire M66238, HALT of charge pump and VCO, phase comparator output UP/DOWN, CKO/PLLO switching.
1	1	Dummy trigger generation command

Serial Data Write Timing



Register Configuration

1. Clock frequency setting command

Reference clock generation 12-bit division ratio, PLL synthesizer 15-bit division ratio and CKO/PLLO division ratio are set at address (A1, A0) = (0, 0).

Data Bit		Description	Default
D0	0	12-bit reference clock dividing ratio is set. D11 and D0 correspond to MSB and LSB, respectively.	0
	1		
D1	0	$K = \sum_{k=0}^{11} (Dk \times 2^k)$ K: Reference clock dividing ratio	1
	1		
D2	0		0
	1		
D3	0		1
	1		
D4	0		0
	1		
D5	0		0
	1		
D6	0		0
	1		
D7	0		0
	1		
D8	0		1
	1		
D9	0		0
	1		
D10	0		0
	1		
D11	0		0
	1		
D12	0	15-bit PLL synthesizer dividing ratio is set. D26 and D12 correspond to MSB and LSB, respectively.	0
	1		
D13	0	$N = \sum_{n=12}^{26} (Dn \times 2^{n-12})$ N: PLL synthesizer dividing ratio	0
	1		
D14	0		0
	1		
D15	0		1
	1		
D16	0		0
	1		
D17	0		1
	1		
D18	0		1
	1		
D19	0		1
	1		
D20	0		1
	1		
D21	0		1
	1		
D22	0		0
	1		
D23	0		0
	1		
D24	0		0
	1		
D25	0		0
	1		
D26	0		0
	1		

Data Bit		Description					Default
D27	0	Setting of CKO/PLLO dividing ratios					0
	1						
D28	0	Dividing Ratio	D29	D28	D27	PLLO/CKO Oscillator Frequency	1
		1/1	0	0	0	25 MHz to 50 MHz	
	1	1/2	0	0	1	12.5 MHz to 25 MHz	
		1/4	0	1	0	6.25 MHz to 12.5 MHz	
D29	0	1/8	0	1	1	3.125 MHz to 6.25 MHz	0
		1/16	1	0	0	1.563 MHz to 3.125 MHz	
	1	1/32	1	0	1	0.781 MHz to 1.563 MHz	

2. Operating mode setting commands

Address (A1, A0) = (1, 0) allows setting of one-shot pulse polarity and width, trigger edge, M66238 entire halt, charge pump and VCO halt, phase comparator UP/DOWN output, LPF cutoff, CKO/PLLO switching, VCO switching and charge pump switching.

Data Bit		Description	Default													
D0	0	Setting of trigger edge	0													
	1	<table><tr><th>D1</th><th>D0</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>Synchronizes with TR CKO is stopped when TR = "H"</td></tr><tr><td>0</td><td>1</td><td>Synchronizes with TR CKO is stopped when TR = "L"</td></tr><tr><td>1</td><td>0</td><td>Synchronizes with TR CKO is output when TR = "H"</td></tr><tr><td>1</td><td>1</td><td>Synchronizes with TR CKO is output when TR = "L"</td></tr></table>		D1	D0	Description	0	0	Synchronizes with TR CKO is stopped when TR = "H"	0	1	Synchronizes with TR CKO is stopped when TR = "L"	1	0	Synchronizes with TR CKO is output when TR = "H"	1
D1	D0	Description														
0	0	Synchronizes with TR CKO is stopped when TR = "H"														
0	1	Synchronizes with TR CKO is stopped when TR = "L"														
1	0	Synchronizes with TR CKO is output when TR = "H"														
1	1	Synchronizes with TR CKO is output when TR = "L"														
D1	0		0													
	1															
D2	0	When trigger occurs: spike of sync clock is not eliminated.	0													
	1	When trigger occurs: spike of sync clock is eliminated (disabled when D1 = 1).														
D3	0	Polarity of one-shot pulse: Negative pulse	0													
	1	Polarity of one-shot pulse: Positive pulse														
D4	0	Setting of one-shot pulse width	0													
	1	<table><tr><th>D5</th><th>D4</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>CKO 2-cycle width</td></tr><tr><td>0</td><td>1</td><td>CKO 4-cycle width</td></tr><tr><td>1</td><td>0</td><td>CKO 8-cycle width</td></tr><tr><td>1</td><td>1</td><td>CKO 16-cycle width</td></tr></table>		D5	D4	Description	0	0	CKO 2-cycle width	0	1	CKO 4-cycle width	1	0	CKO 8-cycle width	1
D5	D4	Description														
0	0	CKO 2-cycle width														
0	1	CKO 4-cycle width														
1	0	CKO 8-cycle width														
1	1	CKO 16-cycle width														
D5	0		0													
	1															
D6	0	CKO/PLLO pin: CKO output	0													
	1	CKO/PLLO pin: PLLO output														
D7	0	Entire M66238: Operating state	0													
	1	Entire M66238: Halt state														
D8	0	VCO: Operating state	0													
	1	VCO: Halt state														
D9	0	Charge pump: ON	0													
	1	Charge pump: OFF														
D10	0	Low pass filter: Operating state	0													
	1	Low pass filter: Separated														
D11	0	Normal use: Not output to outside	0													
	1	Phase comparator UP/DOWN output enable														
D12	0	Normal use	0													
	1	VCO test circuit set														
D13	0	Normal use	0													
	1	Charge pump test circuit set														
D14	0	Normal use	0													
	1	15-bit counter test clock enable														
D15	0	Normal use	0													
	1	Sync clock generator test clock enable														
D16	0	Normal use	0													
	1	Sync clock generator test input enable														
D17	0	Normal use	0													
	1	12-bit counter test output enable														
D18	0	Normal use	0													
	1	15-bit counter test output enable														
D19	0	Normal use	0													
	1	Sync clock generator trigger test output enable														
D20	0	Normal use	0													
	1	Sync clock generator test output enable														
D21 : D29		In normal use: "0" set	0 : 0													

3. Dummy trigger generating command

The internal status of sync clock generator becomes unstable and a stable sync clock output (CKO) is not obtained after the power is turned on, after a reset is cleared or after an internal VCO oscillator frequency is set. To obtain a stable sync clock output, enter a trigger signal from the TR input after VCO oscillator becomes stable, or enter a dummy trigger generating command from the MCU. The PLL synthesizer oscillator frequency after the cancellation of a reset depends on a default (See the register configuration).

Set the command for address (A1, A0) = (1, 1).

Data Bit		Description	Default
D0	0	The command must be stored two times continuously when a dummy trigger is generated. For the first time, set the dummy trigger generating command with D0 = 1. For the second time, set the dummy trigger generating command with D0 = 0. The second setting becomes a sync edge and a clock begins to be output from CKO. After the first setting, CKO is in the halt state.	0
	1		
D1	0	In normal use: "0"	0
	1		
↓			
D29	0		
	1		0

Operating Timing

1. Sync Clock Spike Non-removal Mode upon Occurrence of Trigger

1.1 Setting of Trigger Edge when D1 = 0

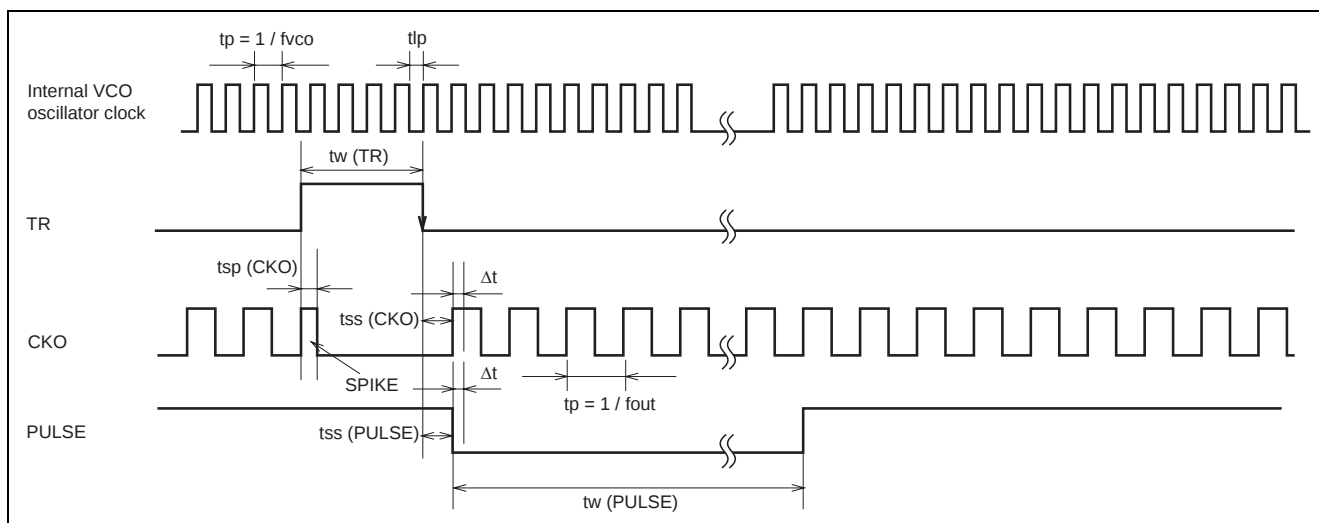
One-shot pulse start timing: 1st leading edge of CKO after TR fall

One-shot pulse polarity: Negative pulse

One-shot pulse width: 16 cycles of CKO

CKO output dividing ratio: 1/2 division

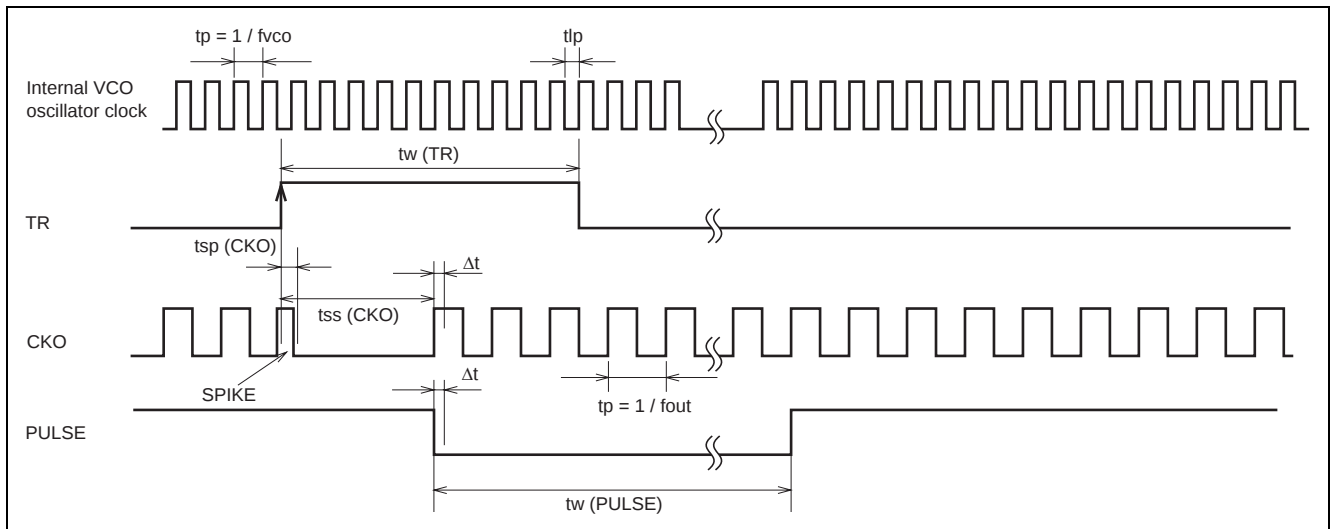
An example set for the condition of address (A1, A0) = (1, 0), data (D6, D5, D4, D3, D2, D1, D0) = (0, 1, 1, 0, 0, 0, 0) is shown below. CKO is a clock output synchronized by TR and PULSE is a one-shot pulse synchronized with the rise of CKO.



1.2 Setting of Trigger Edge when D1 = 1

One-shot pulse start timing:	1st leading edge of CKO after TR rise (except the rise of a spike which occurs when CKO is stopped).
One-shot pulse polarity:	Negative pulse
One-shot pulse width:	16 cycles of CKO
CKO output dividing ratio:	1/2 division

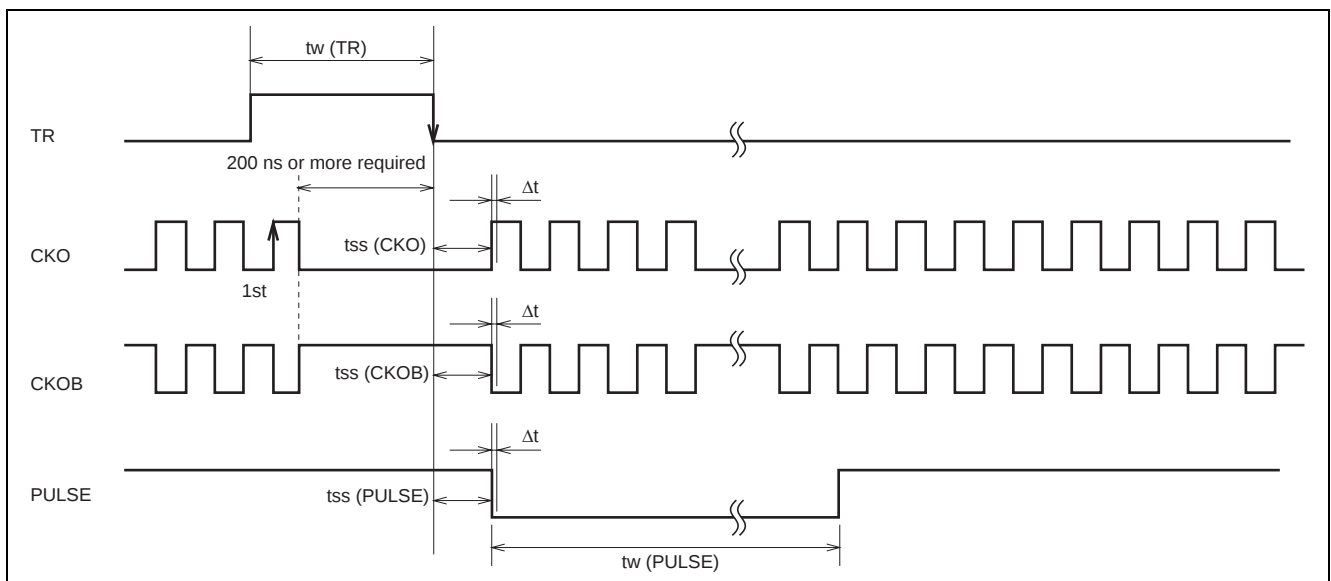
An example set for the condition of address (A1, A0) = (1, 0), data (D6, D5, D4, D3, D2, D1, D0) = (0, 1, 1, 0, 0, 1, 0) is shown below. CKO is a clock output synchronized by TR and PULSE is a one-shot pulse synchronized with the rise of CKO.



2. Sync Clock Spike Removal Mode upon Occurrence of Trigger

When address (A1, A0) = (1, 0) and data (D6, D5, D4, D3, D2, D1, D0) = (0, 1, 1, 0, 1, 0, 0), CKO with the first rise after occurrence of a trigger is output and then CKO stops.

However, this mode is not available when D1 = 1 in trigger edge setting. Set a wide TR so that TR sync edge is entered 200 ns or more after CKO stops.



- Notes:
- 200 ns or more required
 - tss (CKO, CKOB, PULSE) is defined by input clock width "L" + α . In addition, the value of α denotes IC internal delay, and the values of α and tss are definite unless temperature, Vcc, etc. are changed, and tss variations at that time is defined as Δt (sync accuracy: jitter).

CKO/PLLO Output Frequency Range

The M66238 requires an internal VCO oscillator frequency of 25 MHz to 50 MHz.

Settings of dividing ratio K of 12-bit divider and dividing ratio N of 15-bit counter are required in order to determine the internal VCO oscillator frequency. The relation between the settings and the internal VCO oscillator frequency is shown below.

$$\text{Oscillator frequency} \quad f_{\text{VCO}} = \frac{f_{\text{in}} \times N}{K} \text{ (MHz)}$$

$$K = \sum_{k=0}^{11} (D_k \times 2^k)$$

$$N = \sum_{n=12}^{26} (D_n \times 2^{n-12})$$

Note: 3. Setting of $f_{\text{in}} / K \geq 100 \text{ kHz}$ is recommended in consideration of the frequency accuracy characteristics of PLL output.

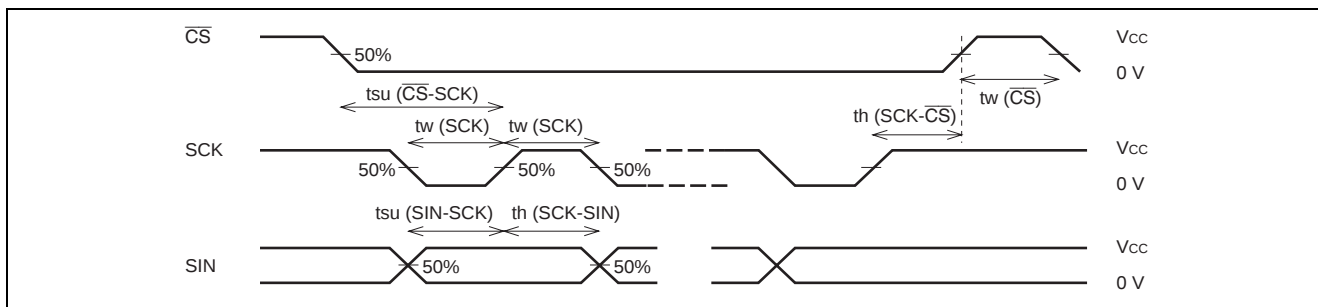
Therefore, set the division ratio K of the 12-bit divider and the division ratio N of the 15-bit counter to meet the following conditions:

$$25 \text{ MHz} \leq f_{\text{VCO}} \leq 50 \text{ MHz}$$

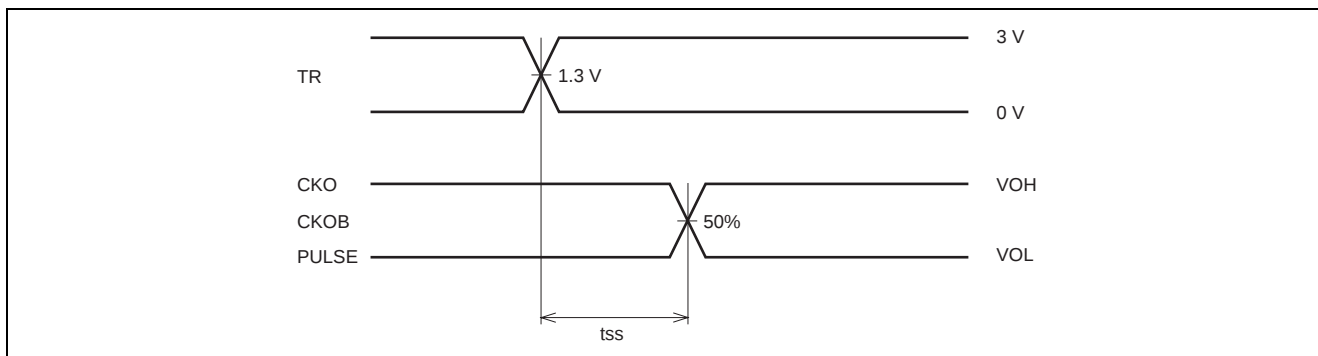
In addition, for PLLO and CKO, setting the division ratios of the sync/division circuit (synchronous clock generating area) to 1/1, 1/2, 1/4, 1/8, 1/16, 1/32 will allow the frequencies of 0.78 Hz to 50 MHz to be accommodated.

Input Timing

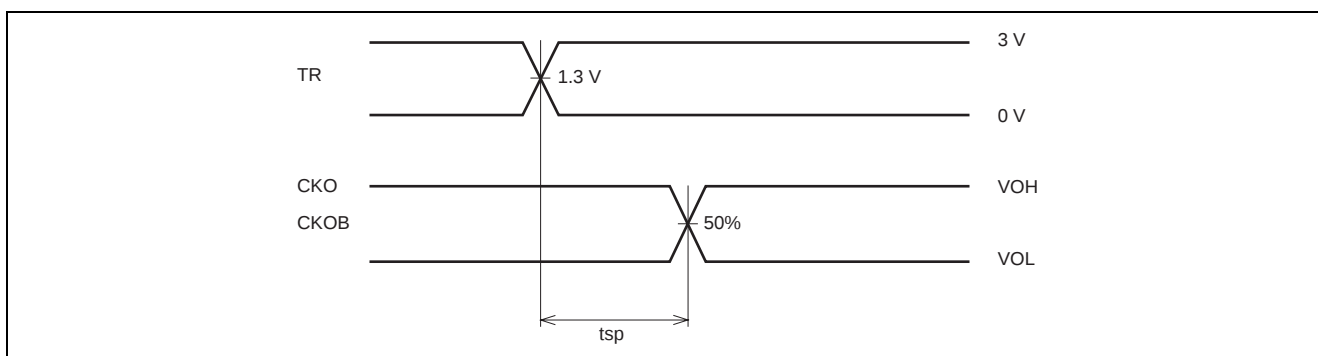
(1) Register Setting



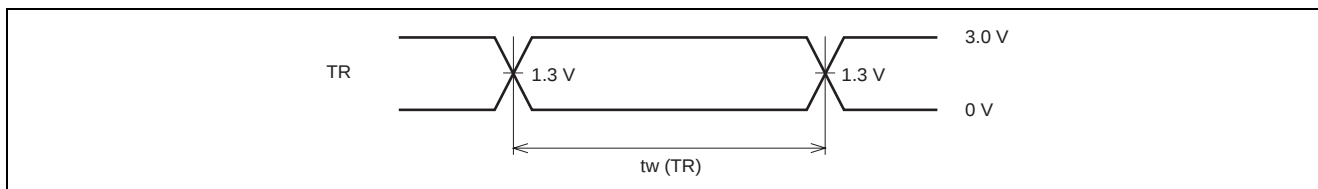
(2) Clock from Trigger Input and One-shot Pulse Output



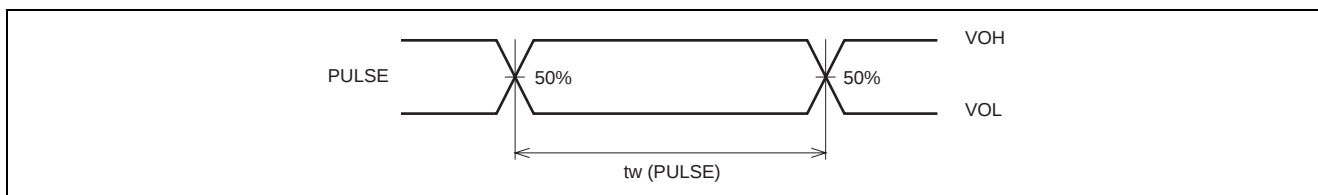
(3) Stop of Clock from Trigger Input



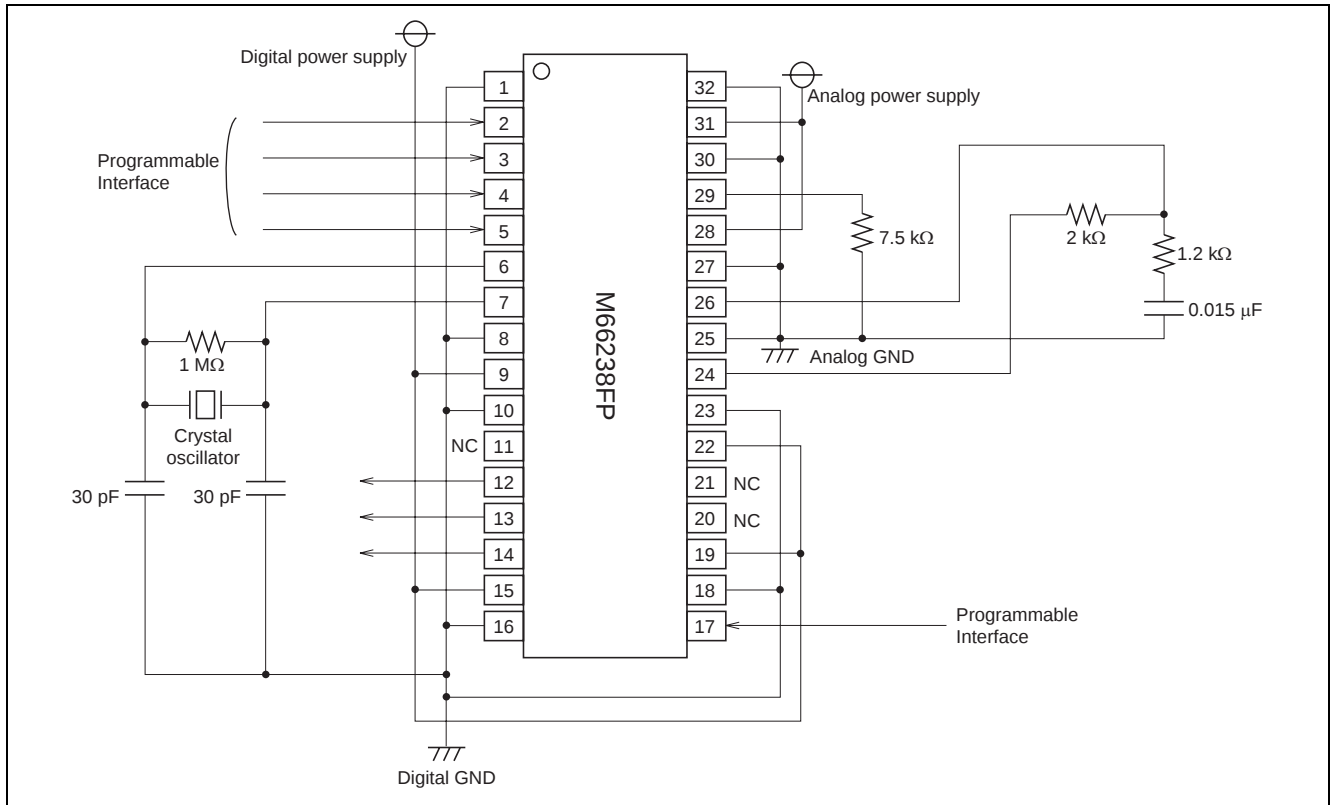
(4) Trigger Input Width



(5) One-shot Pulse Width



Application Circuit Example

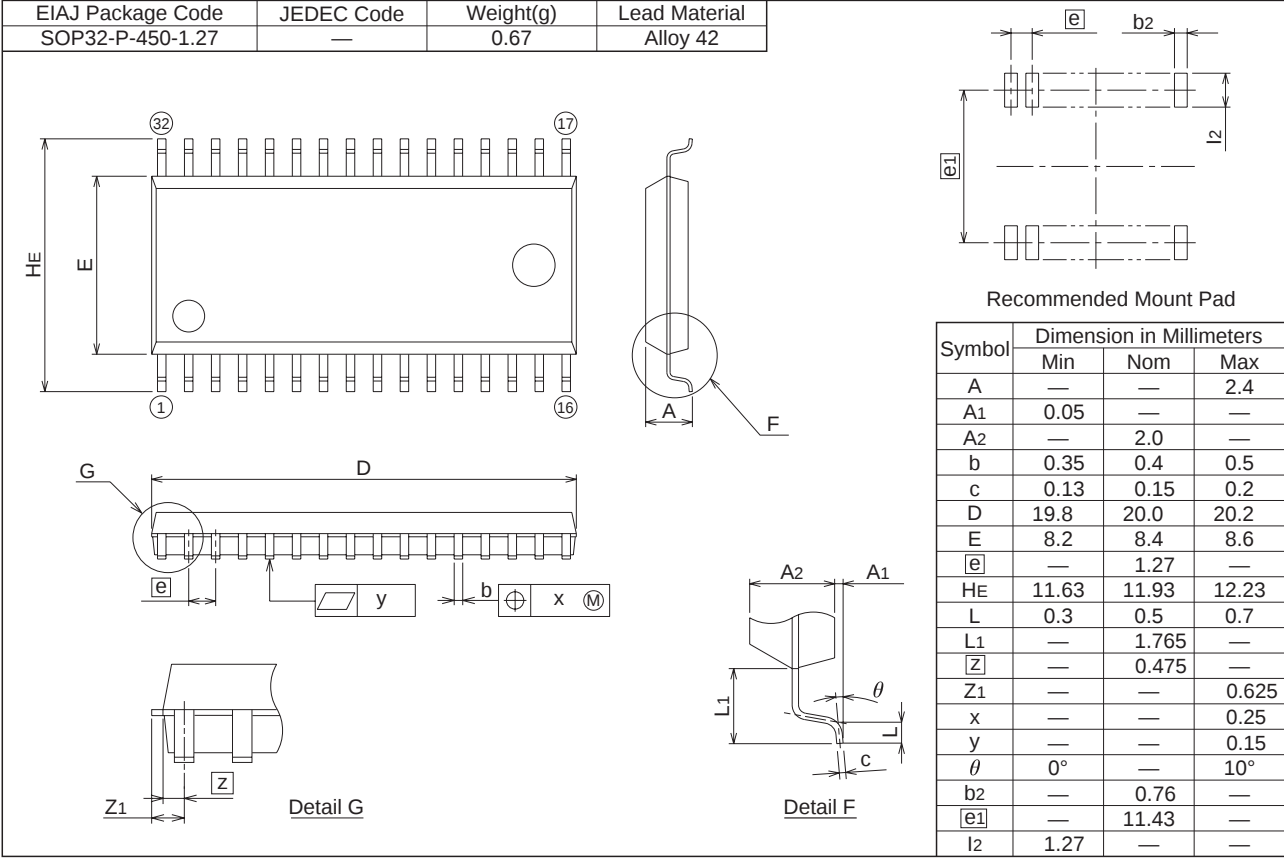


Package Dimensions

32P2W-A

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP32-P-450-1.27	—	0.67	Alloy 42

Plastic 32pin 450mil SOP



Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
 - (1) artificial life support devices or systems
 - (2) surgical implantations
 - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
 - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510