DS2227
Flexible NV SRAM Stik

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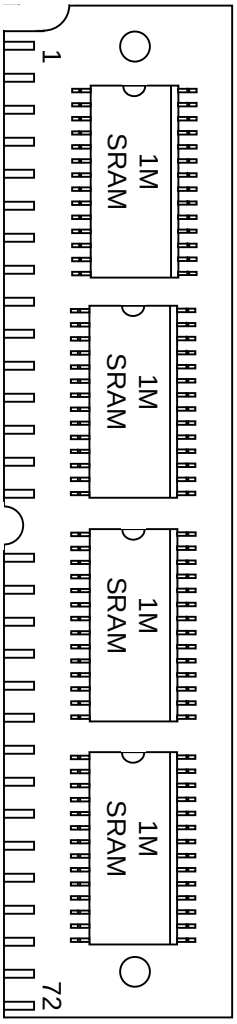
FEATURES

- Flexibly organized as 128k x 32, 256k x 16, or 512k x 8 bits
- Data retention >10 years in the absence of V_{CC}
- Nonvolatile circuitry transparent to and independent from host system
- Automatic write protection circuitry safeguards against data loss
- Separate chip enables allow access by byte, word, or long word
- Fast access times: 70 ns, 100 ns, or 120 ns
- Unlimited write cycles
- Read cycle time equals write cycle time
- Employs popular JEDEC standard 72-position SIMM connection scheme
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time

PIN ASSIGNMENT



72-Pin SIP STIK

DESCRIPTION

The DS2227 Flexible NV SRAM Stik is a self-contained 4,194,304-bit nonvolatile static RAM which can be flexibly organized as 128k x 32 bits, 256k x 16 bits, or 512k x 8 bits. The nonvolatile memory contains all necessary control circuitry and lithium energy sources to maintain data integrity in the absence of power for more than 10 years. The DS2227 employs the popular JEDEC standard 72-position SIMM connection scheme requiring no additional circuitry.

OPERATION

The DS2227 Flexible NV SRAM Stik is used like any standard static RAM. All nonvolatile circuitry is transparent to the user. The flexibility of the part is achieved by providing separate read, write, and chip

select pins for each of the four banks of onboard memories (see Figure 1). For operation as a 512k x 8 NV SRAM Stik, tie all data lines from each bank together (i.e., all D0s together, all D1s together, etc.). Read enables and write enables are also tied together. For operation as a 256k x 16 NV SRAM Stik, tie the data lines from two banks together. Chip enables, read enables, and write enables from these banks are also tied together. Connection to the DS2227 is made by using an industry-standard, 72-position SIMM socket DS9072-72V (AMP part number 821824-8). These SIMM sockets are also available in perpendicular, inclined, or parallel mount, depending on the height available. See the DS907x SipStik™ connectors available from Dallas Semiconductor.

READ MODE

The DS2227 executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 17 address inputs (A_0 - A_{16}) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS2227 is in the write mode whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs to t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS2227 provides fully functional capability for V_{CC} greater than 4.5 volts and guarantees write protection for V_{CC} less than 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS2227 constantly monitors V_{CC}. Should the supply voltage decay, the NV SRAM automatically write-protects itself, all inputs become “don’t care” and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, a power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects the external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

The DS2227 checks lithium status to warn of potential data loss. Each time that V_{CC} power is restored to the DS2227, the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0 volts, the second memory access to the device is inhibited. Battery status can, therefore, be determined by a three-step process. First, a read cycle is performed to any location in memory, in order to save the contents of that location. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, then the battery voltage is less than 2.0V and data is in danger of being corrupted.

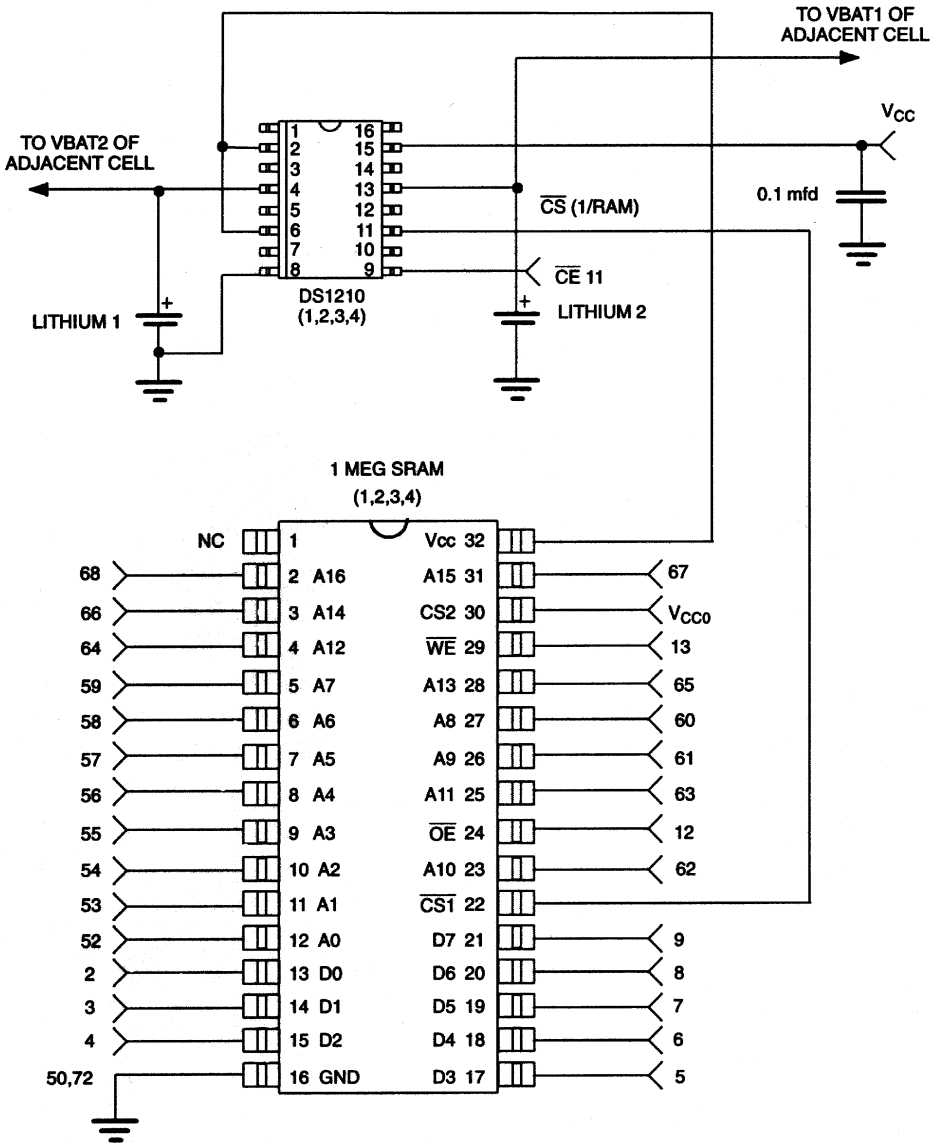
The DS2227 also provides battery redundancy. In many applications data integrity is paramount. The DS2227 provides two batteries for each SRAM and an internal isolation switch to select between them. During battery backup, the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user.

PIN DESCRIPTION Table 1

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	V_{CC}	38	4-D0
2	1-D0	39	4-D1
3	1-D1	40	4-D2
4	1-D2	41	4-D3
5	1-D3	42	4-D4
6	1-D4	43	4-D5
7	1-D5	44	4-D6
8	1-D6	45	4-D7
9	1-D7	46	NC
10	NC	47	4-$\overline{CE}$
11	1-$\overline{CE}$	48	4-$\overline{OE}$
12	1-$\overline{OE}$	49	4-$\overline{WE}$
13	1-$\overline{WE}$	50	GND
14	2-D0	51	V_{CC}
15	2-D1	52	A0
16	2-D2	53	A1
17	2-D3	54	A2
18	2-D4	55	A3
19	2-D5	56	A4
20	2-D6	57	A5
21	2-D7	58	A6
22	NC	59	A7
23	2-$\overline{CE}$	60	A8
24	2-$\overline{OE}$	61	A9
25	2-$\overline{WE}$	62	A10
26	3-D0	63	A11
27	3-D1	64	A12
28	3-D2	65	A13
29	3-D3	66	A14
30	3-D4	67	A15
31	3-D5	68	A16
32	3-D6	69	NC
33	3-D7	70	NC
34	NC	71	NC
35	3-$\overline{CE}$	72	GND
36	3-$\overline{OE}$		
37	3-$\overline{WE}$		

NOTE: Leave all pins marked as NC unconnected.

SCHEMATIC (1 CELL) Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40° to +85°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current	I_{LO}	-5.0		+5.0	µA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0	3.0		mA	
Operating Current	I_{CC}		60	280	mA	
Write Protection Voltage	V_{TP}	4.25	4.37	4.5	V	

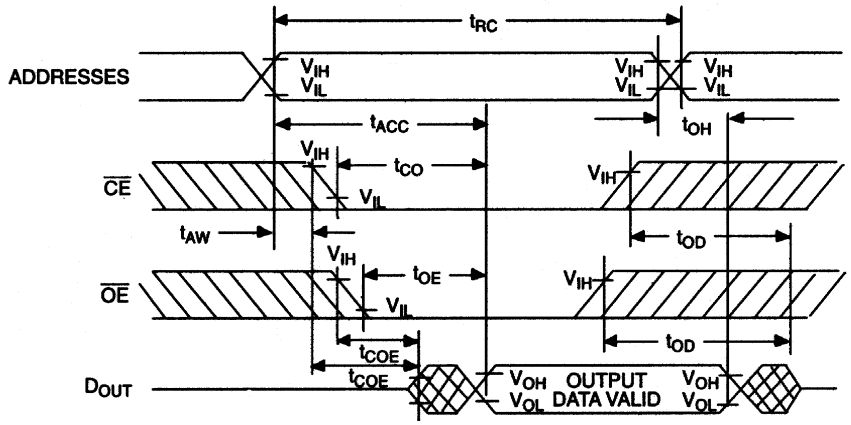
CAPACITANCE (T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20	40	pF	
Output Capacitance	C_{OUT}		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

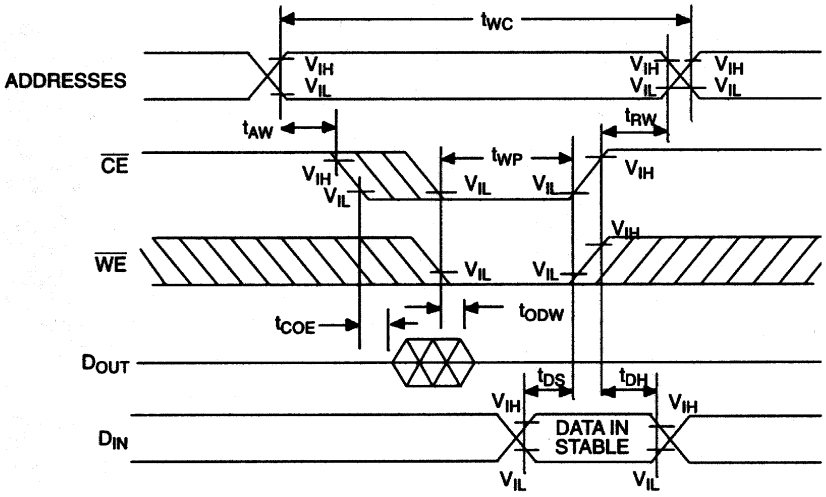
PARAMETER	SYMBOL	DS2227-70		DS2227-100		DS2227-120		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		120		ns	10
Access Time	t_{ACC}		70		100		120	ns	10
$\overline{OE}$ to Output Valid	t_{OE}		35		50		60	ns	10
$\overline{CE}$ to Output Valid	t_{CO}		70		100		120	ns	10
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		5		ns	10
Output High Z from Deselection	t_{OD}		25		35		40	ns	10
Output Hold from Address Change	t_{OH}	5		5		5		ns	10
Write Cycle Time	t_{WC}	70		100		120		ns	10
Write Pulse Width	t_{WP}	55		75		90		ns	3,10
Address Setup Time	t_{AW}	0		0		0		ns	10
Write Recovery Time	t_{WR}	20		20		20		ns	10
Output High Z from $\overline{WE}$	t_{ODW}		25		35		40	ns	10
Output Active from $\overline{WE}$	t_{OEW}	5		5		5		ns	8,10
Data Setup Time	t_{DS}	30		40		50		ns	4,10
Data Hold Time from $\overline{WE}$	t_{DH}	20		20		20		ns	4,5,10

READ CYCLE



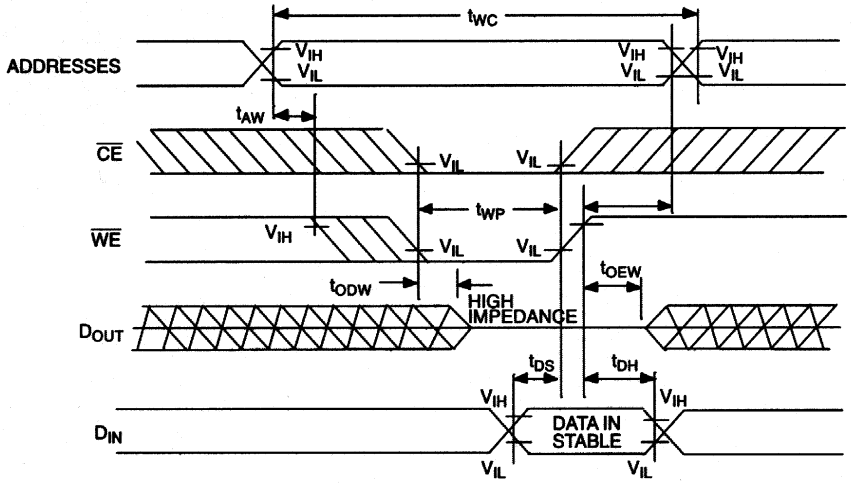
SEE NOTE 1

WRITE CYCLE 1



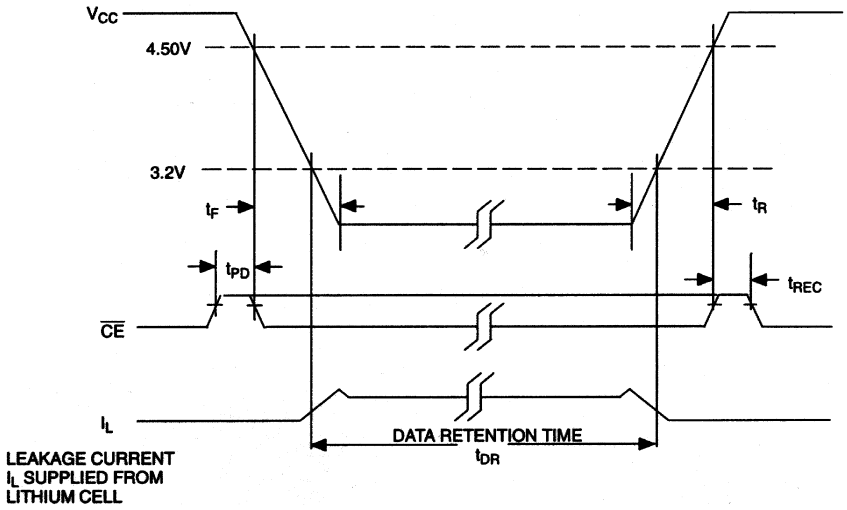
SEE NOTES 2, 3, 4, 5, 6, 7 AND 8

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 5, 6, 7 AND 8

POWER-UP/POWER-DOWN CONDITION



POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ at V_{IH} Before Power-down	t_{PD}	0			µs	
V_{CC} Slew from 4.5V to 4.25V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$ at V_{IH} after Power-up	t_{REC}	2	80	125	ms	

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. t_{DH} is measured from $\overline{WE}$ going high. If $\overline{CE}$ is used to terminate the write cycle then t_{DH} = 20 ns.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.
8. If the $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state in this period.
9. Each DS2227 is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The minimum expected t_{DR} is defined as starting at the date of manufacture.
10. Timings are valid only when $\overline{CE}$ is tied low.

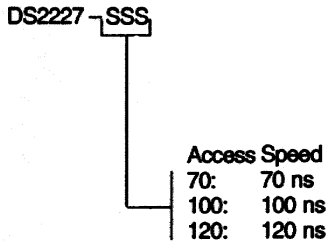
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All Voltages are Referenced to Ground

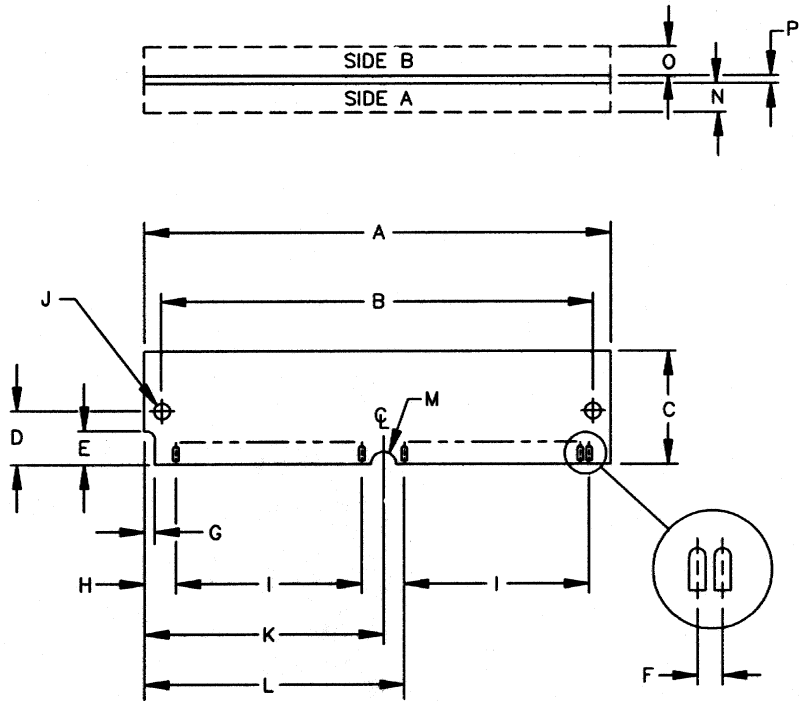
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL gate
Input Pulse Levels: 0 - 3.0 V
Timing Measurements Reference Levels:
Input - 1.5V
Output - 1.5V
Input Pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION



DS2227 72-PIN SIP STIK



DIM	72-PIN	
	MIN	MAX
A	4.245	4.255
B	3.979	3.989
C	0.845	0.855
D	0.395	0.405
E	0.245	0.255
F	0.050 BASIC	
G	0.075	0.085
H	0.245	0.255
I	1.750 BASIC	
J	0.120	0.130
K	2.120	2.130
L	2.245	2.255
M	0.057	0.067
N	-	0.140
O	-	0.140
P	-	0.054

NOTE: DIMENSIONS ARE SHOWN IN INCHES.