

Features

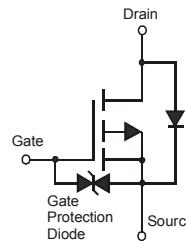
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected**
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**



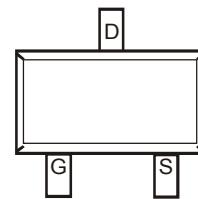
ESD PROTECTED



Top View



Equivalent Circuit



Top View

Mechanical Data

- Case: SOT-323
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminals: Finish - Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.006 grams (approximate)

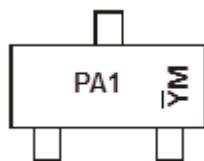
Ordering Information (Note 4)

Part Number	Case	Packaging
DMG1013UW-7	SOT-323	3000 / Tape & Reel

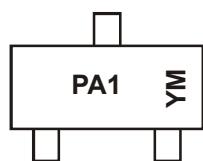
Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>

Marking Information



Chengdu A/T Site



Shanghai A/T Site

PA1 = Product Type Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)

YM = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Y or YM = Year (ex: A = 2013)

M = Month (ex: 9 = September)

Date Code Key

Year	2008	2009	2010	2011	2012	2013	2014	2015				
Code	V	W	X	Y	Z	A	B	C				
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage			V_{GSS}	± 6	V
Continuous Drain Current (Note 5)	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +85^\circ\text{C}$	I_D	-0.82 -0.54	A
Pulsed Drain Current (Note 6)			I_{DM}	-6	A

Thermal Characteristics

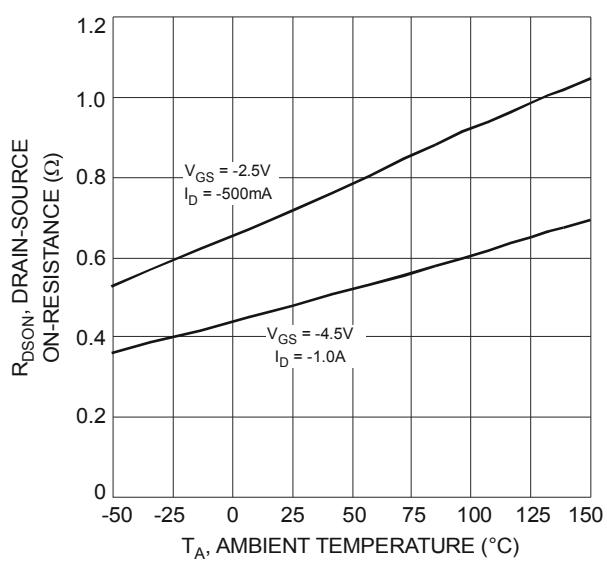
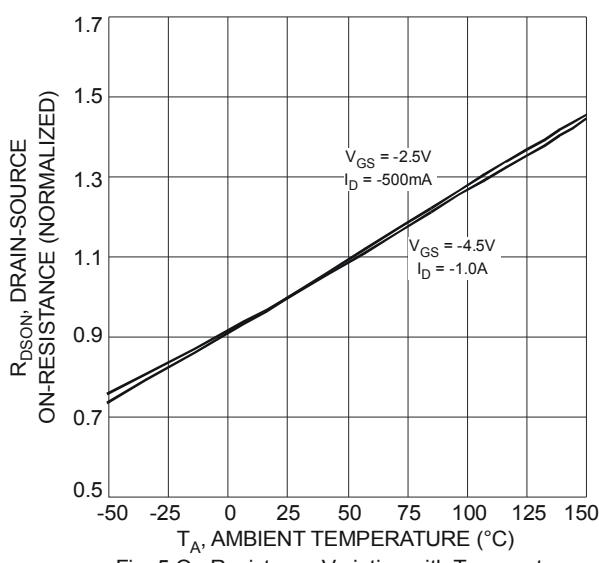
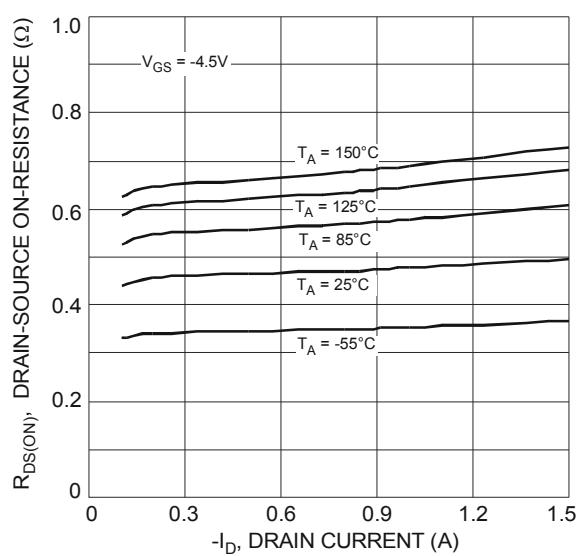
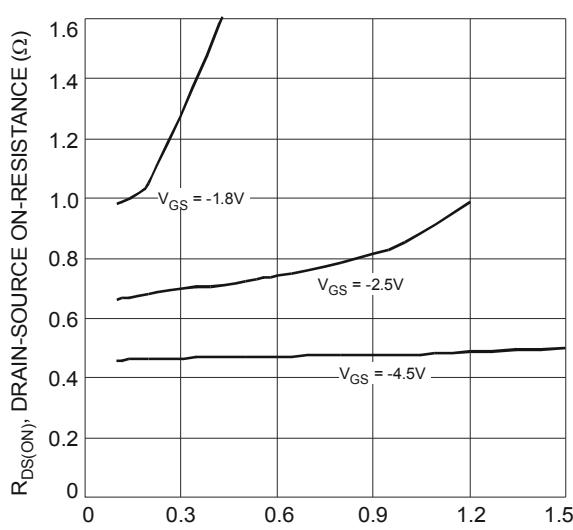
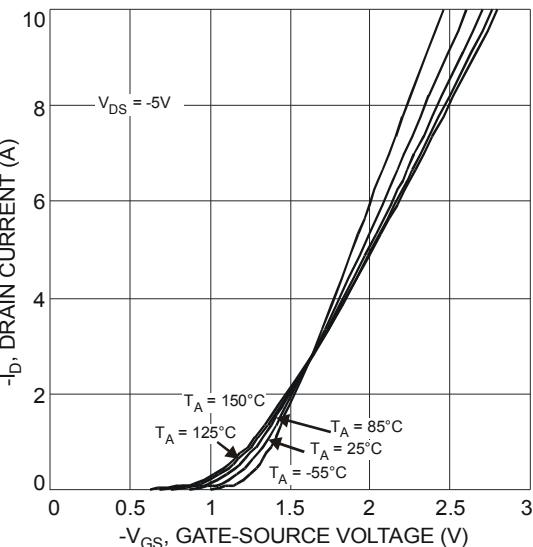
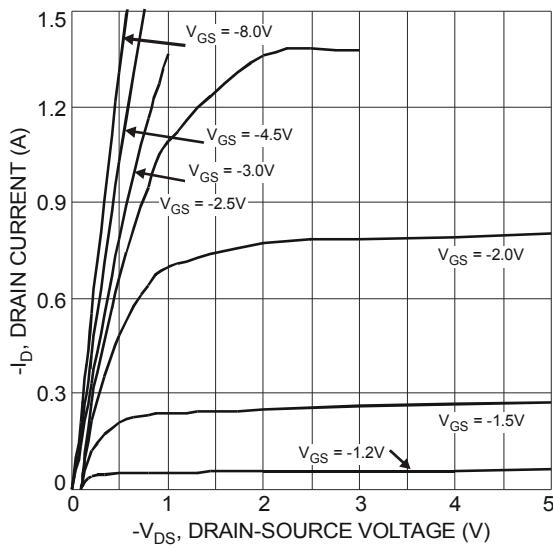
Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	0.31	W
Thermal Resistance, Junction to Ambient @ $T_A = +25^\circ\text{C}$ (Note 5)	$R_{\theta JA}$	398	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Notes: 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
6. Repetitive rating, pulse width limited by junction temperature.

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	-	-	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	-	-	-100	nA	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	-	-	± 2.0	μA	$V_{GS} = \pm 4.5\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.5	-	-1.0	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	-	0.5 0.7 1.0	0.75 1.05 1.5	Ω	$V_{GS} = -4.5\text{V}, I_D = -430\text{mA}$ $V_{GS} = -2.5\text{V}, I_D = -300\text{mA}$ $V_{GS} = -1.8\text{V}, I_D = -150\text{mA}$
Forward Transfer Admittance	$ Y_{fs} $	-	0.9	-	S	$V_{DS} = -10\text{V}, I_D = -250\text{mA}$
Diode Forward Voltage	V_{SD}		-0.8	-1.2	V	$V_{GS} = 0\text{V}, I_S = -150\text{mA}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	59.76	-	pF	$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	12.07	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	6.36	-	pF	
Total Gate Charge	Q_g	-	622.4	-	pC	$V_{GS} = -4.5\text{V}, V_{DS} = -10\text{V}, I_D = -250\text{mA}$
Gate-Source Charge	Q_{gs}	-	100.3	-	pC	
Gate-Drain Charge	Q_{gd}	-	132.2	-	pC	
Turn-On Delay Time	$t_{D(on)}$	-	5.1	-	ns	$V_{DD} = -10\text{V}, V_{GS} = -4.5\text{V}, R_L = 47\Omega, R_G = 10\Omega, I_D = -200\text{mA}$
Turn-On Rise Time	t_r	-	8.1	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	28.4	-	ns	
Turn-Off Fall Time	t_f	-	20.7	-	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.



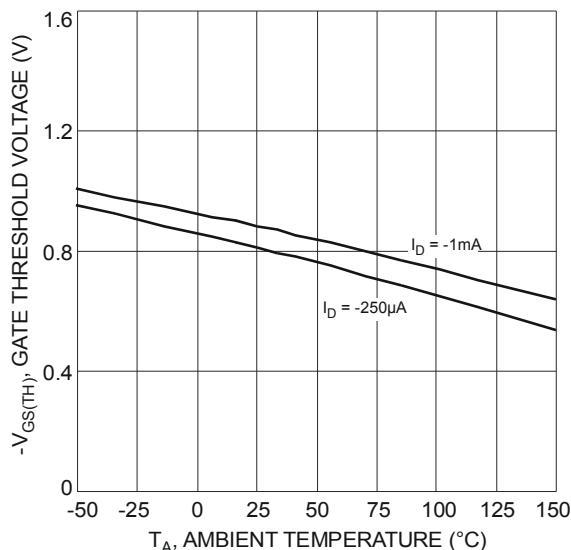


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

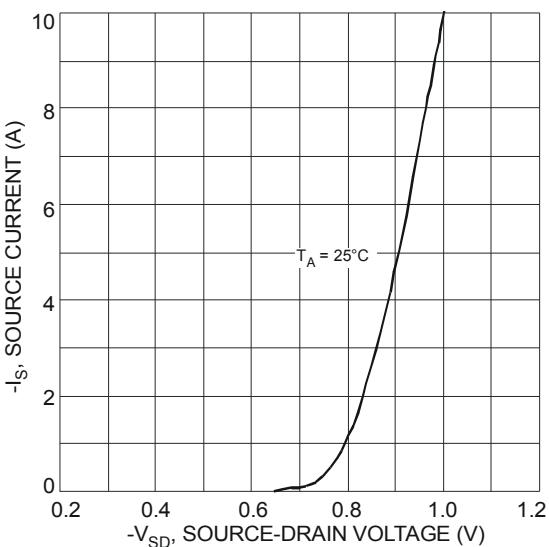


Fig. 8 Diode Forward Voltage vs. Current

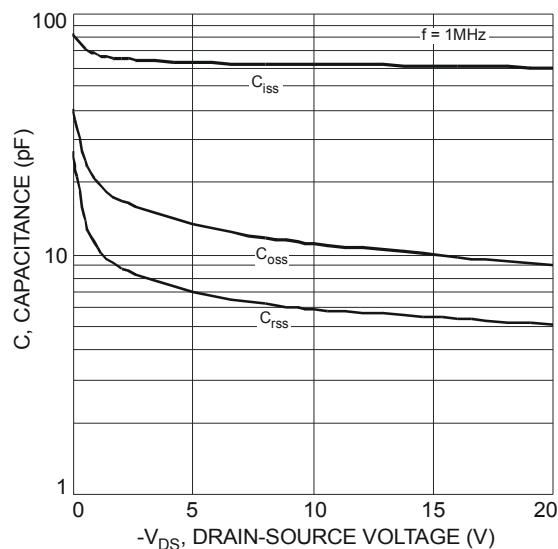


Fig. 9 Typical Total Capacitance

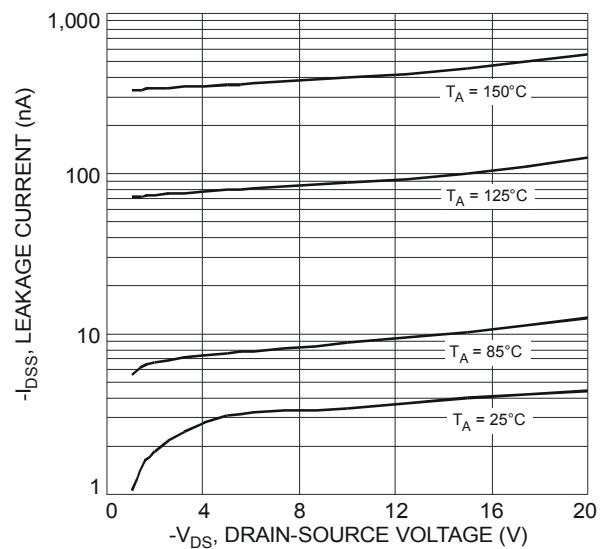


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

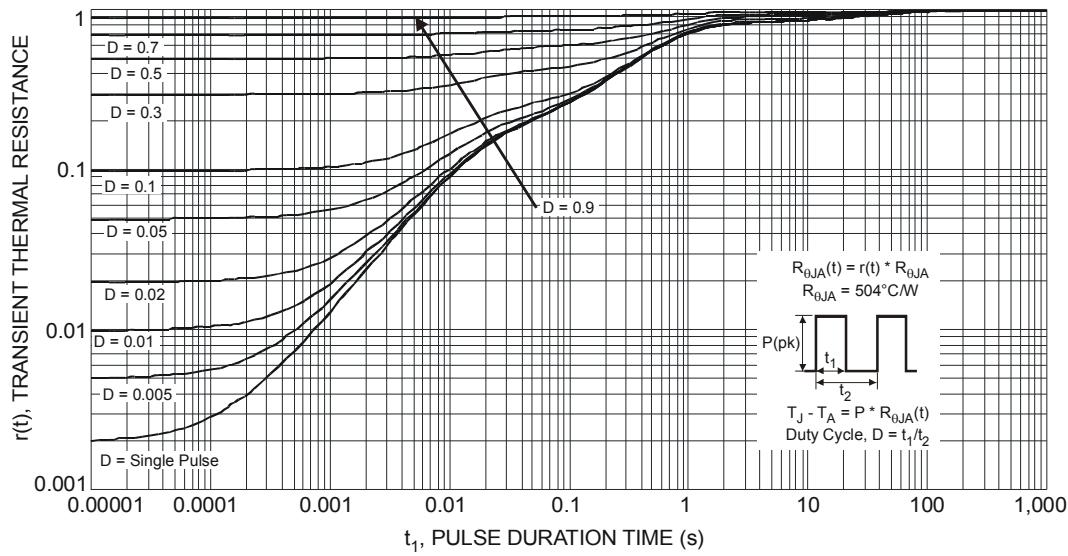
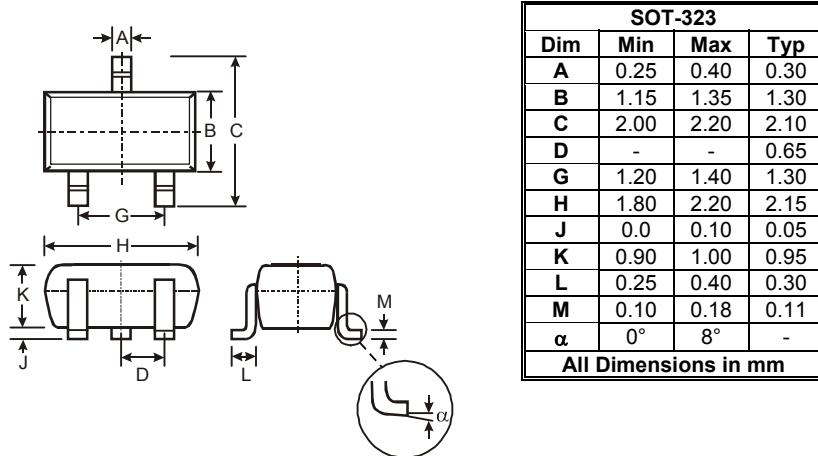


Fig. 11 Transient Thermal Response

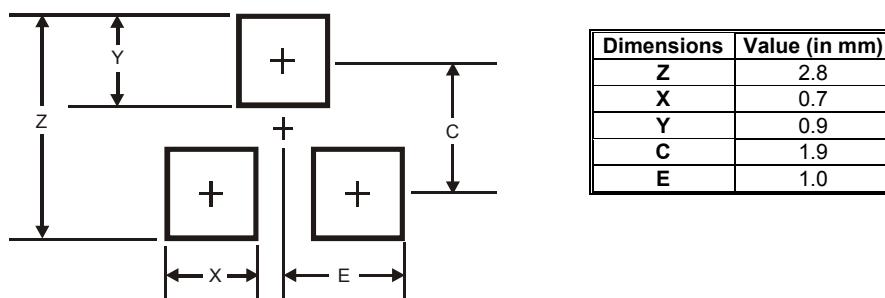
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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