INTERSIL

ICL8052/ICL7104 and ICL8068/ICL7104

16/14/12 Bit Binary A/D Converter Pairs for μProcessors

FEATURES

- 16 bit binary three-state latched outputs plus polarity and overrange. Also 14 and 12 bit versions.
- Ideally suited for interface to UARTs, microprocessors, or other complex circuitry.
- Conversion on demand or continuously.
- Handshake byte-serial transmission synchronously or on demand.
- Guaranteed zero reading for zero volts input.
- True polarity at zero count for precise null detection.
- Single reference voltage for true ratiometric operation.
- Onboard clock and reference.
- Auto-Zero; Auto-Polarity
- Accuracy guaranteed to 1 count.
- All outputs TTL compatible.
- ±10V analog input range
- Status signal available for external sync, A/Z in preamp, etc.

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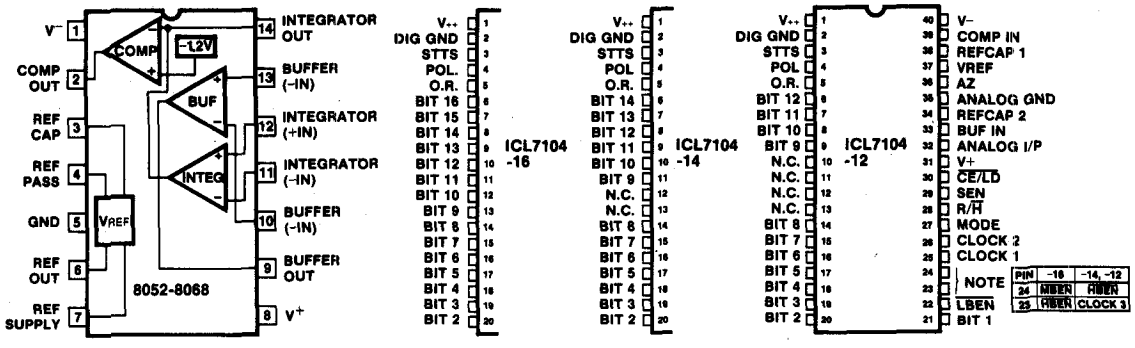
GENERAL DESCRIPTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Intersil's high performance A/D converter family. The 16-bit version, the ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for a wide range of output interfacing. The ICL7014-14 and ICL7104-12 are 14 and 12-bit versions. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc.

PIN CONFIGURATIONS



(OUTLINE DWGS DD,JD,PD)

(OUTLINE DWGS DL,JL,PL)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14-Pin Plastic DIP	ICL8052CPD
8052	0°C to 70°C	14-Pin Ceramic DIP	ICL8052CDD
8052A	0°C to 70°C	14-Pin Plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14-Pin Ceramic DIP	ICL8052ACDD
8068	0°C to 70°C	14-Pin CERDIP	ICL8068CJD
8068A	0°C to 70°C	14-Pin CERDIP	ICL8068ACJD

Part	Temp. Range	Package	Order Number
7104 12-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-12CJL
7104 12-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-12CPL
7104 12-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-12CDL
7104 14-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-14CJL
7104 14-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-14CPL
7104 14-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-14CDL
7104 16-Bit	0°C to 70°C	40-Pin CERDIP	ICL7104-16CJL
7104 16-Bit	0°C to 70°C	40-Pin Plastic DIP	ICL7104-16CPL
7104 16-Bit	0°C to 70°C	40-Pin Ceramic DIP	ICL7104-16CDL

ABSOLUTE MAXIMUM RATINGS

Power Dissipation[1] 500mW
Storage Temperature ..... −65°C to +150°C

8052, 8068

Supply Voltage ..... ±18V
Differential Input Voltage(8068) ..... ±30V
(8052) ..... ±6V
Input Voltage[2] ..... ±15V
Output Short Circuit Duration,
All Outputs[3] ..... Indefinite
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 10 Sec.) ..... 300°C

7104

V+ Supply (GND to V+) 12V
V++ to V− 32V
Positive Supply Voltage (GND to V++) 17V
Negative Supply Voltage (GND to V−) 17V
Analog Input Voltage (Pin 32-39)[4] ..... V+ to V−
Digital Input Voltage ..... V+ +0.3V
(Pins 2-30)[5] ..... GND −0.3V

Notes:

1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70° C. For higher temperatures, derate 10mW/° C.
2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3: Short circuit may be to ground or either supply. Rating applies to +70° C ambient temperature.
4: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
5: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ICL7104 before its power supply is established.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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7104 ELECTRICAL CHARACTERISTICS (V+ = +5V, V++ = +15V, V− = −15V, Ta = 25°C)

CHARACTERISTICS		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Input	CLOCK 1	I_{IN}	Vin = +5V to 0V	±2	±7	±30	μA
Comparator I/P	COMP IN (Note 1)	I_{IN}	Vin = 0V to +5V	−10	±0.001	+10	μA
Inputs with Pulldown	MODE	I_{IH}	Vin = +5V	+1	+5	+30	μA
		I_{IL}	Vin = 0V	−10	±0.01	+10	μA
Inputs with Pullups	SEN, R/$\overline{R}$	I_{IH}	Vin = +5V	−10	±0.01	+10	μA
	$\overline{LBEN}$, $\overline{MBEN}$, $\overline{HBEN}$, CE/$\overline{LD}$ (Note 2)	I_{IL}	Vin = 0V	−30	−5	−1	μA
Input High Voltage	All Digital Inputs	V_{IH}		2.5	2.0	—	V
Input Low Voltage	All Digital Inputs	V_{IL}			1.5	1.0	V
Digital Outputs Three-Stated On	$\overline{LB\ EN}$	V_{OL}	I_{OL} = 1.6 mA	—	.27	.4	V
	$\overline{MB\ EN}$ (16 only) (Note 3)	V_{OH}	I_{OH} = −10μA		4.5	—	V
	$\overline{HB\ EN}$	V_{OH}	I_{OH} = −240μA	2.4	3.5	—	V
	CE/$\overline{LD}$						
	BIT n, POL, OR						
Digital Outputs Three-Stated Off	BIT n, POL, OR	I_{OL}	0 ≤ Vout ≤ V+	−10	±.001	+10	μA
Non-Three-State Digital Output	STTS	V_{OL}	I_{OL} = 3.2 mA	—	.3	.4	V
		V_{OH}	I_{OH} = −400μA	2.4	3.3	—	V
	CLOCK 2	V_{OL}	I_{OL} = 320μA		0.5		V
		V_{OH}	I_{OH} = −320μA		4.5		V
	CLOCK 3 (-12, -14 ONLY)	V_{OL}	I_{OL} = 1.6 mA		.27	.4	V
		V_{OH}	I_{OH} = −320μA	2.4	3.5		V
Switch	Switch 1	$r_{DS(on)}$		—	25k		Ω
	Switches 2,3	$r_{DS(on)}$		—	4k	20k	Ω
	Switches 4,5,6,7,8,9	$r_{DS(on)}$		—	2k	10k	Ω
	Switch Leakage	$I_{D(off)}$		—	15		pA
Clock	Clock Freq. (Note 4)			DC	200	400	kHz
Supply Currents	+5V Supply Current All outputs high impedance	I+	Freq. = 200 kHz		200	600	μA
	+15V Supply Current	I++	Freq. = 200 kHz		.3	1.0	mA
	−15V Supply Current	I−	Freq. = 200 kHz		25	200	μA
Supply Voltage Range	Logic Supply	V+	Note 5	4.0		+11.0	V
	Positive Supply	V++		+10.0		+16.0	V
	Negative Supply	V−		−16.0		−10.0	V

Note 1: This spec applies when not in Auto-Zero phase.
Note 2: Apply only when these pins are inputs, i.e., the mode pin is low, and the 7104 is not in handshake mode.
Note 3: Apply only when these pins are outputs, i.e., the mode pin is high or the 7104 is in handshake mode.
Note 4: Clock circuit shown in Figs. 10 and 11.
Note 5: V+ must not be more positive than V++.

8068 ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	CONDITIONS	8068 MIN	8068 TYP	8068 MAX	8068A MIN	8068A TYP	8068A MAX	UNITS
	EACH OPERATIONAL AMPLIFIER								
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	65		20	65	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		175	250		80	150	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
A_V	Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			2			2		MHz
I_{SC}	Output Short-Circuit Current			5	10		5	10	mA
	COMPARATOR AMPLIFIER								
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
	VOLTAGE REFERENCE								
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPP}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPP}	Supply Current Total				14		8	14	mA

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8052 ELECTRICAL CHARACTERISTICS (V_{SUPP} = ±15V unless otherwise specified)

SYMBOL	CHARACTERISTICS	CONDITIONS	8052 MIN	8052 TYP	8052 MAX	8052A MIN	8052A TYP	8052A MAX	UNITS
	EACH OPERATIONAL AMPLIFIER								
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
A_V	Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			1			1		MHz
I_{SC}	Output Short-Circuit Current			20	100		20	100	mA
	COMPARATOR AMPLIFIER								
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
	VOLTAGE REFERENCE								
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		ohms
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPP}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPP}	Supply Current Total			6	12		6	12	mA

Note 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\,Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 2: This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: 8068/7104

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency = 200KHz

CHARACTERISTICS	CONDITIONS	8068A/7104-12			8068A/7104-14			8068A/7104-16			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	-.000	±.000	+.000	-0.0000	±0.0000	+0.0000	-0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (1)	$V_{in} = V_{Ref.}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step	$-4V \le V_{in} \le +4V$		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 4V$		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		3			2			2		μV
Leakage Current at Input (2)	V_{in} = 0V		200	265		100	165		100	165	pA
Zero Reading Drift	V_{in} = 0V 0° C ≤ T_A ≤ 70° C		1	5		0.5	2		0.5	2	μV/° C
Scale Factor Temperature (3) Coefficient	V_{in} = +4V 0 ≤ T_A ≤ 50° C (ext. ref. 0 ppm/° C)		2	5		2	5		2	5	ppm/° C

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SYSTEM ELECTRICAL CHARACTERISTICS: 8052/7104

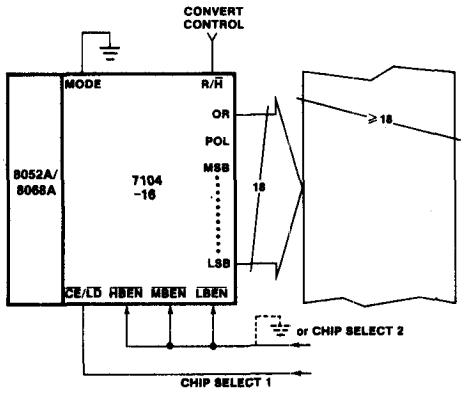
(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency = 200KHz

CHARACTERISTICS	CONDITIONS	8052/7104-12			8052A/7104-14			8052A/7104-16			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	-.000	±.000	+.000	-0.0000	±0.0000	+0.0000	-0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (3)	$V_{in} = V_{Ref.}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-4V \le V_{in} \le +4V$		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 4V$		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		20 50			30			30		μV
Leakage Current at Input (2)	V_{in} = 0V		30	80		20	30		20	30	pA
Zero Reading Drift	V_{in} = 0V 0° ≤ T_A ≤ 70° C		1	5		0.5	2		0.5	2	μV/° C
Scale Factor Temperature Coefficient	V_{in} = +4V 0 ≤ T_A ≤ 70° C (ext. ref. 0 ppm/° C)		3	15		2	5		2	5	ppm/° C

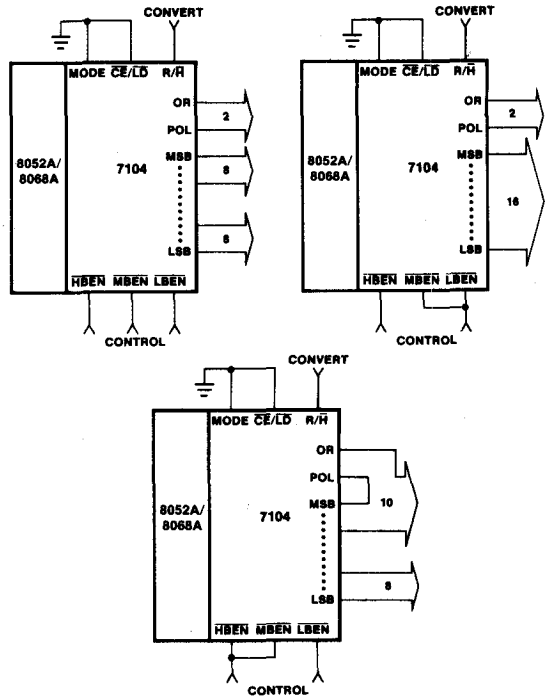
Note 1: Tested with low dielectric absorption integrating capacitor.

Note 2: The input bias currents are junction leakage currents which approximately double for every 10° C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA$ Pd where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 3: The temperature range can be extended to 70° C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.



Full 18 Bit Three State Output



Various Combinations of Byte Disables

AC CHARACTERISTICS (V++ = +15V, V+ = +5V, V− = −15V)

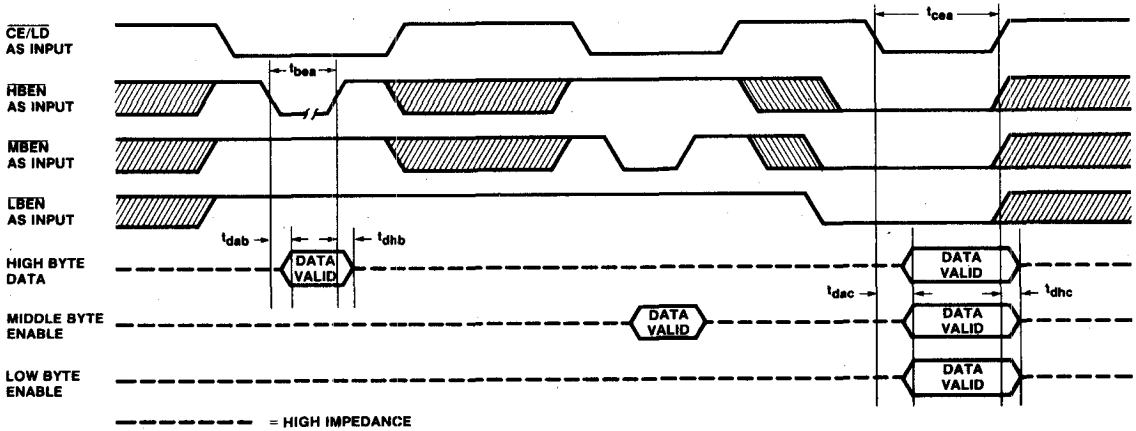


TABLE 1: Direct Mode Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{bea}	$\overline{XBEN}$ Min. Pulse Width		500		ns
t_{dab}	Data Access Time from $\overline{XBEN}$		200		
t_{dhb}	Data Hold Time from $\overline{XBEN}$		200		
t_{cea}	$\overline{CE/LD}$ Min. Pulse Width		500		
t_{dac}	Data Access Time from $\overline{CE/LD}$		200		
t_{dhc}	Data Hold Time from $\overline{CE/LD}$		200		
t_{cwh}	CLOCK 1 High Time	1250	1000		

TABLE 2: Handshake Timing Requirements

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{mw}	MODE Pulse (minimum)		20		ns
t_{sm}	MODE pin set-up time		−150		
t_{me}	MODE pin high to low Z $\overline{CE/LD}$ high delay		200		
t_{mb}	MODE pin high to $\overline{XBEN}$ low Z (high) delay		200		
t_{cel}	CLOCK 1 high to $\overline{CE/LD}$ low delay		700		
t_{ceh}	CLOCK 1 high to $\overline{CE/LD}$ high delay		600		
t_{cbl}	CLOCK 1 high to $\overline{XBEN}$ low delay		900		
t_{cbh}	CLOCK 1 high to $\overline{XBEN}$ high delay		700		
t_{cdh}	CLOCK 1 high to data enabled delay		1100		
t_{cdl}	CLOCK 1 low to data disabled delay		1100		
t_{ss}	Send ENable set-up time		−350		
t_{cbz}	CLOCK 1 high to $\overline{XBEN}$ disabled delay		2000		
t_{cez}	CLOCK 1 high to $\overline{CE/LD}$ disabled delay		2000		
t_{cwh}	CLOCK 1 High Time	1250	1000		

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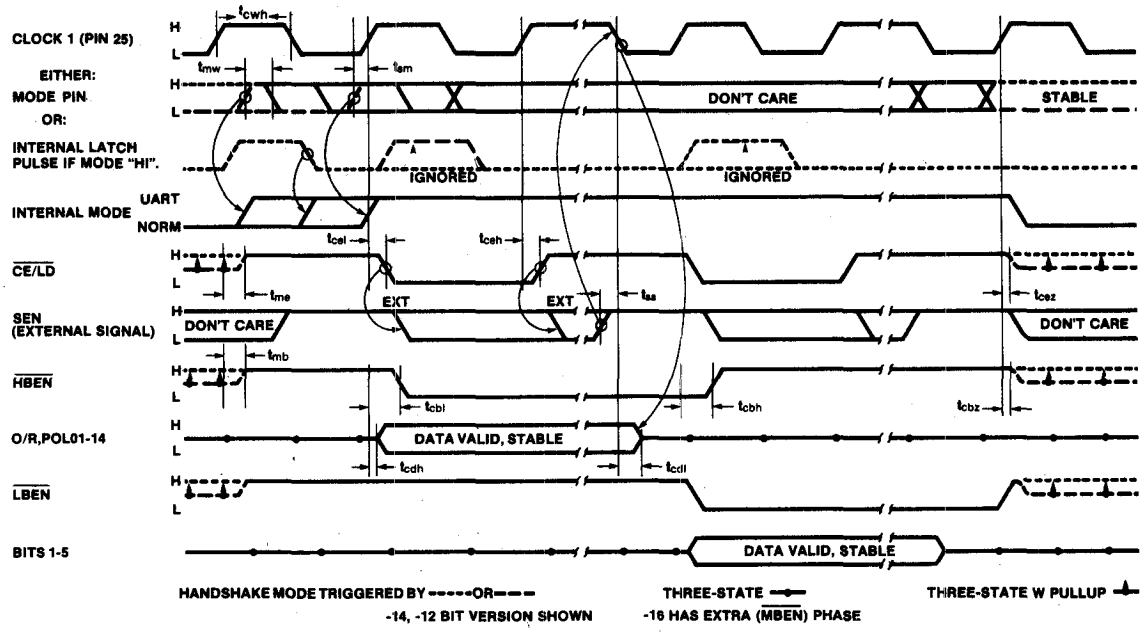


Timing Relationships In Handshake Mode

TABLE 3: Pin Assignment and Function Description

PIN	SYMBOL	OPTION	DESCRIPTION
1	V(++)		Positive Supply Voltage Nominally +15V
2	GND		Digital Ground .0V, ground return
3	STTS		STaTuS output .HI during Integrate and Deintegrate until data is latched .LO when analog section is in Auto-Zero configuration.
4	POL		POLarity. Three-state output. HI for positive input.
5	OR		OverRange. Three-state output.
6	BIT 16 BIT 14 BIT 12	−16 −14 −12	(Most significant bit)
7	BIT 15 BIT 13 BIT 11	−16 −14 −12	Data Bits, Three-state outputs. See Table 4 for format of $\overline{\text{EN}}$ables and bytes. HIGH = true
8	BIT 14 BIT 12 BIT 10	−16 −14 −12	
9	BIT 13 BIT 11 BIT 9	−16 −14 −12	
10	BIT 12 BIT 10 nc	−16 −14 −12	
11	BIT 11 BIT 9 nc	−16 −14 −12	
12	BIT 10 nc nc	−16 −14 −12	
13	BIT 9 nc nc	−16 −14 −12	
14	BIT 8		
15	BIT 7		
16	BIT 6		
17	BIT 5		
18	BIT 4		
19	BIT 3		
20	BIT 2		
21	BIT 1		Least significant bit
22	$\overline{\text{LBEN}}$		Low Byte $\overline{\text{EN}}$able. If not in handshake mode (see pin 27) when LO (with $\overline{\text{CE}}/\overline{\text{LD}}$, pin 30) activates low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 8, 9 and 10.
23	$\overline{\text{MBEN}}$	−16	Mid Byte $\overline{\text{EN}}$able. Activates BITS 9-16, see $\overline{\text{LBEN}}$ (pin 22).
	$\overline{\text{HBEN}}$	−14 −12	High Byte $\overline{\text{EN}}$able. Activates BITS 9-14, POL, OR, see $\overline{\text{LBEN}}$ (pin 22)
24	$\overline{\text{HBEN}}$ CLOCK3	−16 −14 −12	High Byte $\overline{\text{EN}}$able. Activates POL, OR, see $\overline{\text{LBEN}}$ (pin 22). RC oscillator pin. Can be used as clock output.

PIN	SYMBOL	DESCRIPTION
25	CLOCK1	Clock input. External clock or oscillator.
26	CLOCK2	Clock output. Crystal or RC oscillator.
27	MODE	Input LO;Direct output mode where $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ act as inputs directly controlling byte outputs. If pulsed HI causes immediate entry into handshake mode (see Figure 9). If HI, enables $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ as outputs. Handshake mode will be entered and data output as in Figures 7 & 8 at conversion completion.
28	R/$\overline{\text{H}}$	Run/$\overline{\text{Hold}}$; Input HI-conversions continuously performed every 2^{17} (−16) 2^{15} (−14) or 2^{13} (−12) clock pulses. Input LO-conversion in progress completed, converter will stop in Auto-Zero 7 counts before input integrate.
29	SEN	Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates 'send'.
30	$\overline{\text{CE}}/\overline{\text{LD}}$	$\overline{\text{C}}$hip-$\overline{\text{E}}$nable/$\overline{\text{L}}$oa$\overline{\text{D}}$. With MODE (pin 27) LO, $\overline{\text{CE}}/\overline{\text{LD}}$ serves as a master output enable; when HI, the bit outputs and POL, OR are disabled. With MODE HI, pin serves as a $\overline{\text{L}}$oa$\overline{\text{D}}$ strobe (-ve going) used in handshake mode. See Figures 7 & 8.
31	V(+)	Positive Logic Supply Voltage. Nominally +5V.
32	AN.IN	ANalog INput. High side.
33	BUF IN	BUFfer INput to analog chip (ICL8052 or ICL8068)
34	REFCAP2	REFerence CAPacitor (negative side)
35	AN.GND.	ANalog GrouND. Input low side and reference low side.
36	A-Z	Auto-Zero node.
37	VREF	Voltage REFerence input (positive side)
38	REFCAP1	REFerence CAPacitor (positive side)
39	COMP-IN	COMParator INput from 8052/8068
40	V(−)	Negative Supply Voltage. Nominally −15V.

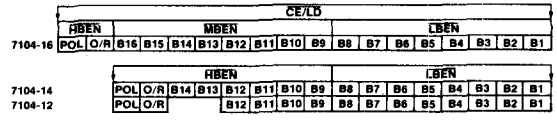


TABLE 4: Three-State Byte Formats and $\overline{\text{EN}}$able Pins.

Fig. 1 shows the functional block diagram of the operating system. For a detailed explanation, refer to fig. 2 below.

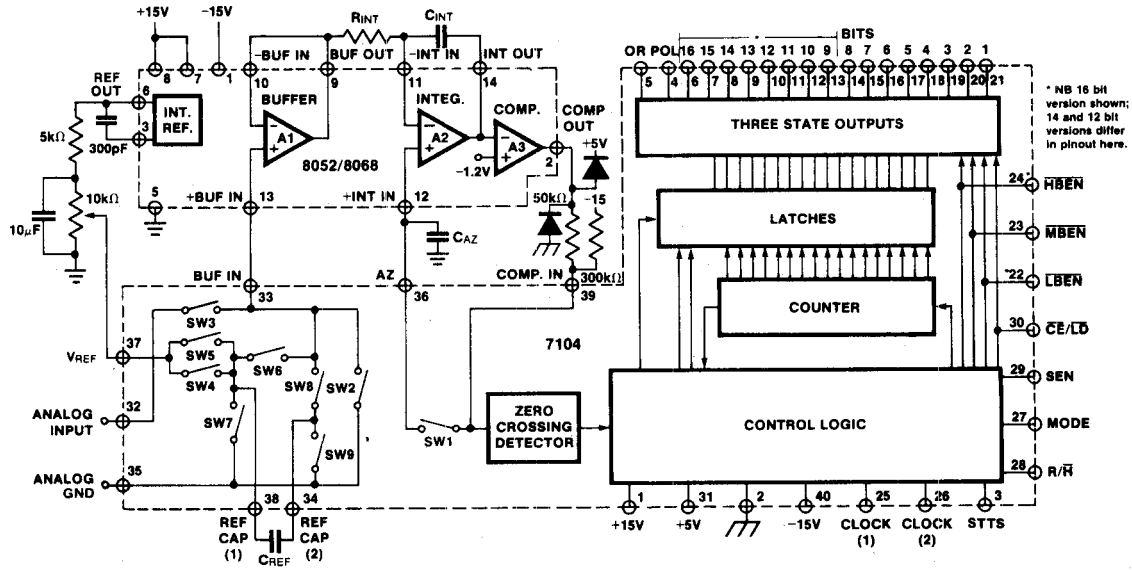


Figure 1: 8052A (8068A)/7104 16/14/12 Bit A/D Converter Functional Block Diagram

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent Circuit of the Analog Section of both the ICL7104/8052 and the ICL7104/8068 in the 3 different phases of operation. If the Run/$\overline{\text{Hold}}$ pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 131,072 for −16; 32,368 for −14; and 8092 for −12 clock periods per cycle (see Figure conversion timing).

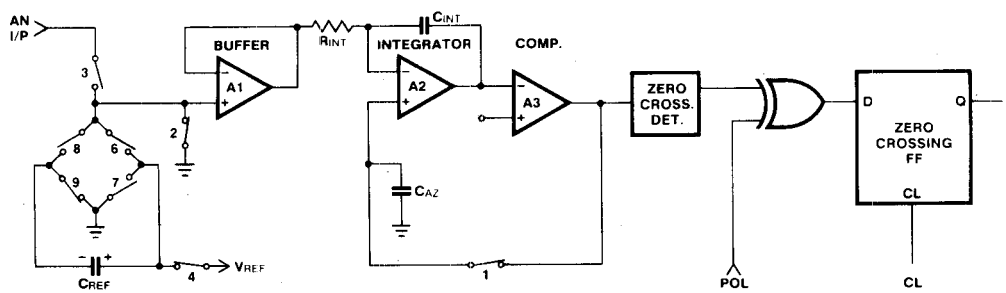


Figure 2A: Phase I Auto-Zero

1. **Auto-Zero Phase I** Fig. 2A

   During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output no longer changes with time. Also, switches 4 and 9 recharge the reference capacitor to V_{REF}.

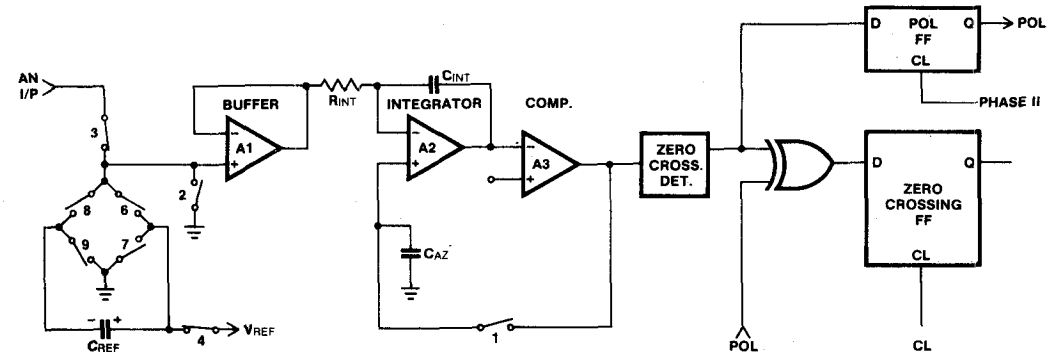


Figure 2B: Phase II Integrate Input

2. Input Integrate Phase II Fig. 2B

During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to V_{REF} during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

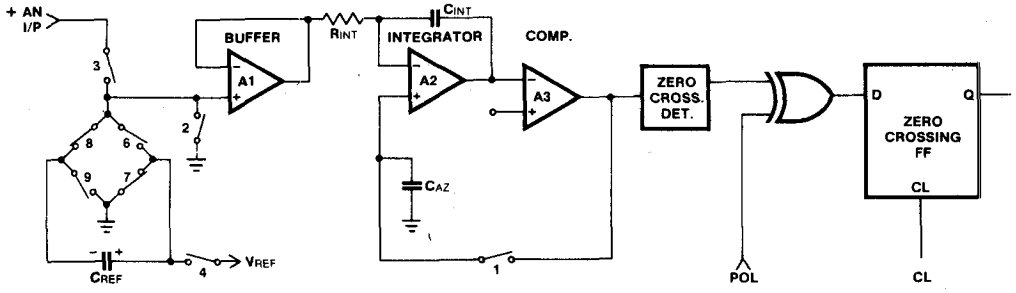


Figure 2C: Phase III + Deintegrate

Deintegrate Phase III Fig. 2C & D

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause $+V_{REF}$ to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate phase, the input voltage required to give a full scale reading = $2V_{REF}$.

Note: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/$\overline{\text{Hold}}$ is manipulated, see Run/$\overline{\text{Hold}}$ Input in detailed description, digital section).

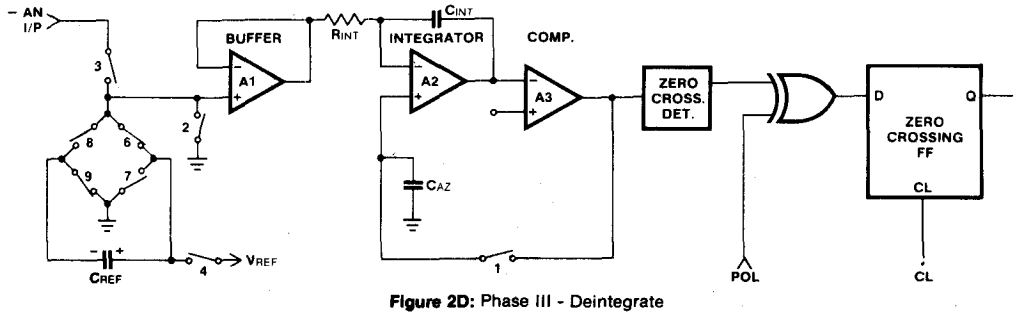
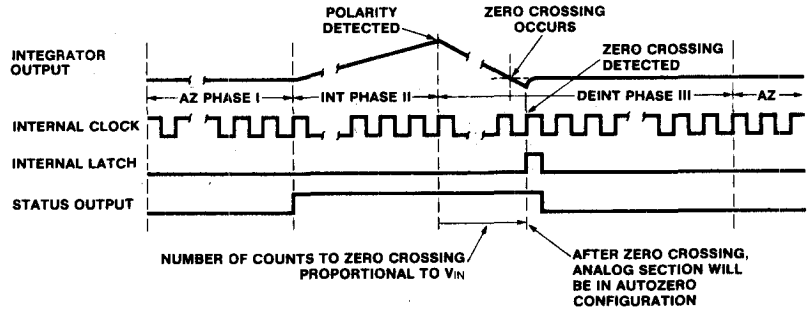


Figure 2D: Phase III - Deintegrate



	COUNTS		
	Phase I	Phase II	Phase III
-16	32768	32768	65536
-14	8192	8192	16384
-12	2048	2048	4096

Figure 3: Conversion Timing

4

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40 μA give good results with a nominal of 20 μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then -

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is give by

$$C_{INT} = \frac{\begin{bmatrix}\text{(32768 for -16}\\ \text{(8192 for -14 X clock period)}\\ \text{(2048 for -12}\end{bmatrix} \text{ X } (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale (100...000) and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of 1/3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 4. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1-2μV, allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermo-electric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. For further discussion, see App. Note A030.

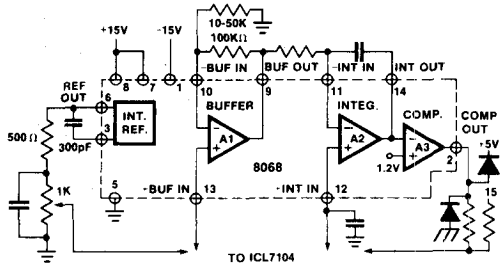


Figure 4: Adding Buffer Gain to ICL8068

Table 5: Typical Component Values

V++ = +15V, V+ = 5V, V− = −15V, Clock Freq = 200 kHz

ICL8052/8068 with	ICL7104-16			ICL7104-14		ICL7104-12		UNITS
Full scale V_{IN}	200	800	4000	100	4000	50	4000	mV
Buffer Gain	10	1	1	10	1	10	1	
R_{INT}	100	43	200	47	180	27	200	kΩ
C_{INT}	.33	.33	.33	0.1	0.1	.022	.022	μF
C_{AZ}	1.0	1.0	1.0	1.0	1.0	.47	.47	μF
C_{ref}	10	1.0	1.0	10	1.0	4.7	4.7	μF
V_{REF}	100	400	2000	50	2000	25	200	mV
Resolution	3.1	12	61	6.1	244	12	980	μV

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and for systems where system noise is a limiting factor, particularly in low signal level conditions, will give better performance.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator circuit, a 16, 14 or 12 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 5 (16 bit version shown).

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ICL7104 Electrical Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14 and 7104-12, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.

Run/Hold Input

When the Run/Hold input is connected to V+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16, 32768 for 7104-14 and 8192 for 7104-2 clock periods, regardless of the resulting value.

If Run/Hold goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/Hold stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/Hold input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/Hold. See Figure 6 for details.

Using the Run/Hold input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in Auto-Zero with Run/Hold low. When Run/Hold goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). Run/Hold may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/Hold can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/Hold input can be provided by connecting it to the CLOCK3 (-12, -14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

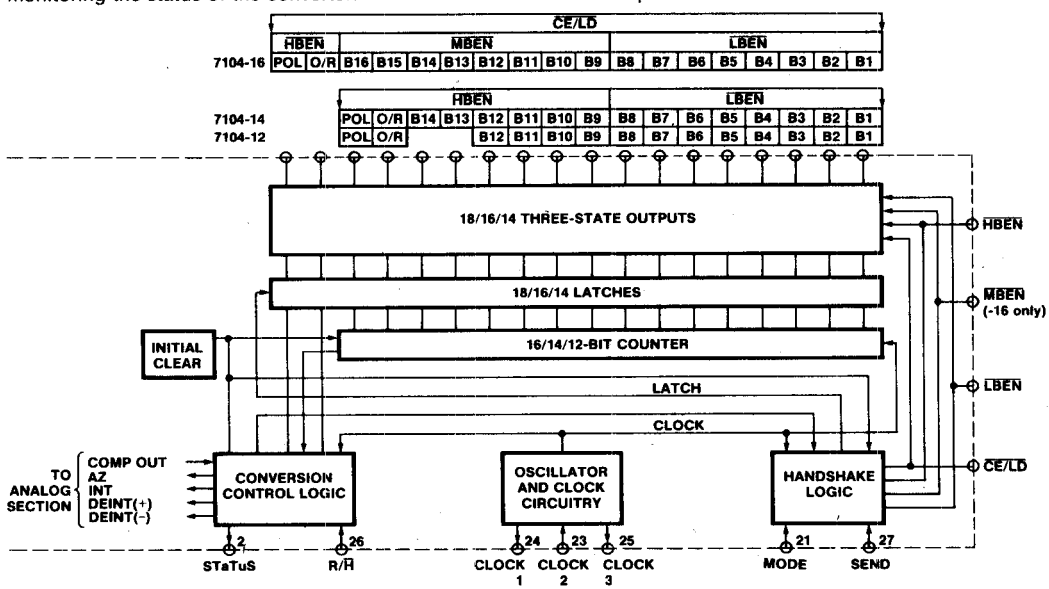


Figure 5: Digital Section

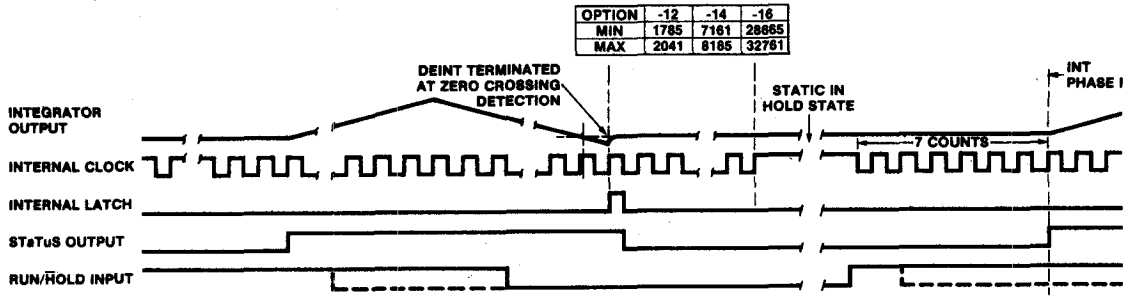


Figure 6: Run/Hold Operation

If the Run/Hold input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/Hold to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs[bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes]are accessible under control of the byte and chip ENable terminals as inputs. These ENable inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip ENable input is low, taking a byte ENable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used. The timing requirements for these outputs are shown under AC Characteristics and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

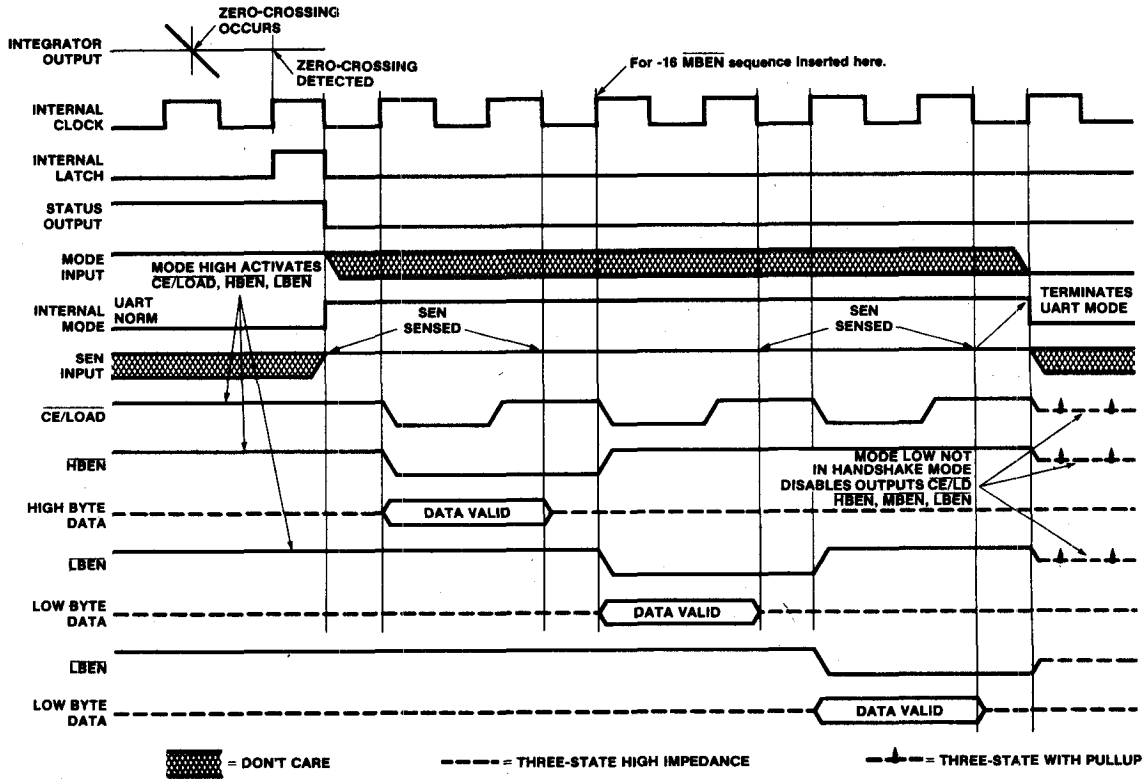


Figure 7: Handshake With SEN Held Positive

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte ENable inputs. This mode is specifically designed to allow a direct interface between the ICL7104 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7104 provides all the control and flag signals necessary to sequence the three (ICL7106-16) or two (ICL7104-14, -12) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte ENable terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send ENable pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte ENable line goes low, and the Chip ENable/LoaD line (pin 30) (CE/LD) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte ENable pin will be cleared high, and (unless finished) the CE/LD and the next byte ENable pin will go low. This will continue until all three (2 in the case of 12 and 14 bit devices) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte ENable pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip ENable will be three-stated off, if MODE is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 7, 8, and 9, and Table 2.

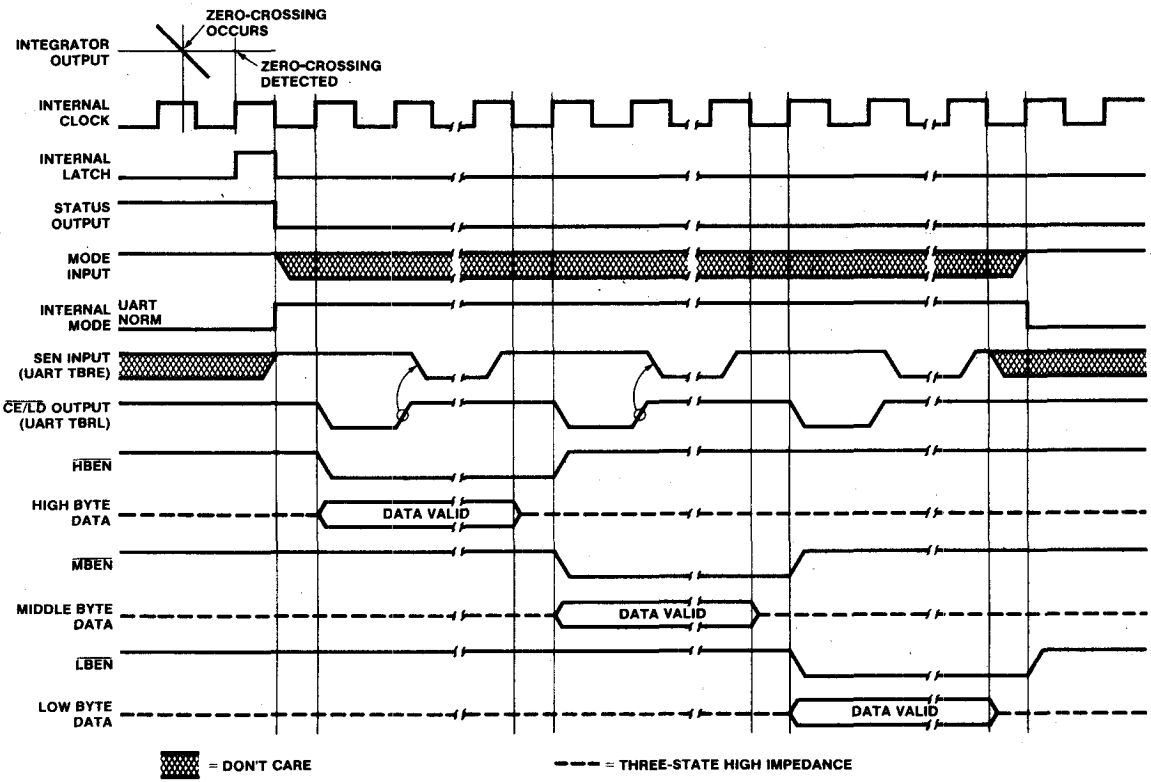


Figure 8: Handshake - Typical UART Interface Timing

Figure 7 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{CE}/\overline{LD}$, $\overline{LBEN}$, $\overline{MBEN}$ and $\overline{HBEN}$ terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{CE}/\overline{LD}$ and the $\overline{HBEN}$ outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bis 9-14) outputs are enabled. The $\overline{CE}/\overline{LD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte $\overline{EN}$able remains low for two clock periods. Thus the $\overline{CE}/\overline{LD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte $\overline{EN}$able as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using $\overline{CE}/\overline{LD}$, $\overline{MBEN}$ and $\overline{LBEN}$ while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14, -12).

Figure 8 shows an output sequence where the SENinput is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}/\overline{LD}$ terminal of the ICL7104 drives the TBRL (Transmitter Buffer Register Load) input to the UART.

The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The $\overline{CE}/\overline{LD}$ and $\overline{HBEN}$ terminals will go low after SEN is sensed, and the high order byte outputs become active. When $\overline{CE}/\overline{LD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE}/\overline{LD}$ and $\overline{MBEN}$ (-16) or $\overline{LBEN}$ outputs go low, and the corresponding byte outputs become active. Similarly, when the $\overline{CE}/\overline{LD}$ returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for $\overline{LBEN}$. One-half internal clock later, the handshake mode will be cleared, and the chip and byte $\overline{EN}$able terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion

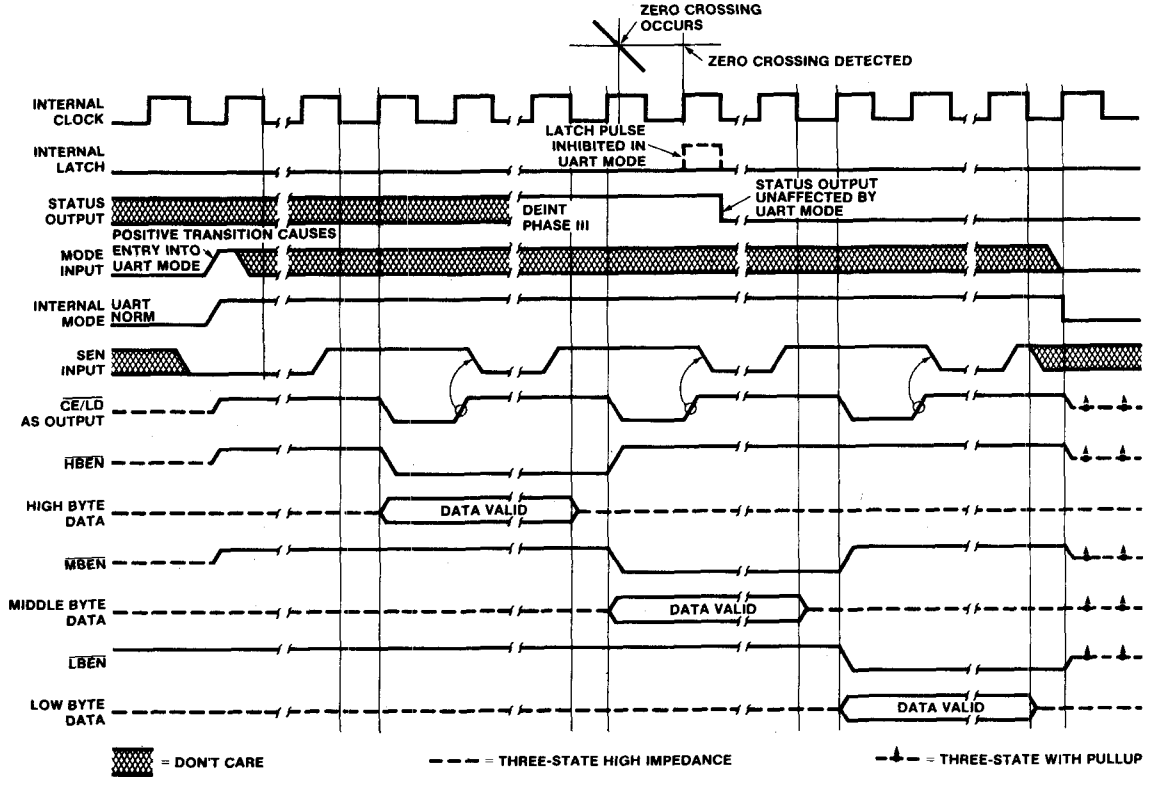


Figure 9: Handshake Triggered By Mode

except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 11 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/$\overline{\text{Hold}}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Initial Clear Circuitry

The internal logic of the 7104 is supplied by an internal regulator between V++ and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" FF cleared (i.e. in "direct" mode). This, however, will also clear these registers if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" FF should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to buss conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE FF will be cleared as fast as possible (see Fig. 7 for timing). For these and other reasons, adequate supply bypass is recommended.

Oscillator

The ICL7104-14 and -12 are provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator.

Figure 10 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by f = .45/RC. A 50-100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 32768 (-16), 8192 (-14), 2048 (-12) clock periods is close to an integral multiple of the 60Hz period.

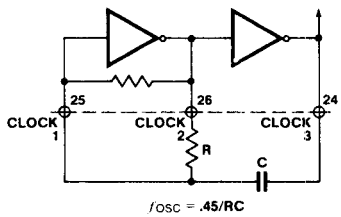


Figure 10: RC Oscillator

Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 11 shows a crystal oscillator circuit, which can be used with all 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.

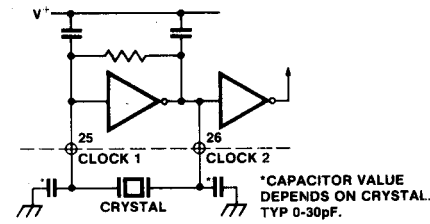


Figure 11: Crystal Oscillator

POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the ICL7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V+ supply (nom. +5V) being more positive than the V++ supply. If there is any possibility of this occuring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V+ and V++ to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of 8068 or 8052/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 12.

APPLICATIONS INFORMATION

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar
A017 "The Integrating A/D Converter", by Lee Evans
A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood
A025 "Building a Remote Data Logging Station", by Peter Bradshaw
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

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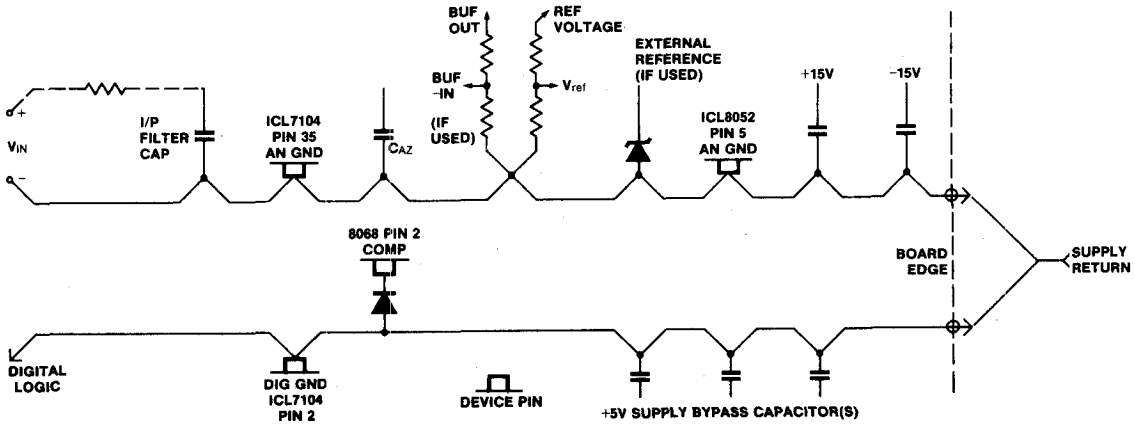

Figure 12: Grounding Sequence

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