S19233

Data Sheet

10 G Ethernet/Fibre Channel/SONET/SDH Dual CDR

FEATURES

- Complies with ITU-T specifications, 50 mUI_{pp} max. jitter generation (50 KHz - 80 MHz)
- Complies with XFP MSA Specifications
- 25 mUI_{pp} Jitter Generation
- CML serial input sensitivity at 5 mV_{pp} Diff.
- Dual CDR - 9.95 to 11.32 Gbps operation
- Superior Crosstalk Isolation
- Electronic Dispersion Compensation (EDC) Optimized for 0 to 100 Km SMF with 2 dB dispersion penalty
- Low power EDC ideal for Power Level 2 XFP modules
- Suitable for low Optical Signal to Noise Ratio (OSNR) environments
- Automatic Threshold Adjust
- External threshold & Phase Adjust
- AGC embedded equalizer
- LOS Function - Compliant to GR-253
- Integrated equalizer that support over 24” FR-4 on Transmitter Electrical Side
- Transmitter (Optical Side) - CDR
- Lock detect indication
- 740 mW Typical Power
- -40 to 85°C operation
- CMOS 0.13 Micron Technology
- 1.8 and 3.3 Volt Power Supply
- 6 mm x 6 mm PBGA package with RoHS compliant lead free option
- ESD - 1500 V, 1000 V High Speed Inputs

APPLICATIONS

- 10 G Fibre Channel and Ethernet Designs
- 10 GbE with FEC
- 10 G SONET/SDH/FEC Designs
- SONET/SDH Test Equipment
- SONET/SDH/FEC DWDM Equipment
- XFP MSA Modules

GENERAL DESCRIPTION

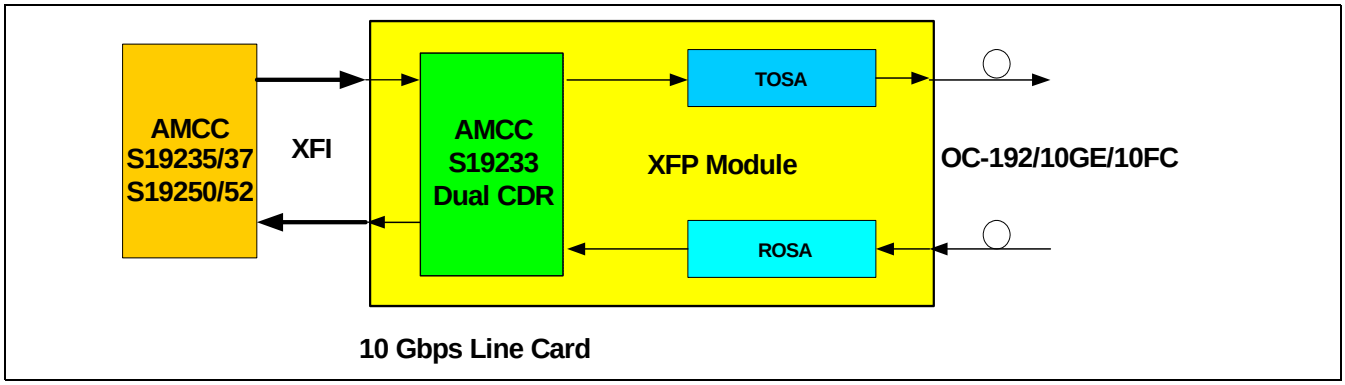
The S19233 is a fully integrated low power dual CDR device with Electronic Dispersion Compensation (EDC). It is suitable for use in 10 GbE/10G FC/ SONET/SDH PMD modules, such as the XFP MSA modules. This device can be used to compensate channel impairments caused by either single mode fiber up to 100 km or FR-4 copper medium over 24”. Integrated in this device on the receive optical side, an AGC amplifier with offset cancellation circuitry, EDC/ Equalization with control circuitry, and CDR. On the transmit electrical side the S19233 also has an equalization circuit, and CDR that reshapes the data after up to 24" of transmission over copper on FR-4 PWB material. The low-jitter CML interfaces guarantees compliance with the bit error rate requirements of the Telcordia and ITU-T standards. The S19233 is packaged in a 6 mm by 6 mm PBGA, offering designers a small package outline.

Value Proposition - Design multiple XFP modules ranging from 2 km to 120 km link with one footprint. The S19233 is pin and software compatible to the EDC based 10G Dual CDR S19256.

S19256: 2 km-40 km;

S19233: 40 km-120 km

Figure 1. System Block Diagram



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S19233 OVERVIEW

The S19233 can be used to implement the front end of SONET/SDH/FEC/10GbE/FC/G.709 equipment which consists primarily of the serial transmit interface and the serial receive interface. The system timing circuitry consists of a high-speed phase detector, clock and data recovery unit and equalization circuitry. The device utilizes on-chip clock recovery PLL components that allow the use of a slower external clock reference, 155.52 MHz (or equivalent FEC/10GbE/ 10 Gbps FC rate), in support of existing system clocking schemes.

The EDC function is embedded in the optical receive side. It provides control to compensate chromatic dispersion in different fiber links. On the transmitter side, an equalizer is integrated in the receive front end to reshape the data after transmission over FR-4. This enables low bit error rate and transmission over longer trace length.

The low-jitter, 1-bit, CML interfaces guarantee compliance with the bit-error rate requirements of the Telcordia and ITU-T standards. The 10 Gbps serial electrical interface specifications are compliant with the XFI as specified in the XFP MSA module specification. The high speed serial input and output can be connected to the AMCC SerDes (S19235 or S19237) across 600 mm (24”) of improved FR-4 material or across 400 mm of standard FR-4 with one connector.

Table 2 shows the suggested interface device(s) for the S19233.

Table 1. Standard Compliance List

Standard	Revision	Date
XFP - 10 Gigabit Small Form Factor Pluggable Module	4.0	4/13/04
T1.105.03 - 2002 SONET Jitter Tolerance specification	-	08/2002
GR-253-CORE	3.0	09/2000
GR-253-ILR- Sonet Jitter Specifications	Issue 3A	10/2000
G.825 SDH Jitter Tolerance specification	-	03/2000
G.783 Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks	-	02/2004
IEEE 802.3ae	-	8/30/2002
X3.T11 FC-PH-3 10 G	Rev 0	5/2003
ESD - JEDEC standard: JESD22-A114-B	Rev B	6/2000

Note: Standards compliance only relates to applicable sections pertaining to this product type.

Transmitter Side Operations

1. 1-bit serial data input
2. Equalization to compensate for FR-4
3. Threshold and Offset cancellation adjust
4. Clock and Data recovery
5. Data retime
6. Serial data output

Receiver Side Operations

1. Serial input with AGC (Equalization)
2. 10 mV_{pp} Differential Sensitivity with threshold adjust
3. Loss of signal detection
4. Clock and Data recovery
5. Serial data output

Common Operations

1. Optical and Electrical Loopbacks
2. Power Down CDR

Table 2. AMCC Suggested Interface Devices

AMCC	S19235	SFI4 Phase 1 SONET/SDH STS-192/10 Gig Ethernet CMOS Transceiver with ISI Compensation
AMCC	S19237	SFI4 Phase 1 SONET/SDH STS-192/10 Gig Ethernet CMOS Transceiver with ISI Compensation

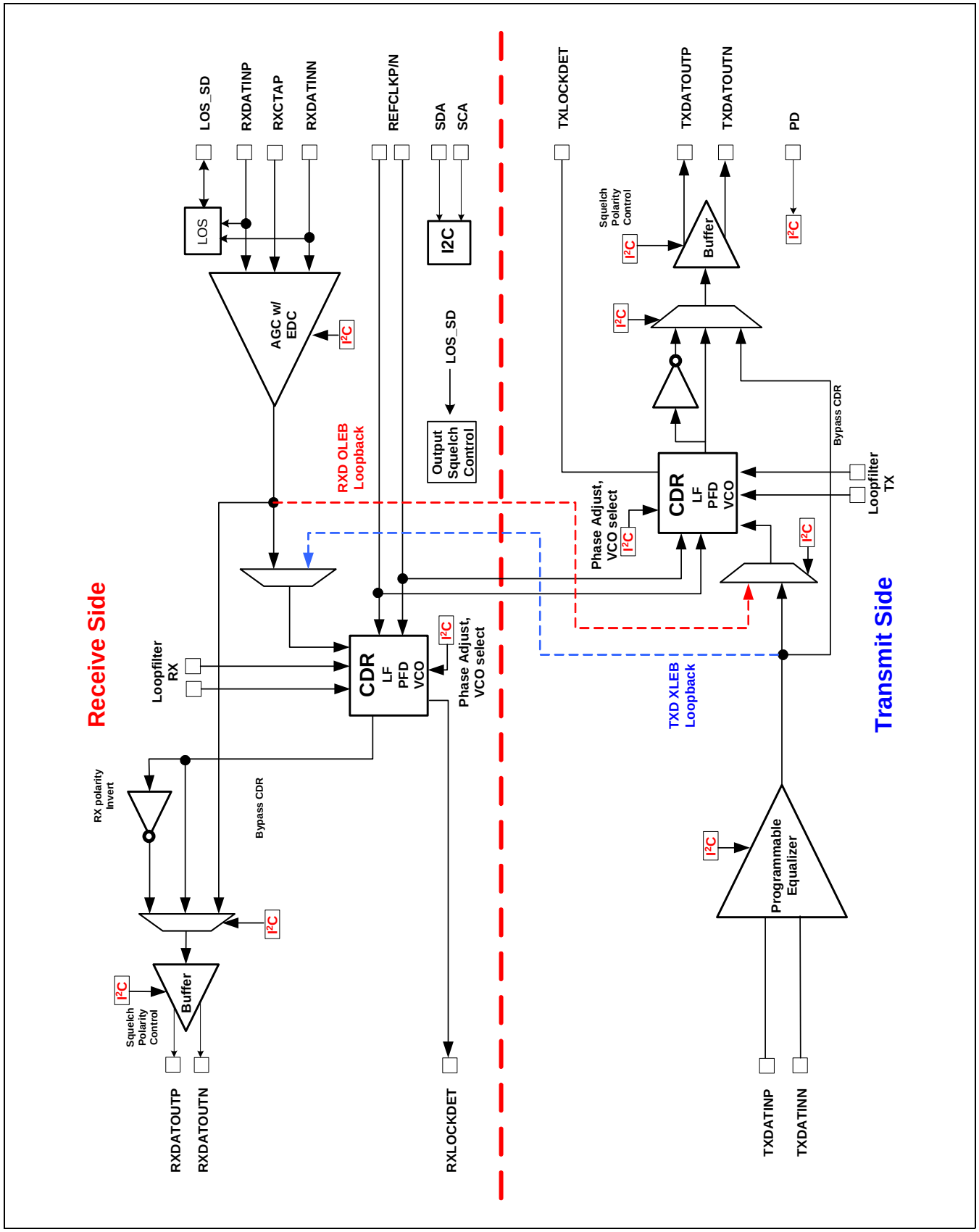
POWER UP SEQUENCE

This Power Up Sequence provides details for the required reset sequence to initialize the S19233 following power on or system reset.

3. Apply the reference clock to pin **REFCLKP/N**
4. Set pin **PD** high for at least two clock cycles then set low to initiate initialization and for normal operation.

The initialization will complete in 13 clock cycles following the falling edge of the *PD* signal. The *PD* signal must remain low for normal operation.

Figure 2. S19233 Dual CDR Block Diagram



RECEIVE OPTICAL SIDE – DESCRIPTION

The receive side of the S19233 dual CDR device provides an important EDC function to compensate chromatic dispersion for 10 Gigabit Ethernet/10 G Fibre Channel/SONET STS-192 transmitted over single mode fiber. It reshapes the received signal waveform and amplifies the signal to an optimal signal level so that the receive side CDR can achieve optimum performance.

Analog Front End

An AGC gain stage with offset adjust capability is at the first input stage. The S19233 AGC stage takes the differential serial data from the RXDATINP/N pins. There is a center-tap pin, RXCTAP, that provides a flexible solution for a single-ended input configuration. The input to this stage must be AC coupled.

Clock Data Recovery

Clock Data recovery (CDR), as shown in the block diagram in Figure 2, S19233 Dual CDR Block Diagram, recovers a clock that is the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a Phase Lock Loop (PLL) so that it samples the data in the center of the data eye pattern.

The Clock Data Recovery Unit (CDR) extracts a synchronous signal from the serial data input using a PLL. The PLL consists of a Voltage Controlled Oscillator (VCO), Phase/Frequency Detectors (PFD), and a loop filter.

The frequency detector ensures predictable lock-up conditions. It is used during acquisition and serves as a means to pull the VCO into the range of the data rate where the phase detector is capable of acquiring lock.

The phase detector used in the CDR is designed to give minimum static phase error of the PLL. When a transition has occurred, the value of the sample in the vicinity of the transition indicates whether the VCO clock leads or lags the incoming data, and the phase detector produces a binary output accordingly.

When a loss of signal condition exists, the PLL locks onto the reference clock (REFCLKP/N) to provide a steady output clock. The output data is invalid and can be squelched.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter (LF). The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by the reference input (REFCLKP/N) onto which the PLL locks when data is lost. If the frequency of the incoming signal varies by a value greater than that stated in Table 13, with respect to REFCLKP/N, the PLL will be declared out of lock, and the PLL will lock to the reference clock.

The loop filter transfer function is optimized in order to enable the PLL to track the jitter yet tolerate the minimum transition density expected in a received 10 Gigabit Ethernet, 10 G Fiber Channel and SONET data signal. There are two pins (RXCAP1 and RXCAP2) to connect the external capacitor and resistors in order to adjust the PLL loop performance.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by the Telcordia standard.

Receive Signal Lock Detect

The S19233 contains a lock detect circuit that monitors the integrity of the serial data inputs. If the received serial data fails the frequency test as describe previously, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss-of-signal or loss-of-lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than the typical value stated in Table 13, Performance Specifications, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within the typical value stated in Table 13, Performance Specifications, the PLL will be declared in lock and the lock detect output will go active. An inactive Signal Detect (SD) setting will also cause an out-of-lock condition.

Receiver Output Polarity Invert

The output data polarity swap is implemented for the ease of design. This adds routing flexibility for either top or bottom PCB placement of IC or optics compatibility.

When the RX_POLINV is set high through the I^2C interface, the polarity of the receiver output is inverted.

Receiver Output Squelch

The output data squelch functions are controlled through the I2C BUS® interface. RX_SQ_POL determines the polarity of the receive squelch data and RX_SQ_EN is the control bit used to enable or disable the squelch feature. The RX_SQ_CNTL bit is a receiver squelch control bit. See Table 3 for details.

Table 3. Receive Squelch Control

RX_SQ _EN	*RX_SQ _CNTL*	*RX_SQ[1:0]*	Function
1	0	XX	Squelch RX data
1	1	00	LOS_SD (LOS) output controls the squelch
1	1	01	RXLOCK signal controls the squelch. The LOS condition will also trigger RXLOCK.
1	1	10	LOS_SD (SD) input control the squelch
1	1	11	(1) RX squelch function is controlled by LOS or RXLOCK (Default: LOS_SDC is active high) (2) RX squelch function is controlled by SD or RXLOCK if LOS_SD is low
0	X	XX	Disable squelch feature for RX

RECEIVE OPTICAL SIDE – CONTROL DESCRIPTION

Receive Serial Data In (RXDATINP/N) – External Pin

The Receive Data In (RXDATIP/N) pins are differential Current Mode Logic (CML) inputs. They receive inputs from an optics module or other upstream logic device. The RXDATIP/N is internally terminated with two 50 Ω resistors in series. The two 50 Ω resistors are center-tapped with a 25 pF capacitor for use in single-ended applications.

The RXDATIP/N inputs must be AC coupled. These pins are internally biased and terminated 100 Ω line-to-line.

RXDATIP/N Internal Center-Tapped Termination (RXCTAP) – External Pin

The RXDATIP/N is internally terminated with two 50 Ω resistors in series. The two 50 Ω resistors are center-tapped with a 25 pF capacitor. The input to the capacitor can be directly accessed through the RXCTAP pin. This input should be connected to a broadband 850 pF capacitor to ground when used in single-ended applications. This termination scheme enables the S19233 to be driven in the single-ended mode and offers better common-mode noise rejection. This input should be left floating if RXDATIP/N is driven differentially.

Receive Loop Filter (RXCAP1, RXCAP2) – External Pin

The CDR external loop filter capacitor and resistors are connected to the RXCAP1 and RXCAP2 pins. These devices should be surrounded by a ground shield. Component values should be as stated in Table 19, Transmit and Receive External Loop Filter Components.

Receive Lock (RXLOCK) – External Pin

RXLOCK goes active after the receive PLL has locked on the incoming data stream after initially locking onto the clock provided on the REFCLK pins. RXLOCK is an asynchronous output. The Receive Lock status is also available as *RXLOCK* register read only bit.

Receive Loss of Signal/Signal Detect (LOS_SD) – External Shared Pin

This is a dual purpose pin. This pin is configured as a Loss of Signal (LOS) pin or can be changed to a Signal Detect (SD) pin through the I^2C interface using the *LOS_SD bit*. The LOS can be programmed active high or active low by setting RX_LOS_POL bit to 1 or 0 respectively. The LOS threshold and hysteresis are adjustable via the I^2C control registers. Upon receiving

an LOS condition the PLL will lock to reference until the LOS condition is de-asserted. LOS pin is not configured as an open drain or open collector output.

The signal detect is an active high or active low LVTTL single-ended input to be driven by the external optical receiver module to indicate the presence of received optical power. Active level (high or low) is programmed by the *SDPOL*. When a loss-of-light condition occurs, an active SD will cause the internal PLL to be locked to the REFCLK input signal.

Receive Lock-to-Reference (*LCKREFRXB*) – I²C Register

Active low. Lock-to-Reference (*LCKREFRXB*) input register will force the PLL to lock to the local Reference Clock (REFCLK) when active. This bit should be set to inactive which is default, for normal operation. This input is only accessible through the I²C bus register.

Receive Signal Detect Polarity (*SDPOL*) – I²C Register

The signal detect polarity is an input bit that will set the LOS_SD input as either active high or active low when the LOS_SD bit is set inactive. Setting this pin low will set the LOS_SD input as active low. Setting this bit high will set the LOS_SD input as active high. This input is only accessible through the I²C bus register.

Receive Squelch Serial Output (RX_SQ_EN) – I²C Register

The Squelch Serial Output data enable (RX_SQ_EN), when asserted high, will enable the squelch function in the receiver.

TRANSMIT ELECTRICAL SIDE – DESCRIPTION

Programmable Equalization

The transmit front end have programmable equalization to compensate for 24 inches FR-4 applications. Equalization is necessary to compensate for bandwidth attenuation/distortions caused by the PWB.

Signal Conditioning Operation

On the Transmit side, the S19233 performs the signal conditioning stage in the processing of a transmit 10 Gigabit Ethernet/10 G Fibre Channel/SONET STS-192/ data stream. The rate will depend upon the REFCLK frequency used. A high-frequency bit clock is generated from a 155 MHz (or equivalent FEC/ 10 Gigabit Ethernet rate) frequency reference by using a clock synthesizer consisting of an on-chip phase-lock loop circuit with a divider, VCO and loop filter.

Clock Data Recovery – Transmit

The CDR shown in the block diagram in Figure 2, is a monolithic PLL that generates the serial output clock frequency locked to the input Reference Clock (REFCLKP/N) used by the receive side.

The REFCLKP/N input must be generated from a crystal oscillator which has a frequency accuracy that meets the value stated in Table 13 in order for the Transmit Serial Data (TXDATOUTP/N) frequency to have the accuracy required for operation in a SONET/ 10 Gigabit Ethernet system. The REFCLK must also meet the phase noise requirements shown in Figure 5 in order to meet the jitter generation specifications as defined in GR-253-Core, Issue 3, September 2000. Lower accuracy crystal oscillators may be used in applications less demanding than the SONET/SDH.

The on-chip PLL consists of; a phase detector, which compares the phase relationship between the VCO output and the REFCLK input, a loop filter, which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Transmit Output Polarity Invert

The output data polarity swap is implemented for the ease of design. This adds routing flexibility for either top or bottom PCB placement of IC or optics compatibility.

When the TX_POLINV is set high through the I^2C interface, the polarity of the transmitter output is inverted.

Transmit Output Squelch

The output data squelch functions are controlled through the I^2C interface. TX_SQ_POL determines the polarity of the receive squelch data and TX_SQ_EN is the control bit used to enable or disable the squelch feature. The TX_SQ_CNTL bit is a transmit squelch control bit. See Table 4 for details.

Table 4. Transmit Squelch Control

TX_SQ_EN	*TX_SQ_CNTL*	Function
0	X	Disable Squelch
1	0	Squelch TX data
1	1	Default mode. TXLOCK signal controls the squelch.

TRANSMIT ELECTRICAL SIDE – CONTROL DESCRIPTION

Transmit Serial Data In (TXDATIP/N) – External Pin

The Transmit Data In (TXDATIP/N) pins are differential Current Mode Logic (CML) inputs. They receive inputs via a PWB trace which can be up to 10 inches in length. The TXDATIP/N is internally terminated with two 50 Ω resistors in series. The two 50 Ω resistors are center-tapped with a 850 pF capacitor for use in single-ended applications.

The TXDATIP/N inputs must be AC coupled. These pins are internally biased and terminated 100 Ω line-to-line.

Transmit Loop Filter (TXCAP1, TXCAP2) – External Pin

The CDR external loop filter capacitor and resistors are connected to the TXCAP1 and TXCAP2 pins. These devices should be surrounded by a ground shield. Component values should be as stated in Table 19, Transmit and Receive External Loop Filter Components.

Transmit Lock (TXLOCk) – External Pin

TXLOCK goes active after the transmit PLL has locked on the incoming data stream after initially locking onto the clock provided on the REFCLK pins. TXLOCK is an asynchronous output. The Transmit Lock status is also available as *TXLOCK* read only register bit.

Transmit Lock-to-Reference (*LCKREFTXB*) – I^2C Register

Active low. Lock-to-Reference (*LCKREFTXB*) will force the PLL to lock to the local Reference Clock (REFCLK) when active. This bit should be set to inactive which is default, for normal operation. This input is only accessible through the I^2C bus register.

Transmit Squelch Serial Output (TX_SQ_EN) – I^2C Register

Squelch Serial Output data enable (TX_SQ_EN), when asserted high, will enable the squelch function in the transmitter.

Reference Clock (REFCLKP/N) – External Pin

The Reference Clock (REFCLKP/N) pins are Differential CML 155.52 MHz to 177 MHz input used to establish the initial operating frequency of the clock recovery Phase Lock Loop (PLL) and is also used in the absence of data to maintain PLL lock. Table 5 summarizes the REFCLK rates used in typical applications. This input is internally biased and terminated 100 Ω line-to-line and must be AC coupled. Additionally, Table 5. shows the corresponding RX and TX register configured VCO selections for the frequency of operation. See *S19233 Programming Manual* for additional information on RX and TX VCO selection.

Table 5. Reference Frequency for the Clock Recovery Unit

Error Correcting Capability	Percentage Bandwidth Expansion Due to Code Words and Frame Synchronization Byte (FSB)	Increased Receive Data Input (SERDATI) Frequency	Required (REFCLK) Frequency	RX_VCO_SEL[1:0]/ TX_VCO_SEL[1:0]
STS-192, 0 bytes	0% increase	9.953 Gbps	155.52 MHz	01
STS-192, Reed Soloman - 255/238	7.14% increase	10.66 Gbps	166.63 MHz	10
STS-192, Reed Soloman - 255/237	7.59% increase	10.709 Gbps	167.33 MHz	10
10 Gigabit Ethernet	0% increase	10.000 Gbps	156.25 MHz	01
10 Gigabit Ethernet 64/ 66B Encoded	3.125% increase	10.3125 Gbps	161.13 MHz	01
10 Gigabit Ethernet 64/ 66B Encoded - 255/238	7.14% increase	11.0491 Gbps	172.642 MHz	11
10 Gigabit Ethernet 64/ 66B Encoded - 255/237	7.59% increase	11.0957 Gbps	173.37 MHz	11
10 G Fibre Channel	0% increase	10.51875 Gbps	164.35 MHz	10
10 G Fibre Channel, Reed Soloman - 255/238	7.14% increase	11.27 Gbps	176.095 MHz	11
10 G Fibre Channel, Reed Soloman - 255/237	7.59% increase	11.32 Gbps	176.84 MHz	11

PD – External Pin

Powerdown/Reset pin. This is a dual purpose pin. Active high. Default low, when high, power downs the Transmitter and Receiver. The I2C interface and reset generation logic is functional during power-down with REFCLK supplied. The falling edge initiates a complete reset of TX/RX including 2-wire serial interface. The reset function asynchronously resets the device.

Electrical Diagnostic Loopback Enable (XLEB) – I^2C Register

The XLEB is an active low input that selects the diagnostic loopback mode. In this mode, the Transmitter Data (TXD) is routed internally to the receive side. The serial data is recovered by the receive CDR then send back out the electrical side through pin RXDATOUTP/N. This mode is accessible through the I^2C bus register.

Optical Side Line Loopback Enable (OLEB) – I^2C Register

This active low input selects line loopback mode. In this mode, the Receiver Data (RXD) from the receive side is routed internally to the transmit side. The serial data is recovered by the transmit CDR then send back out the optical side through pin TXDATOUTP/N. This mode is accessible through the I2C BUS® register.

I2C BUS® and Address Register

S19233 uses a simple bi-directional two-wire bus for efficient inter-IC control. All register controlled features and functions are programmed via the I²C. Table 11summarizes the register map and description necessary for proper operation. A more detailed description can found in the S19233 Programmer's Reference Manual, PRM2001.

The following are some important features of I²C bus:

- The S19233 has a unique address on the bus and a slave configuration at all times.
- Only two bus lines are required; a serial Data Input/Output line (SDA) and a Clock line (SCL).

The serial port interface is based on the I²C. Communication occurs across two wires and is formatted in frames. The two wires are clock (SCL) and data (SDA). At the rising edge of RSTB, the S19233 loads the device address into a register from the DEVICE_ADDR[6:0] and uses it to decode accesses to its registers. The DEVICE_ADDR[6:0] default is fixed at 51h. The address bits are used to uniquely identify the S19233 device if multiple I²C devices are controlled by a single microprocessor. A more detailed I²C interface description can found in the S19233 I²C Interface Application Note, AN2076.

A frame is formatted as shown in Figure 3.

I²C Start/Repeat Conditions: A falling edge on SDA during SCL high time.

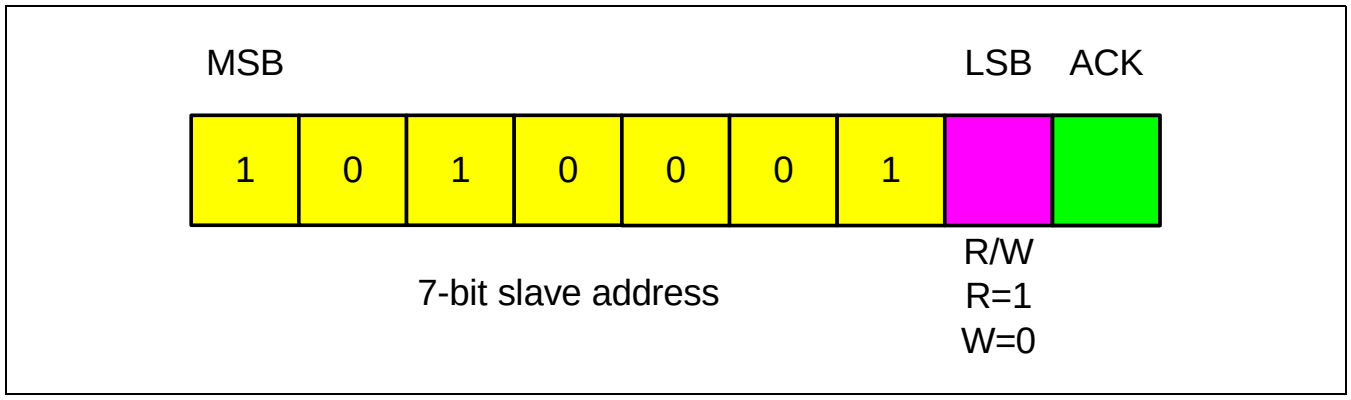
I²C Acknowledge: A low assertion on the SDA line from the receiver after a data transfer.

I²C Not Acknowledge: A high left on the SDA line by the receiver after a data transfer.

Stop Code: A rising edge on SDA during SCL high time. After this condition, the bus becomes tristated, and both SDA and SCL are pulled high.

REFCLKP/N must be supplied continuously in order to access read/write registers through the I²C interface.

Figure 3. Two Wire Slave Address



SONET AND ETHERNET JITTER CRITERIA

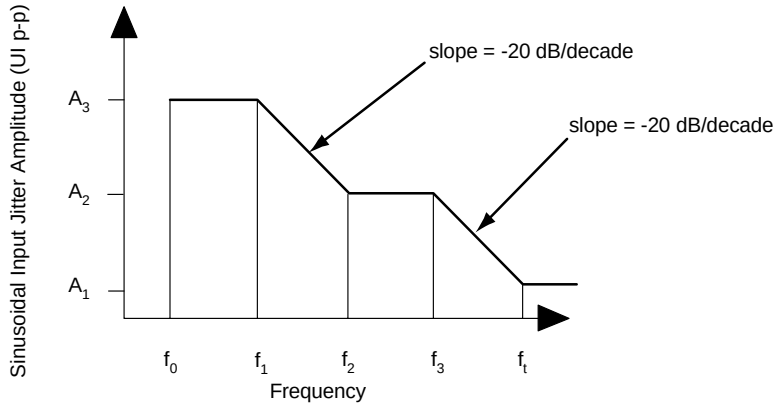
SONET Jitter Transfer

The following jitter transfer requirement applies to STS-192 interfaces as defined in GR-253-Core. For STS-192 interfaces, the jitter transfer function shall meet specifications in Table 13 when input sinusoidal jitter up to the jitter tolerance mask level in Figure 4 is applied.

SONET Jitter Tolerance

The following jitter tolerance requirement applies to STS-192 interfaces as defined in GR-253-Core. STS-192 interfaces shall tolerate, as a minimum, input jitter applied according to the mask in Figure 4.

Figure 4. SONET STS-192 Jitter Tolerance Mask



OC-N Level	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_3 (kHz)	f_t (kHz)	A_1 UI_{PP}	A_2 UI_{PP}	A_3 UI_{PP}
OC-192	10	2k	20k	400	4000	0.15	1.5	15

SONET Jitter Generation

The following jitter generation requirement applies to STS-192 interfaces as defined in GR-253-CORE.

According to GR-253-CORE, jitter generation shall not exceed 0.10 UI_{PP} for STS-192 interfaces when measured using a bandpass measurement filter with a high-pass cutoff frequency of 50 kHz and a low-pass cutoff frequency of at least B3 = 80 MHz.

Note that for SONET rates up to STS-48, the current jitter generation requirement in GR-253-CORE states that the generated jitter must be less than 0.01 UI_{rms} and 0.10 UI_{PP}. At the STS-192 rate, the measurement of RMS phase variations with less than 0.01 UI granularity (1 picosecond) may not be feasible. Therefore, this requirement specifies the jitter generation only in terms of 0.10 UI_{PP}.

The S19233 exceeds the Telcordia Jitter Generation Specification by having less than 50% of the budget in normal modes of operation.

10 Gigabit Ethernet Jitter Tolerance

The following 10 Gigabit Ethernet jitter tolerance requirement applies to 10GBASE-ER as defined in IEEE Std 802.3ae. This total jitter is composed of three components: deterministic jitter; random jitter; and an additional sinusoidal jitter.

The three fundamental components of Jitter Tolerance testing are:

- Input Jitter (Dj and Rj)
- Sinusoidal Jitter
- Test Pattern (Test patterns are different for 10GBASE-R and 10GBASE-W)

Input Jitter (amount of Dj and Rj)

Dj: 0.35 UI_{pp}

Rj: 0.015 UI_{rms}

The random jitter (Rj) component of the input signal has uniform spectral content over the measurement frequency range of at least 1 MHz to 1 GHz. Input Signal must pass the bathtub curves between BERs of 10^{-6} and 10^{-12} as shown in Figure 5.

Sinusoidal Jitter

The Sj applied for tolerance testing is defined by the jitter mask shown in Figure 6 and Table 6 (per section IEEE Std 802.3ae). The Loop Bandwidth (LB) for S19233 is approximately 8 MHz.

Test Pattern

Test pattern is chosen per IEEE Std 802.3ae Section 52.9.1. The test pattern is a static pattern and can be loaded into a BERT. IEEE Std 802.3ae specifies two pseudo-random test patterns for 10GBASE-ER testing. One pattern represents typical scrambled data while the other represents a less typical pattern which could happen by chance and is thought to be more demanding of the transmission process including the clock recovery sub-system. Both patterns are balanced over their length of 33792 bits.

Test pattern is constructed from 4 Segments

- 1 segment is constructed with 128 Blocks
- 1 block is 2 Sync Bits and 64 Payload Bits
- Pay load bits are generated with the scrambler shown in Figure 7.
- Scrambler seeded per Table 7 and Table 8.
- Data input is set to 1 or 0.

Figure 5. Input Jitter for Receiver Test

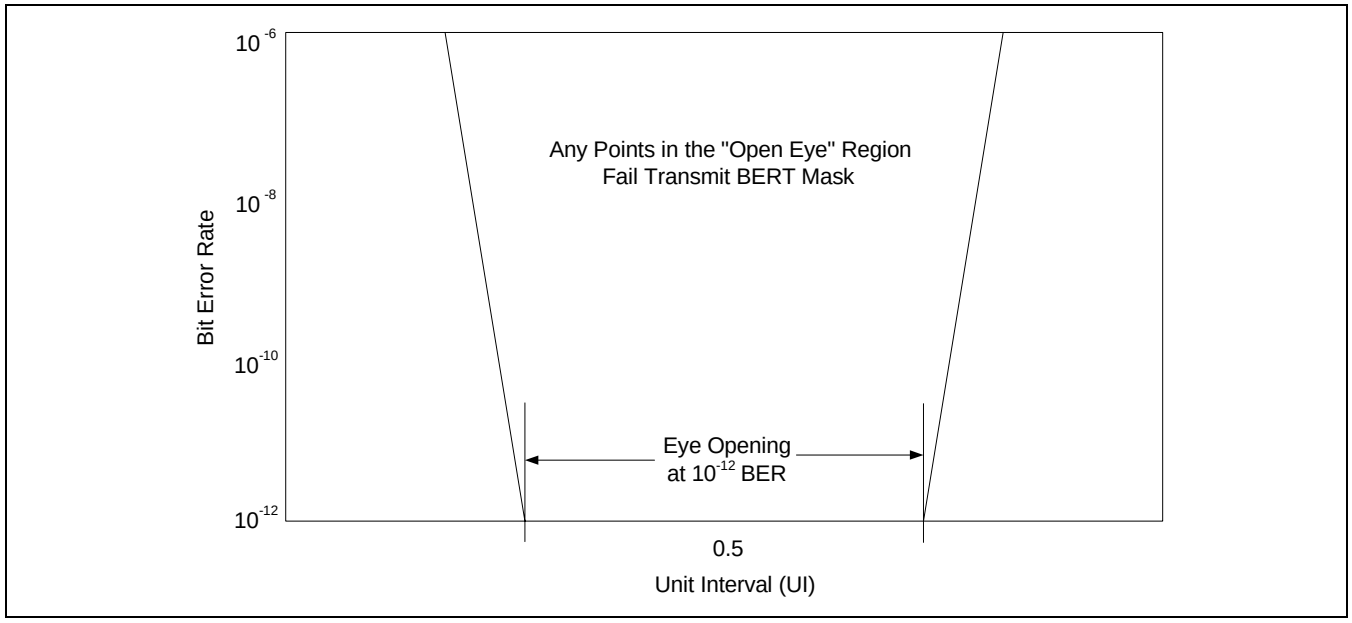


Figure 6. Applied Sinusoidal Jitter - 10GbE

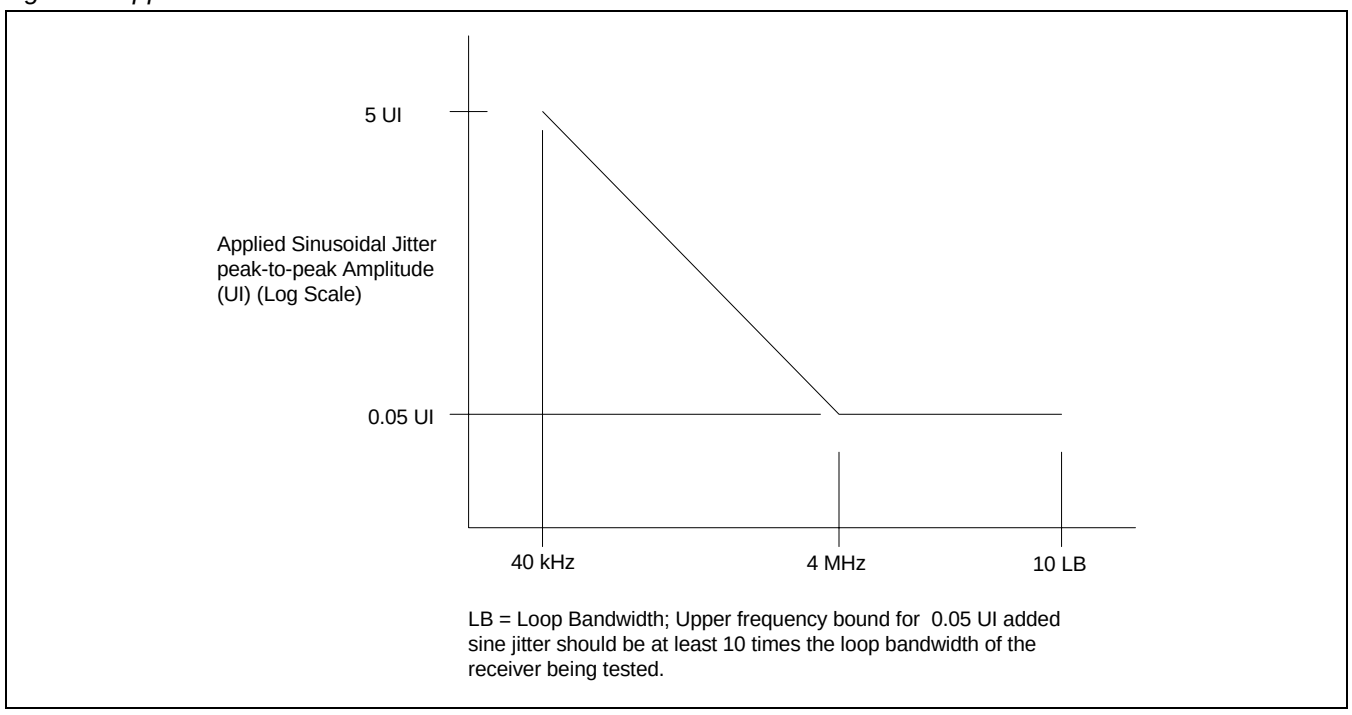


Table 6. Applied Sinusoidal Jitter

Frequency Range	Sinusoidal Amplitude Jitter (UI Peak to Peak)
f < 40 kHz	NA
40 kHz < f < 4 MHz	$(2 \times 10^5)/f$
4 MHz < f < 10 LB	0.05

Figure 7. Scrambler and Descrambler

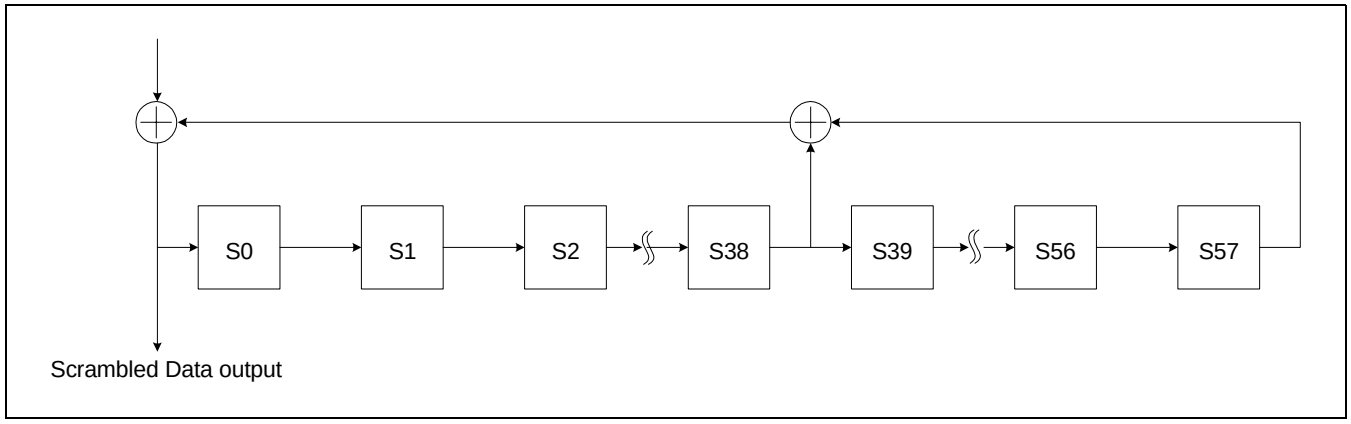


Table 7. Pattern Segments

Segments	Seed [57:0]
A_n	0x3C8B44DCAB6804F
B_n	0x34906BB85A38884
A_i	Inverted Seed for A_n
B_i	Inverted Seed for B_n

Table 8. Test Patterns

Pattern	Sequence of Segments
1	$B_n\ B_i\ B_n\ B_i$
2	$A_n\ A_i\ A_n\ A_i$

PIN ASSIGNMENTS AND DESCRIPTIONS

Table 9. Signals Pin Assignments and Descriptions

Pin Name	Level	I/O	Pin#	Description
TRANSMITTER SIGNALS				
TXDATINP TXDATINN	High Speed Diff CML	I	G7 G6	**Transmit Serial Data Input.** Differential high speed serial data input for transmitter. Internally terminated 100 Ω line-to-line (50 Ω + 50 Ω with center tap capacitor). This input must be AC coupled. Clock is recovered from transitions on these inputs.
TXCAP1 TXCAP2	Analog	I	D7 C7	**Transmit Loop Filter Capacitors**. Connections for external loop filter capacitors and resistors. See Figure 14, External Loop Filters, and Table 19, Transmit and Receive External Loop Filter Components.
TXLOCK	3.3 V LVTTL	O	E6	**Transmit Lock**. Active High. Goes active after the transmit PLL has locked on the incoming data stream after initially locking onto the clock provided on the REFCLK pins. TXLOCK is an asynchronous output.
TXDATOUTP TXDATOUTN	High Speed Diff CML	O	A5 A6	**Transmit Serial Data Output**. Serial data stream signals, normally connected to an optical transmitter module. Output return loss, S_{22} of -12dB at 15 GHz.
RECEIVER SIGNALS				
RXDATINP RXDATINN	High Speed Diff CML	I	A1 A2	**Receive Serial Data Input.** Differential high speed serial data input for receiver. Internally biased and terminated 100 Ω line-to-line (50 Ω + 50 Ω with center tap capacitor). This input must be AC coupled.
RXCTAP	Analog	I	C2	**Center Tap Input.** This input should be connected to a broadband 850 pF capacitor to ground.
RXCAP1 RXCAP2	Analog	I	D1 E1	**Receive Loop Filter Capacitors**. Connections for external loop filter capacitors and resistors. See Figure 14, External Loop Filters, and Table 19, Transmit and Receive External Loop Filter Components.
LOS_SD	3.3 V LVTTL Pull-up	I/O	F4	Dual purpose pin - **Loss of Signal Output for Receiver or Signal Detect Input for Receiver.** Active High. Goes active after the receiver fail to sense the incoming data stream. This Loss of Signal is an asynchronous output. When LOS_SD register is set to 0 via I^2C, this pin becomes the Signal Detect Input for Receiver. **Signal Detect Input for Receive**. active HIGH default. May be adjusted to be active low with I^2C control. Signal to be driven by the external optical receiver module to indicate sufficient received optical power. When inactive the RX PLL will be forced to lock to the REFCLKP/N inputs and the data will be forced to a logical '0' or 1' state depending on the polarity of SQ_POL signal and squelch enable feature.
RXDATOUTP RXDATOUTN	High Speed Diff CML	O	G3 G2	**Serial data output for Receiver**.
RXLOCK	3.3 V LVTTL	O	C4	**Receive Lock**. Active High. Goes active after the receive PLL has locked on the incoming data stream after initially locking onto the clock provided on the REFCLK pins. RXLOCK is an asynchronous output.

Table 9. Signals Pin Assignments and Descriptions (Continued)

Pin Name	Level	I/O	Pin#	Description
COMMON Signals				
PD/RSTB	LVCMOS pull-down	I	D3	**Powerdown/Reset**, active HIGH input. Default Low, when high, power downs the Transmitter and Receiver. 2-wire Serial (I2C) interface and reset generation logic is functional during power-down.The falling edge initiates a complete reset of TX/RX including 2-wire serial interface.
REFCLKP REFCLKN	LVPECL	I	E5 E4	**Reference Clock**. 155.52 MHz (or equivalent FEC/10 GE/10 G FC frequency) input used as the reference for the internal bit clock frequency synthesizer for both receive and transmit reference clock. This input is internally biased and terminated. This input must be AC coupled. REFCLKP/N must be supplied continuously in order to access read/write registers through the I2C interface.
SDA SCL	I2C BUS®	I/O I	C5 C3	**I²C BUS®.** Bi-directional 2-wire bus for efficient inter-IC control. This bus reads from and writes into most of the S19233 control logic.
SCANMODE	LVTTL Pull-down	I	E3	**Scan Logic Input. Active High.** Bring device into scan mode. Default low for normal operation.

Table 10. Common Pin Assignments and Descriptions

Pin Name	Level	I/O	Pin #	Description
AVDD_TX	+1.8 V		B7, E7	Transmit analog power supply
AVDD_RX	+1.8 V		C1, F1	Receive analog power supply
VDD_TX	+1.8 V		B5, B6	Transmit CML power supply
VDD_RX	+1.8 V		F2, F3	Receive CML power supply
VDD_PA_TX	+1.8 V		F5, F6	Transmit PA power supply
VDD_PA_RX	+1.8 V		B2, B3	Receive PA power supply
VDD_CMOS	+1.8 V		D4	CMOS power supply
VDD_33IO	+3.3 V		B4	I/O power supply
VSS	GND		A3, A4, A7, B1, C6, D2, D5, D6, E2, F7, G1, G4, G5	Ground

I2C SERIAL CONTROL INTERFACE REGISTER MAP SUMMARY

Table 11 below contains the register map summary for the S19233. For detailed register descriptions, please consult the S19233 - Programmer's Reference Manual: PRM2001. When programming the S19233 device, care should be take to preserve the default state of all RESERVED register bits - see note below.

Register Access Type Definitions

- RW = Read/Write Access
- RO = Read Only Access
- N/A = Access Type Not Applicable

Table 11. Register Map Summary

Address (hex)	Default Value[a]	Bit Field	Register Name	Mode	Description
0x00	-	7:0	RESERVED	N/A	RESERVED
0x01	0001 0111	4	SDPOL	RW	Signal Detect Polarity for *LOS_SD* (Active High)
		2	LOS_SD	RW	*LOS_SD* Pin Configured as LOS or SD (LOS)
		1	XLEB	RW	XFI (Electrical Side) Line Loopback (Disabled)
		0	OLEB	RW	Optical (Optical Side) Line Loopback (Disabled)
0x02	0001 100x	7	RX_CDRBYC	RW	RX CDR Bypass (Disabled)
		5	RX_POLINV	RW	RX Output Polarity Invert (Non-Inverted)
		4	RX_I2CRSTB	RW	RX Reset (Disabled)
		3	LCKREFXB	RW	Force RX to Lock to Reference (disabled)
		0	RXLOCK	RO	RX Lock Status
0x03	0001 100x	7	TX_CDRBYC	RW	TX CDR Bypass (Disabled)
		5	TX_POLINV	RW	TX Output Polarity Invert (Non-Inverted)
		4	TX_I2CRSTB	RW	TX Reset (Disabled)
		3	LCKREFTXB	RW	Force TX to Lock to Reference (Disabled)
		0	TXLOCK	RO	TX Lock Status
0x04	0111 1011	7	RX_SQ_POL	RW	RX Squelch Polarity (Low)
		6	RX_SQ_EN	RW	RX Squelch Enable (Enabled, see Table 3)
		5	RX_SQ_CNTL	RW	RX Squelch Control (Enabled, see Table 3)
		4:3	RX_SQ	RW	RX Squelch Control (see Table 3)
		2	TX_SQ_POL	RW	TX Squelch Polarity (active low)
		1	TX_SQ_EN	RW	TX Squelch Enable (Enabled, see Table 4)
		0	TX_SQ_CNTL	RW	TX Squelch Control (see Table 4)
0x05	0000 1101	4:2	RX_CLKOFFSET	RW	RX Clock Phase Offset
0x06	-	7:0	RESERVED	N/A	RESERVED
0x07	0010 0100	5:3	RX_OUTPUT_SLEW	RW	RX Output Slew Rate Control
		2:0	TX_OUTPUT_SLEW	RW	TX Output Slew Rate Control

Table 11. Register Map Summary

Address (hex)	Default Value[a]	Bit Field	Register Name	Mode	Description
0x08	-	7:0	RESERVED	N/A	RESERVED
0x09	0101 0001	6:0	DEVICE_ADDR	RO	I^2C Device Address
0x0A	-	7:0	RESERVED	N/A	RESERVED.
0x0B	00-- ----	7	RXCOREPD	RW	RX Core Power Down (Disabled)
		6	TXCOREPD	RW	TX Core Power Down (Disabled)
0x0C	100- ----	7	RX_PA_DCOFFADJ_ON	RW	RX Automatic Offset Threshold Adjust (On)
0x0D	-	7:0	RESERVED	N/A	RESERVED
0x0E	---- 001-	3:1	RX_OUT_SWING	RW	RX Output Swing (Low Swing Mode)
0x0F	-	7:0	RESERVED	N/A	RESERVED
0x10	1000 0000	7:0	RX_PA_DCOFFSET	RW	RX Manual Offset Threshold Adjust
0x11	1--- ----	7	TX_PA_DCOFFADJ_ON	RW	TX Automatic Offset Threshold Adjust (On)
		6:5	RESERVED1[6:5][b]	RW	RESERVED1[6:5]
0x12	-	6:3	RESERVED2[6:3][b]	RW	RESERVED2[6:3]
0x13	---- 001-	3:1	TX_OUT_SWING	RW	TX Output Swing (Low Swing Mode)
0x14	-	7:0	RESERVED	N/A	RESERVED
0x15	1000 0000	7:0	TX_PA_DCOFFSET	RW	TX Manual Offset Threshold Adjust
0x16	0000 0000	7:0	RX_LOS_VTH_ASTC	RW	RX LOS Assert Threshold
0x17	0000 0001	7:0	RX_LOS_VTH_DSTC	RW	RX LOS De-assert Threshold
0x18	-	7:0	RESERVED	N/A	RESERVED
0x19	1111 0101	6	RX_LOS_POL	RW	RX LOS Polarity (Active High)
		5	RX_LOS_CNTL	RW	RX LOS Function (Enabled)
0x1A	1100 0000	6:5	RX_PA_STEP_CNTL	RW	RX Offset Threshold Adjust Step Size
		4:0	RX_EQ_CNTL_LINK_ OPT2	RW	RX Equalizer Setting
0x1B	1010 0110	4:0	RX_EQ_CNTL_LINK_ OPT1	RW	RX EDC Setting
0x1C - - 0x1E	-	7:0 ...	RESERVED	N/A	RESERVED
0x1F	xxxx xxxx	2	RX_LOS_MEM	RO	RX LOS Status
		1	RX_RSSI_HIRANGE	RO	RX RSSI High Range Indicator
0x20	xxxx xxxx	7:0	RX_PA_DCOFFADJ_ FBC	RO	RX Auto Threshold Adjust Read Back Value
0x21	xxxx xxxx	7:0	RX_RSSI	RO	RX RSSI Value
0x22 - - 0x70	-	7:0 ...	RESERVED	N/A	RESERVED

Table 11. Register Map Summary

Address (hex)	Default Value[a]	Bit Field	Register Name	Mode	Description
0x71	1100 0000	6:5	TX_PA_STEP_CNTL	RW	TX Offset Threshold Adjust Step Size
		4:0	TX_EQ_CNTL_LINK_ OPT2	RW	TX Equalizer Setting
0x72	1010 0011	4:0	TX_EQ_CNLT_LINK_ OPT1	RW	TX EDC Setting
0x73 - - 0x76	-	7:0 ...	RESERVED	N/A	RESERVED
0x77	xxxx xxxx	7:0	TX_PA_DCOFFADJ_ FBC	RO	TX AutomaticThreshold Adjust Read Back Value
0x78 - - 0xC3	-	7:0 ...	RESERVED	N/A	RESERVED
0xC4	0111 0000	7:6	VCO_SEL_CNTL	RW	RX & TX VCO Select
0xC5 - - 0xFF	-	7:0 ...	RESERVED	N/A	RESERVED

a. Default values are based on a post reset view of the register map and may differ from part to part depending on the associated register. Consult the Programmer's Reference Manual, PRM2001, for additional notes. "x" represents an unknown value as the associated register bit is configured as read only and may be dependant on a status signal or input value. "-" represents a factory fused default value based on process variation.

b. Consult the Programmer's Reference Manual, PRM2001, for register 0x11 and 0x12 RESERVED1/2 settings when using device revision S19233PBIEB.

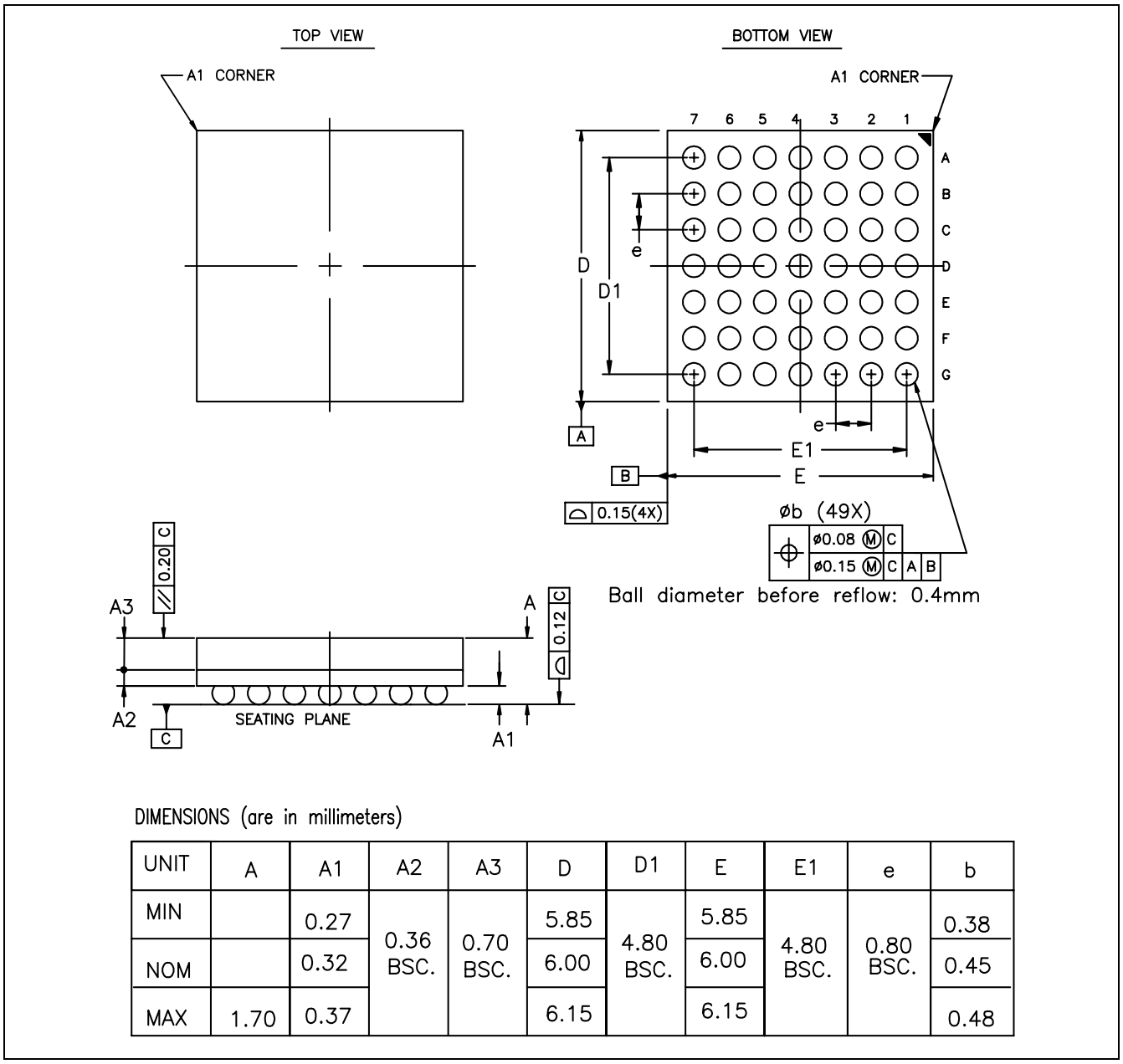
S19233 PINOUT (TOP VIEW)

Figure 8. S19233 Pinout (Top View)

	1	2	3	4	5	6	7
A	RXDATINP	RXDATINN	VSS	VSS	TXDATOUTP	TXDATOUTN	VSS
B	VSS	VDD_PA_RX	VDD_PA_RX	VDD33IO	VDD_TX	VDD_TX	AVDD_TX
C	AVDD_RX	RXCTAP	SCL	RXLOCK	SDA	VSS	TXCAP2
D	RXCAP1	VSS	PD	VDD_CMOS	VSS	VSS	TXCAP1
E	RXCAP2	VSS	SCANMODE	REFCLKN	REFCLKP	TXLOCK	AVDD_TX
F	AVDD_RX	VDD_RX	VDD_RX	LOS_SD	VDD_PA_TX	VDD_PA_TX	VSS
G	VSS	RXDATOUTN	RXDATOUTP	VSS	VSS	TXDATINN	TXDATINP

S19233 – 49 PBGA PACKAGE MECHANICAL DRAWING

Figure 9. S19233 – 49 PBGA Package Mechanical Drawing



DIMENSIONS (are in millimeters)

UNIT	A	A1	A2	A3	D	D1	E	E1	e	b
MIN		0.27	0.36 BSC.	0.70 BSC.	5.85	4.80 BSC.	5.85	4.80 BSC.	0.80 BSC.	0.38
NOM		0.32			6.00		6.00			0.45
MAX	1.70	0.37			6.15		6.15			0.48

PACKAGE MATERIAL NOTE:
Standard Package: Ball Composition - 63/37 Sn/Pb.
Green / RoHS Compliant Package: Ball Composition - 96.5/3.0/0.5 Sn/Ag/Cu.

Table 12. Thermal Management

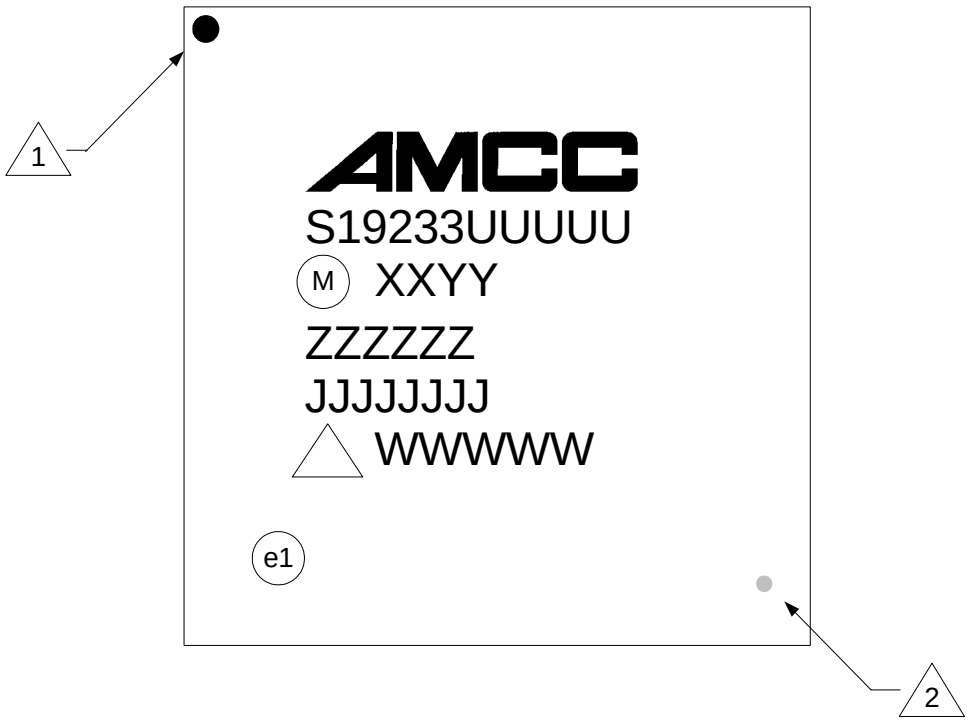
Device	Θja	Θjc
S19233	42.1°C/Watt	13.8°C/Watt

S19233 – 49 PBGA PACKAGE MARKING DRAWING

Figure 10. S19233 – 49 PBGA Package Marking Drawing (Top View)

NOTES (Unless Otherwise Specified):

1. Dot Represents PIN 1 (A01) Designator
2. Engineering Sample designator (white dot). When present, this signifies pre-production grade material. Pre-production grade material is not guaranteed to meet the specifications in this document.



LEGEND (in row order - including symbols):

ROW #1:	●	PIN 1 Designator
ROW #2:		AMCC Logo
ROW #3:		AMCC Device Part Number UUUUU: Package Option
ROW #4:	(M)	Mask Protection Symbol XX: Assembly Year Code YY: Assembly Week Code
ROW #5:		ZZZZZZ: AMCC 6 Digit Lot Code
ROW #6:		JJJJJJJJ: up to 8 Digit Subcontractor Lot Code
ROW #7:	△	ESD Symbol WWWWW: Assembly Location
ROW #8:		Engineering Sample (ES) Designator (only on Pre-Production Devices)
	(e1)	RoHS Lead Free Compliant Symbol (per JEDED-JESD97). When present, this signifies a lead free package.

PERFORMANCE SPECIFICATIONS

High-speed/low noise design practices must be implemented to meet the following performance specifications. Consult AMCC's Applications Engineering Department for recommendations regarding your specific application: support@amcc.com.

Table 13. Performance Specifications

Parameter	Min	Typ	Max	Units	Conditions
VCO					
Nominal VCO Center Frequency (both transmit and receive side)	9.953		11.1	GHz	
Upper End VCO Center Frequency (both transmit and receive side)			11.32[a]	GHZ	Consult factory for conditional restrictions
Frequency difference at which the receive PLL goes out of lock (REFCLK compared to the divided down VCO clock). LOCKDET is de-asserted when PLL goes out of lock.	±350		± 550	ppm	
Frequency difference at which receive PLL goes into lock (REFCLK compared to the divided down VCO clock). LOCKDET is asserted 0.5 ms after PLL goes into lock.	± 220		± 320	ppm	Guaranteed by design
Reference Clock					
Reference Clock Frequency Tolerance (Transmit and Receive)	-100		+100	ppm	
Reference Clock Range	155		177	MHz	
Reference Clock Rise & Fall Times for 155.52 MHz (or equivalent FEC/10 Gigabit Ethernet rate) REFCLK	0.2		1.25	ns	20% to 80% of amplitude.
Duty Cycle of Reference Clock	40		60	%	
Reference Clock Differential Input	640		1600	mV	AC coupled
CDR					
L_{CID} Consecutive identical digits at Serial Data Input			80	bits	Number of bits with no transitions (ITU-T spec is 72)
Acquisition Phase Lock Time			100	ms	After the release of RSTB, with device already powered up and with a valid REFCLK.
Transmitter Specification					
V_{IDIFF} Differential Input Sensitivity	50			mV_{pp}	PRBS31, 10^{-12} BER
V_{IDIFF} Maximum Differential Input			820	mV_{pp}	

Table 13. Performance Specifications (Continued)

Parameter	Min	Typ	Max	Units	Conditions
SDD11 (Figure 12, Point B) Differential input Return Loss	8			dB	0.1 - 5.5 GHz
	8 -20.66 $\log_{10}(f/5.5)$			dB	5.5-12 GHz
SCC11 (Figure 12, Point B) Common Mode Input Return Loss	3			dB	0.1 - 15 GHz. Common mode
SCD11 (Figure 12, Point B) Common Mode Input Return Loss	10			dB	0.1 - 15 GHz. Common mode
SDD22 (Figure 12, Point E) Differential Output Return Loss	8			dB	0.1 - 5.5 GHz
	8 -20.66 $\log_{10}(f/5.5)$			dB	5.5-12 GHz
Receiver Specification					
V_{IDIFF} Differential input sensitivity[b]		5	10	mV_{pp}	PRBS31, 10^{-12} BER, 9.953 - 10.709Gbps
		6	15	mV_{pp}	PRBS31, 10^{-12} BER, 11.1 Gbps
V_{IDIFF} Maximum differential input			2400	mV_{pp}	
$V_{ISINGLE}$ Single ended input sensitivity[b] (one wire)		5	10	mV_{pp}	PRBS31, 10^{-12} BER, 9.953 - 10.709Gbps
		6	15	mV_{pp}	PRBS31, 10^{-12} BER, 11.1 Gbps
$V_{ISINGLE}$ Single ended maximum input (one wire)			1200	mV_{pp}	
SDD11 (Figure 12, Point F) Differential input Return Loss	8			dB	0.1 - 5.5 GHz
	8 -20.66 $\log_{10}(f/5.5)$			dB	5.5-12 GHz
SCC11 (Figure 12, Point F) Common Mode Input Return Loss	3			dB	0.1 - 15 GHz. Common mode
SCD11 (Figure 12, Point F) Common Mode Input Return Loss	10			dB	0.1 - 15 GHz. Common mode
SDD22 (Figure 12, Point C) Differential Output Return Loss	8			dB	0.1 - 5.5 GHz
	8 -20.66 $\log_{10}(f/5.5)$			dB	5.5-12 GHz
SCC22 (Figure 12, Point C) Common Mode Output Return Loss	3			dB	0.1 - 15 GHz. Common mode
SCD22 (Figure 12, Point C) Common Mode Output Return Loss	10			dB	0.1 - 15 GHz. Common mode

Table 13. Performance Specifications (Continued)

Parameter	Min	Typ	Max	Units	Conditions
Transmitter Jitter					
Transmitter Jitter Generation J_{gen} for Telecom (Figure 12, Point E, 50K-80M band Jitter)		25	50	mUI_{pp}	• SONET OC-192 framed data, payload filled with PRBS23 • 9.953 & 10.709 Gbps • 50 mV differential input
Transmitter Jitter Tolerance J_{tol} for Datacom (Figure 12, Point B)	0.67 TJ			UI_{pp}	• PRBS31 • 10.3125 Gbps • 50 mV differential input
	0.075 DCD			UI_{pp}	
	0.32 DDJ			UI_{pp}	
	0.224 RJ			UI_{pp}	
	0.05 SJ			UI_{pp}	See XFP mask
Transmitter Jitter Tolerance J_{tol} for Telecom (Figure 12, Point B)	0.67 TJ			UI_{pp}	• SONET OC-192 framed data, payload filled with PRBS23 • 10.709 Gbps • 50 mV differential input
	0.075 DCD			UI_{pp}	
	0.32 DDJ			UI_{pp}	
	0.224 RJ			UI_{pp}	
	0.05 SJ			UI_{pp}	See XFP mask
Transmitter Jitter Transfer Bandwidth for Datacom (Figure 12, Point E)			8	MHz	PRBS31 or scrambled 64/66B pattern
Transmitter Jitter Transfer Bandwidth for Telecom (Figure 12, Point E)			8	MHz	PRBS31
Transmitter Jitter Transfer peaking for Datacom (Figure 12, Point E)			0.03	dB	< 50 KHz
			1	dB	> 50 KHz
Transmitter Jitter Transfer peaking for Telecom (Figure 12, Point E)			0.03	dB	< 120 KHz
			1	dB	> 120 KHz
Receiver Jitter					
Receiver Jitter Tolerance J_{tol} - 10GbE & 10GFC (Figure 12, Point F)	0.65 TJ			UI_{pp}	• SONET OC-192 framed data, payload filled with PRBS31 • 10.3125 Gbps • 50 mV differential input
	0.05 DCD			UI_{pp}	
	0.30 DDJ			UI_{pp}	
	0.25 RJ			UI_{pp}	
	0.05 SJ			UI_{pp}	See Figure 6.
Receiver Jitter Tolerance J_{tol} - SONET/SDH/G.709 (Figure 12, Point F)	0.3	0.6		UI_{pp}	SONET OC-192 framed data, payload filled with PRBS23, 9.953 Gbps and 10.709 Gbps

Table 13. Performance Specifications (Continued)

Parameter	Min	Typ	Max	Units	Conditions
Receiver Output Jitter for Datacom (Figure 12, Point C, Broadband Jitter)			0.23	UI_{pp}	10.3125 Gbps
Receiver Jitter Transfer Bandwidth for Datacom (Figure 12, Point C)			8	MHz	PRBS31 or scrambled 64/66B pattern
Receiver Jitter Transfer Bandwidth for Telecom (Figure 12, Point C)			8	MHz	PRBS31
Receiver Jitter Transfer peaking for Datacom (Figure 12, Point C)			0.03	dB	< 50 KHz
			1	dB	> 50 KHz
Receiver Jitter Transfer peaking for Telecom (Figure 12, Point C)			0.03	dB	< 120 KHz
			1	dB	> 120 KHz
Receiver LOS					
LOS Assert time			100	µS	
LOS De-assert time			100	µS	
LOS Assert Voltage	8		400	mV_{pp}	Differential (minimum run length of 4)
LOS De-assert Voltage	10		400	mV_{pp}	Differential (minimum run length of 4)

a. 11.32 Gbps operation has only been verified on a sample lot under nominal conditions. It is anticipated that operating the device near the specification limits (low voltage/high temperature) under extreme process conditions may reduce the maximum operating rate. Data sheet parameters are characterized and guaranteed up to 11.1 GHz. For operation at 11.32GHz consult factory for special consideration.

b. Peak-to-peak voltage is measured using averaged 1010...10 pattern near the center of the waveform.

Figure 11. 155.52 MHz REFCLK Phase Noise

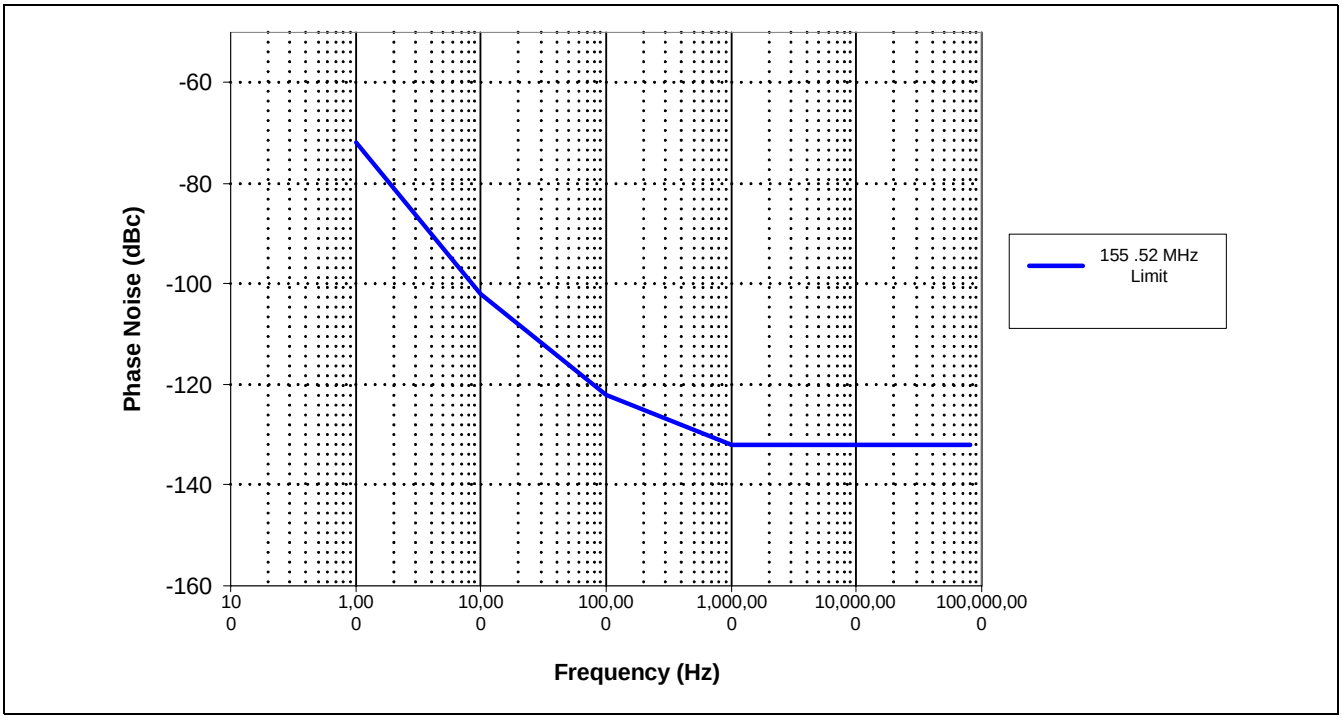
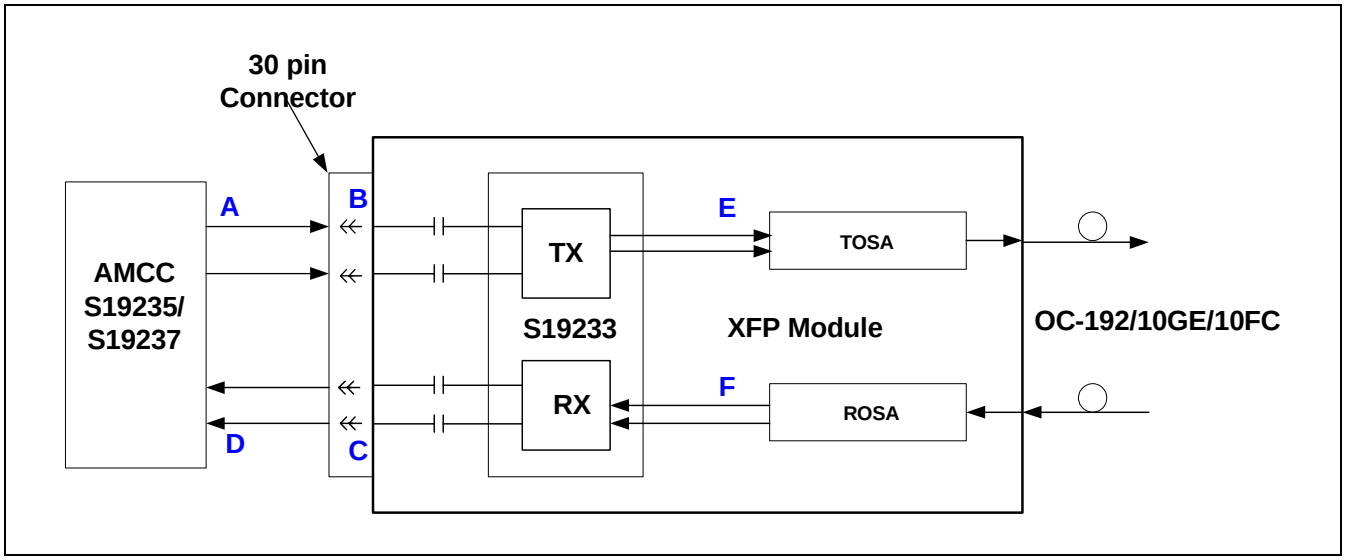


Figure 12. S19233 with XFP System Performance Points



ELECTRICAL CHARACTERISTICS

Table 14. Absolute Maximum Stress Ratings

The following are the absolute maximum stress ratings for the S19233 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only, and operation of the device at the maximums stated, or any other conditions beyond those indicated in the “Recommended Operating Conditions” of the document, are not inferred. Exposure to absolute maximum rating conditions will affect device reliability.

Parameter	Symbol	Min.	Max.	Units	Conditions
Storage Temperature Range	T_{STG}	-55	+150	°C	
1.8 V Supply	$V_{DD\_1.8}$	1.65	1.95	V	
3.3 V Supply	$V_{DD\_3.3}$	3.03	3.56	V	
Voltage on High Speed CML Input Pin			2400	mV	Differential
Voltage on Low Speed CML Input Pin			1600	mV	Differential
Voltage on any LVCMOS Input Pin			$V_{DD\_3.3}$+0.5	V	
Voltage on any LVTTL Input Pin			$V_{DD\_3.3}$+0.3	V	
LVTTL Output Sink Current			3	mA	
LVTTL Output Source Current			4	mA	

Electrostatic Discharge (ESD) Sensitivity Rating - Human Body Model (HBM):
The S19233 is rated to the following ESD voltages based upon JEDEC standard: JESD22-A114-B
1. CLASS 1C- All pins are rated at or above 1500 volts except high speed I/O pins which are only rated to 1000 volts.
Adherence to standards for ESD protection should be taken during the handling of the devices to ensure that the devices are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, "Protection of Electrical and Electronic Parts, Assemblies and Equipment." Contact your local FAE or sales representative for applicable ESD application notes.

Table 15. Recommended Operating Conditions

The device will meet all electrical specifications at a junction temperature under bias of 125C but part lifetime and reliability may be reduced. It is recommended that prudent thermal management techniques are used to maximize device lifetime.

Parameter	Min.	Typ	Max.	Units	Conditions
Ambient Temp under Bias	-40		+85	°C	Industrial Temp. Range
Junction Temp under Bias			+125	°C	
Voltage on 1.8 V Supply	1.71	1.80	1.89	V	(± 5%) wrt GND
Current on 1.8 V Supply		380	425	mA	
Voltage on 3.3 V Supply	3.135	3.3	3.465	V	(± 5%) wrt GND
Current on 3.3 V Supply			7	mA	
Power		740	820	mW	Typical supply voltages. Max power of 650 mW with LOS turned off.
Power Supply Noise Rejection			36	mV_{pp}	1.8V supply (50 KHz - 1 MHz)
			54	mV_{pp}	1.8V supply (1 MHz - 10 MHz)
			66	mV_{pp}	3.3V supply (50 KHz - 1 MHz)
			99	mV_{pp}	3.3V supply (1 MHz - 10 MHz)

Table 16. Serial I/O Interface Specifications

Parameter	Description	Min	Typ	Max	Units	Conditions
Transmitter CML Output						
V_{ODIFF}	Serial Output Differential Voltage Default - Low swing High swing	 400 700		 700 1200	mV_{pp}	Output loading is 100 Ω line-to-line.
t_r & t_f (20-80%)	Rise and Fall Times	24		35	ps	20-80%
R_{ODIFF}	Differential Output Impedance[a]	80	100	120	Ω	Over process, voltage and temperature range.
Receiver CML Output						
V_{ODIFF}	Serial Output Differential Voltage	340		850	mV_{pp}	Meets XFI host receiver differential input compliance mask.
t_r & t_f (20-80%)	Rise and Fall Times	24		35	ps	20-80%
R_{ODIFF}	Differential Output Impedance[a]	80	100	120	Ω	Over process, voltage and temperature range.

a. R_{ODIFF} is not measured, however will correlate to CML input resistor which is measured.

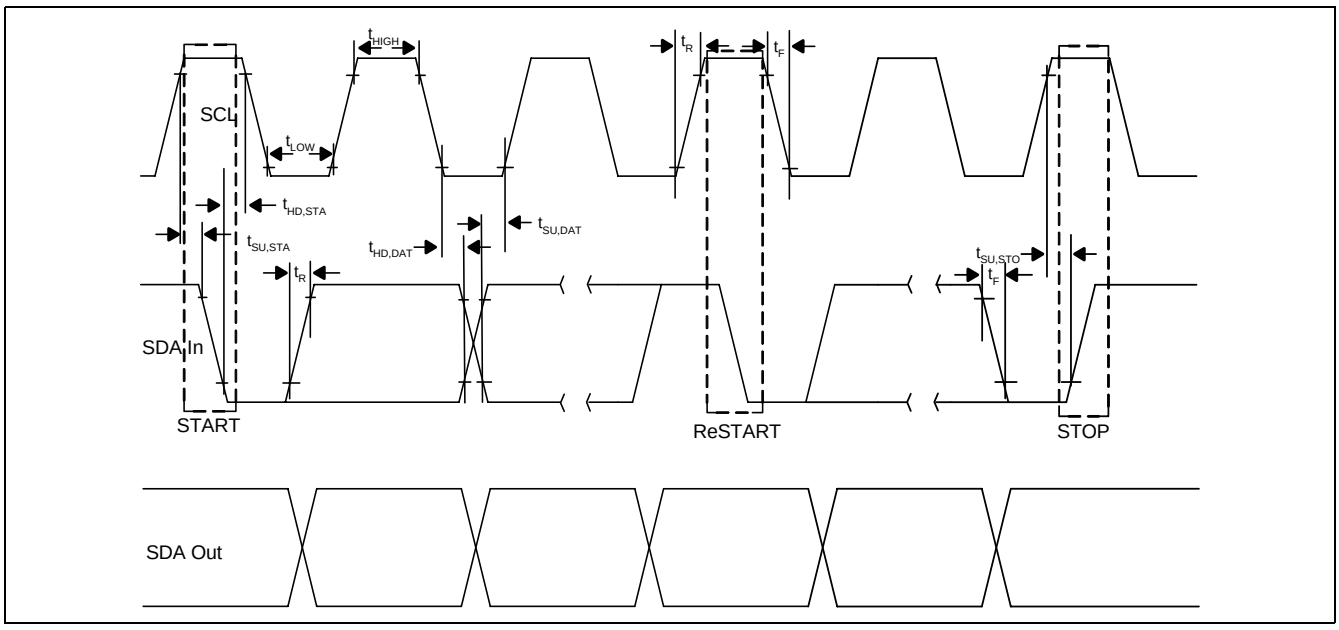
Table 17. LVTTL Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	2		$V_{DD\_3.3}$ + 0.3 V	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
I_{IN}	Input Leakage Current			200	µA	pins with pull up or pull down
V_{OH}	Output High Voltage	$V_{DD\_3.3}$ - 0.5 V		$V_{DD\_3.3}$ + 0.3 V	V	
V_{OL}	Output Low Voltage	0		0.4	V	I_{OL} = 3 mA
$LVTTL_{FREQ}$	Input/Output Operating Frequency			10	MHz	

Table 18. I²C Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	$V_{DD\_3.3}$ * 0.7		$V_{DD\_3.3}$ + 0.5	V	
V_{IL}	Input Low Voltage	-0.3		$V_{DD\_3.3}$ * 0.18	V	
I_{IN}	Input Leakage Current			20	µA	
V_{OH}	Output High Voltage	$V_{DD\_3.3}$ -0.5 V		$V_{DD\_3.3}$ + 0.3 V	V	
V_{OL}	Output Low Voltage	0		0.4	V	I_{OL} = 3 mA
$Clock_{FREQ}$	Serial Clock Operating Frequency			400	KHz	
t_{LOW}	Clock pulse width low	1.3			µs	
t_{HIGH}	Clock pulse width high	0.6			µs	
$t_{HD,STA}$	START Hold Time	0.6			µs	
$t_{SU,STA}$	START Set-up Time	0.6			µs	
$t_{HD,DAT}$	Data In Hold Time	0.1			µs	
$t_{SU,DAT}$	Data In Set-up TIme	0.1			µs	
$t_{SU,STO}$	STOP Set-up TIme	0.6			µs	
$t_{R,400}$	Input Rise Time (400 KHz)			300	ns	From ($V_{IL,MAX}$-0.15) to ($V_{IH,MIN}$+0.15)
$t_{F,400}$	Input Fall Time (400 KHz)			300	ns	From ($V_{IH,MIN}$+0.15) to ($V_{IL,MAX}$-0.15)

Figure 13. I2C BUS® Timing Diagram



EXTERNAL LOOP FILTER COMPONENTS

Table 19. Transmit and Receive External Loop Filter Components, See Figure 14

CSU_REFCLK	Reference Designator	Description	Value	Unit
155.52 MHz REFCLK 155.52 MHz REFCLK	R_1, $R_{2,}$	Resistor, Surface Mount, 0402	143	Ω
	C_1	Capacitor, Surface Mount	10	µF
	R_3, R_4	Resistor, Surface Mount, 0402	143	Ω
	C_2	Capacitor, Surface Mount	10	µF

Figure 14. External Loop Filter Components

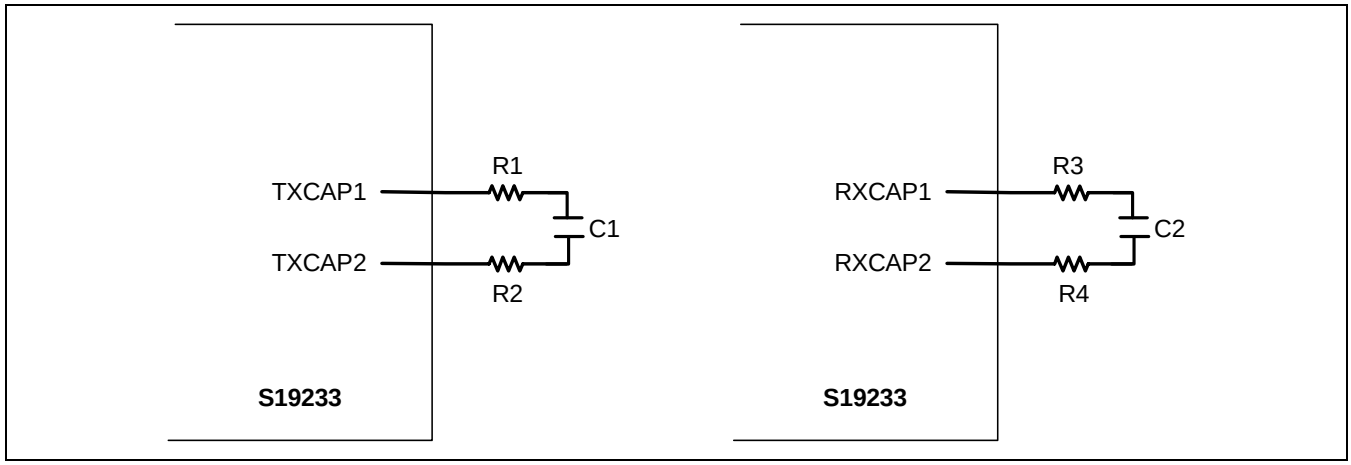
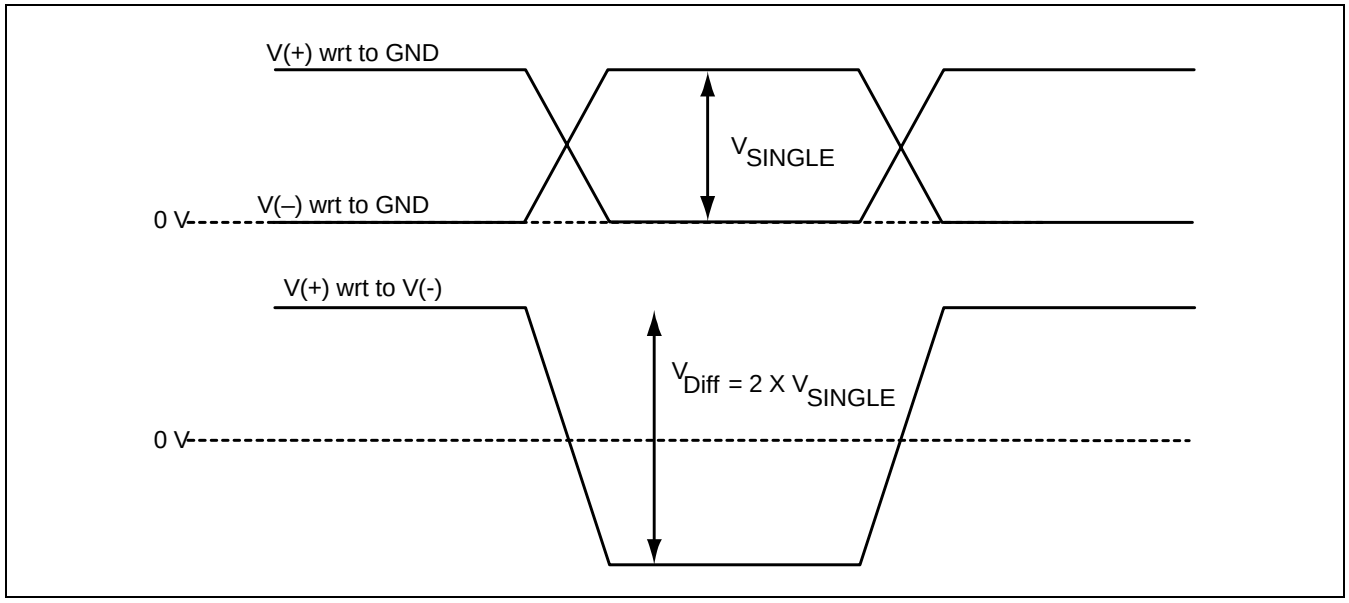


Figure 15. Differential Voltage Measurement



Note: WRT = With Respect To

RECOMMENDED TERMINATIONS

Figure 16. S19233 Differential CML Output to +5 V/+3.3 V LVPECL Input AC Coupled Termination

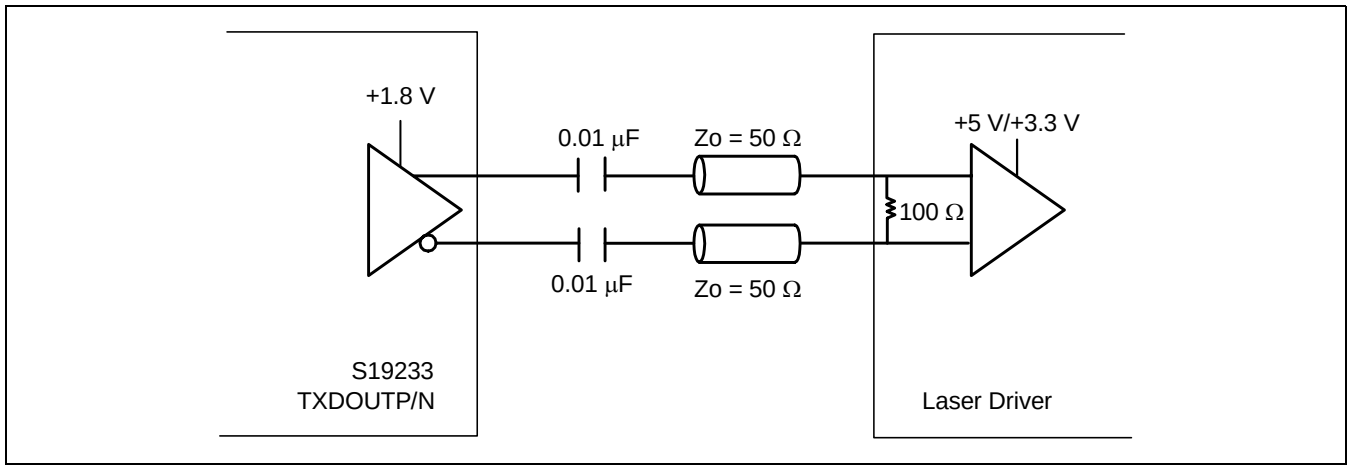


Figure 17. +5 V Differential PECL Driver to S19233 Differential CML Input AC Coupled Termination

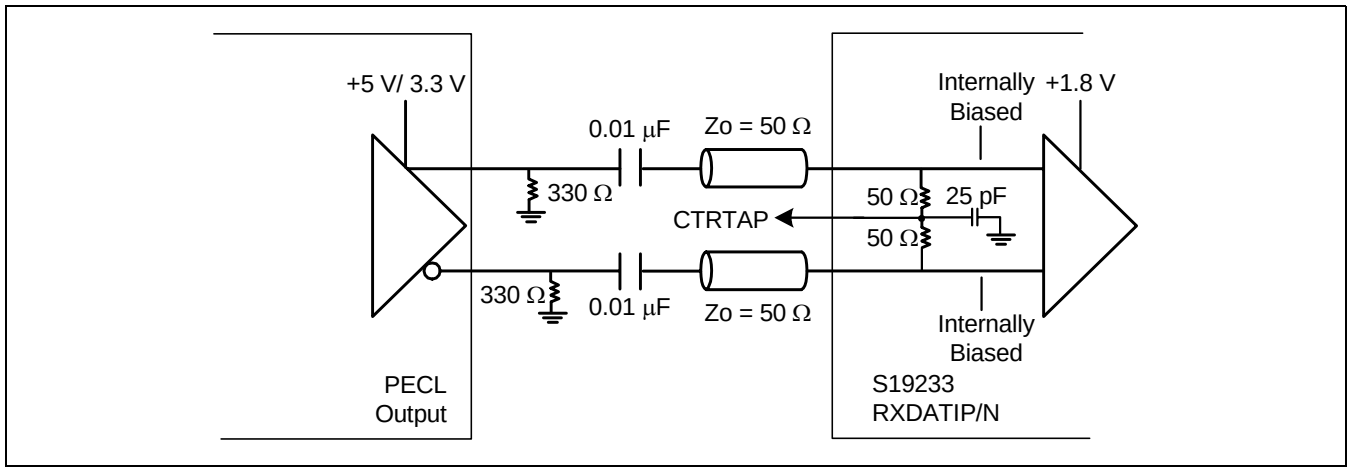


Figure 18. +5 V/+3.3 V Differential PECL Driver to S19233 CML Reference Clock Input AC Coupled Termination

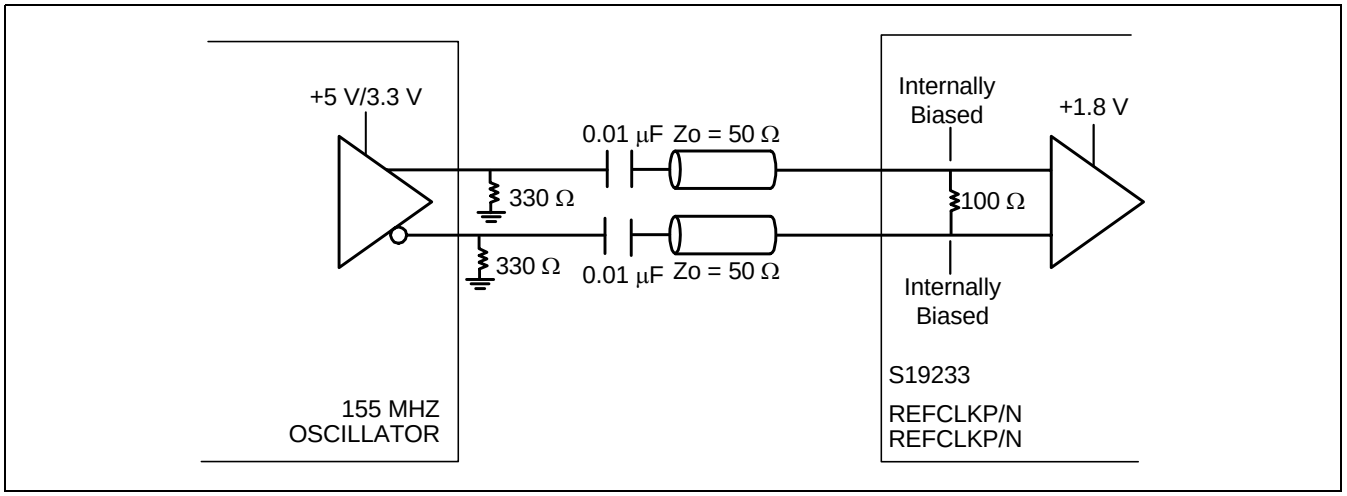
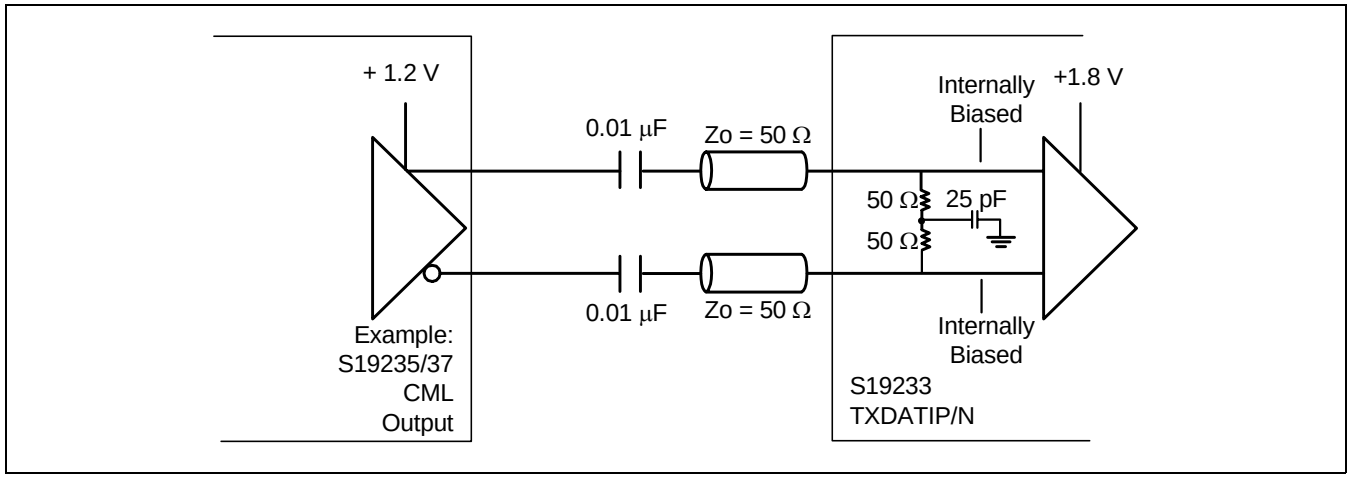


Figure 19. + 1.2 V Differential CML Driver to S19233 Differential CML Input AC Coupled Termination



DOCUMENT REVISION HISTORY

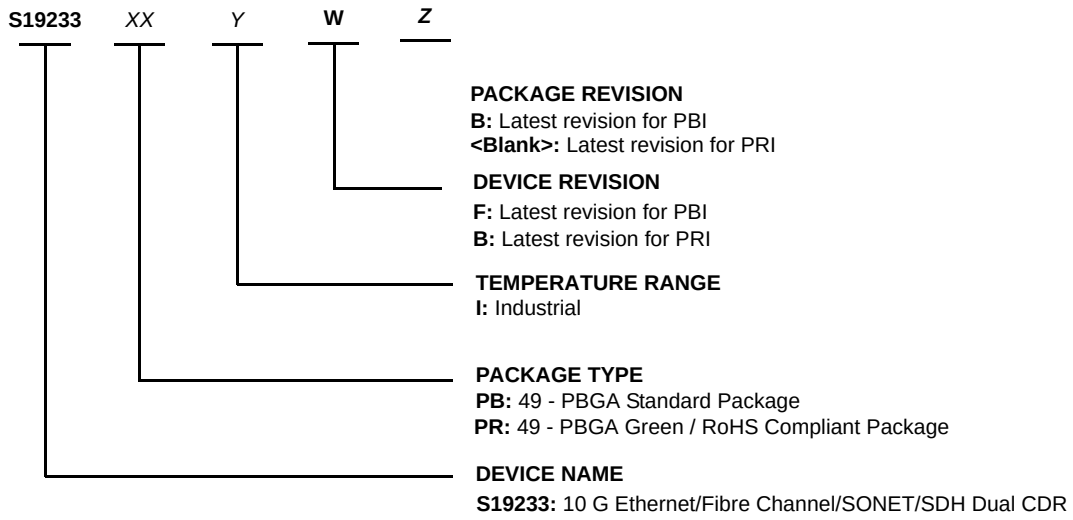
Revision	Date	Description
5.00	3/16/07	• Page 1, Changed 650 mW to 740 mW for Typical Power. • Page 6, Included Power Up Sequence paragraph. • Page 13, Updated default address statement for I^2C BUS and Address Register. • Page 19, Updated Table 9, I^2C BUS SCL I/O status changed to I. • Page 21, Updated Table 11, address 0x09 Mode from RW to RO. • Page 26, Design practice note added to Performance Specification, Table 13. • Page 26, Update Table 13, VCO condition note added for 11.32G. • Page 30, Update ESD Rating (1500V/1000V HS). • Page 31, Update Table 15, 1.8V Supply Current and Power. • Page 32, Table 16, Included note on R_{ODIFF}. • Page 32, Table 17, Removed 20uA Input Leakage Current line. • Page 33, Updated Table 18, I^2C BUS SDA to SCL hold time and V_{IL} Max value. • Page 39, Ordering Information, PRI/PBI line order adjust.
3.04	01/29/07	• Page 9, Added clarification to LOS condition. • Page 20,Updated Table 11, Register Map Summary. • Page 26, Removed condition in Table 13 for Nominal VCO Center Frequency line item. • Page 29, Updated Table 13, note a. • Page 30, Updated ESD Rating. • Page 33, Updated Loop Filter Values. • Page 38, Updated Ordering Information format to replace revision EB with FB and PRI with PRIB
3.03	09/18/06	• Cosmetic Changes Only
3.02	09/18/06	• Page 20, Updated Table 11, Register Map Summary • Page 24, Updated package drawing and added lead free symbol • Page 33, Updated loop filter resistor values • Page 37, Updated Ordering Information to replace revision CB with EB and add PRI
3.01	02/27/06	• Updated datasheet layout. Realigned sections to fit AMCC format. • Page 20, Update Table 11, Register Map Summary • Page 26, Update Table 13, Performance Summary • Page 32, Update Table 16 and 17 • Page 38, Updated Ordering Information to replace revision BB with CB
3.00	01/27/06	• Page 1, Updated feature list. • Page 7, Update Figure 2 to more accurately reflect chip operation and features. • Page 12, Include RX and TX VCO selections in Table 5. • Page 20, Update Table 10, Register Map Summary. • Page 25, Update Table 15 with RX VCO selection. • Page 29, Update Table 23 with TX VCO selection. • Page 26, Update Table 26 performance specifications. • Page 38, Added I^2C Timing Diagram. • Page 39, Update Table 27 Serial I/O Interface Specifications. • Page 41, Updated Table 29 I^2C Input/Output Characteristics. • Page 42, Updated Table 31 Recommended Operating Conditions with max current. • Page 43, Updated Table 32 with TX and RX external loop filter values. • Page 47, Updated Ordering Information to replace S19233PB with S19233PBIBB

DOCUMENT REVISION HISTORY (CONTINUED)

Revision	Date	Description
2.00	04/29/05	• Page 1, Updated feature list • Page 14-17, Updated SONET and Ethernet Jitter sections • Page 20, Update Table 11, Register Map Summary • Page 24, Updated Table 12, Thermal Management • Page 26, Updated Table 13, Performance Specifications • Page 32, Updated Table 16, Serial I/O Interface Specifications • Page 32, Updated Table 17, LVTTL Input/Output characteristics • Page 33, Updated Table 18, I^2C Input/Output Characteristics • Page 31, Updated Table 15, Recommended Operating Conditions • Page 34, Updated Table 19, Resistor value changes
1.00	02/11/05	• Initial release

ORDERING INFORMATION

Device Code	Product
S19233PBIFB **S19233PRIB**	**S19233 - 10 G Ethernet/Fibre Channel/SONET/SDH Dual CDR** Industrial Temp, Standard Package **S19233 - 10 G Ethernet/Fibre Channel/SONET/SDH Dual CDR** Industrial Temp, RoHS Compliant Package



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