

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

MITSUBISHI MICROCOMPUTERS

M35040-XXXFP, M35041-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35040-XXXFP and M35041-XXXFP are character pattern display controllers designed to display title, time and date, and operation messages inside the viewfinder. It uses a silicon gate CMOS process and is housed in a 20-pin shrink SOP package.

The differences among M35040-XXXFP and M35041-XXXFP are noted below.

The descriptions that follow describe the M35040-XXXFP unless otherwise noted.

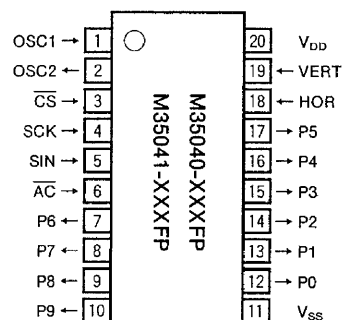
Type name	Characters available	DA7 of display RAM (bit 7 of addresses 00 ₁₆ to EF ₁₆)
M35040-XXXFP	128	Set to "0"
M35041-XXXFP	256	Set the MSB of character code

The character patterns for the M35040-001FP and M35041-001FP which are standard ROM type of the M35040-XXXFP and M35041-XXXFP are also included.

FEATURES

- Screen composition 24 columns × 10 lines
- Number of characters displayed 240 (Max.)
- Character composition 12 × 18 dot matrix
- Characters available
 - M35040-XXXFP 128 characters
 - M35041-XXXFP 256 characters
- Character sizes available 4 (horizontal) × 4 (vertical)
- Display locations available
 - Horizontal direction 62 locations
 - Vertical direction 64 locations
- Blanking Character, units
 - Cycle : approximately 1 second, or approximately 0.5 seconds
 - Duty : 25%, 50%, or 75%
- Data input By the 16-bit serial input function
- Coloring
 - Character unit 8 colors (RGB output)
 - Raster coloring 8 colors (RGB output)
 - Specified by register
 - Matrix-outline coloring 8 colors (RGB output)
 - Specified by register
 - Border coloring 8 colors (RGB output)
 - Specified by register

PIN CONFIGURATION (TOP VIEW)



Outline 20P2Q-A

- Blanking
 - Blanking0 Blanking off
 - Character size blanking
 - Border size blanking
 - Matrix-outline blanking
 - Blanking1 Blanking of the border size for the G component of RGB output.
 - Blanking2 Blanking of the border size for the B component of RGB output.
- Synchronized separation circuit Built-in
- Output ports
 - 6 shared output ports (toggled between RGB output)
 - 4 dedicated output ports
- Oscillation stop function
 - Be possible to stop the oscillation for display
- Display RAM erase function
- Reversed character display function (character unit)

APPLICATION

Cam corder

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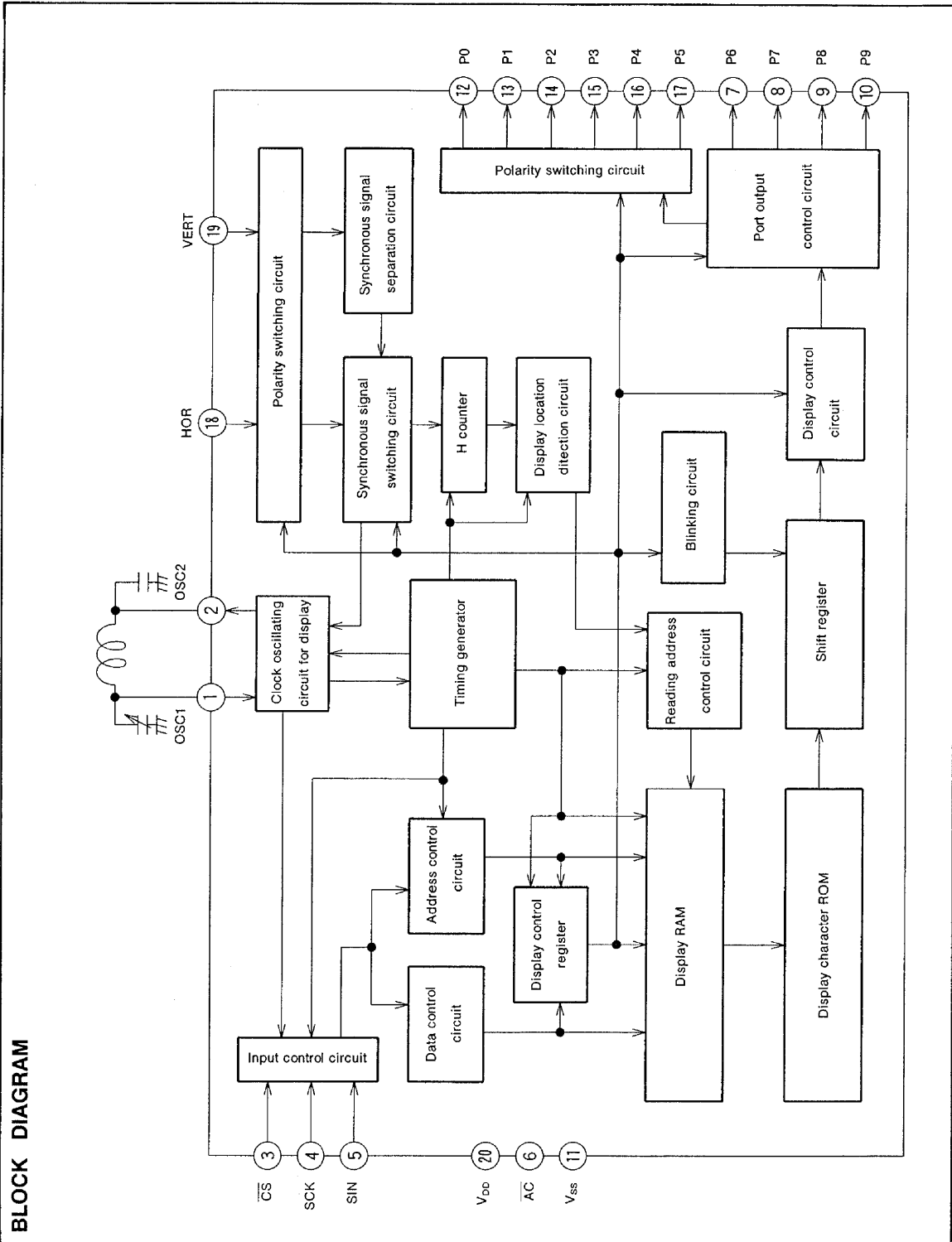
SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input /Output	Function
1	OSC1	Pins for attachment of external oscillator circuit	Input	There are the pins for attaching an external display oscillator circuit. The standard oscillation frequency is approximately 7MHz. This oscillation frequency determines the horizontal position of the display on the viewfinder and the width of the characters. LC oscillation and RC oscillation are possible.
2	OSC2		Output	
3	CS	Chip select input	Input	This is the chip select pin, and when serial data transmission is being carried out, it goes to "L". Hysteresis input. Includes built-in pull-up resistor.
4	SCK	Serial clock input	Input	When CS pin is "L", SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included.
5	SIN	Serial data input	Input	This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Includes built-in pull-up resistor.
6	AC	Auto-clear input	Input	When "L", this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor.
7	P6	Port P6 output	Output	This is the output port. Port data is set by PTD6.
8	P7	Port P7 output	Output	This is the output port. Port data is set by PTD7.
9	P8	Port P8 output	Output	This is the output port. Port data is set by PTD8.
10	P9	Port P9 output	Output	This is the output port. Port data is set by PTD9.
11	V _{SS}	Earthing pin	—	Please connect to GND using circuit earthing pin.
12	P0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK0 signal output.
13	P1	Port P1 output	Output	This pin can be toggled between port pin output and R signal output.
14	P2	Port P2 output	Output	This pin can be toggled between port pin output, BLNK1 signal output, and CO signal output.
15	P3	Port P3 output	Output	This pin can be toggled between port pin output and G signal output.
16	P4	Port P4 output	Output	This pin can be toggled between port pin output, BLNK2 signal output, and BLNK signal output.
17	P5	Port P5 output	Output	This pin can be toggled between port pin output and B signal output.
18	HOR	Horizontal synchronization signal input	Input	This pin inputs the horizontal synchronization signal. Hysteresis input.
19	VERT	Vertical synchronization signal input	Input	This pin inputs the vertical synchronization signal. Hysteresis input.
20	V _{DD}	Power pin	—	Please connection to +5V or +3V with the power pin.

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

MEMORY CONSTITUTION

Address 00₁₆ to EF₁₆ are assigned to the display RAM, address F0₁₆ to F5₁₆ are assigned to the display control registers. The internal circuit is reset and all display control registers (address F0₁₆ to F5₁₆) are set to "0" and display

RAM (address 00₁₆ to EF₁₆) are set to "FF₁₆" when the $\overline{AC}$ pin level is "L".

The memory constitution of the M35040-XXXXP is different from the M35041-XXXXP.

Each of them are shown in Figure 1 and Figure 2.

Bit Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
00 ₁₆	0	0	CF	REV	BLINK	B	G	R	0	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀
	⋮	⋮	CF	Reverse	Blinking	Character color				⋮	Character code					
EF ₁₆	0	0	CF	REV	BLINK	B	G	R	0	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀
F0 ₁₆	0	0	0	SEPV	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0
F1 ₁₆	0	0	0	TEST 2	TEST 1	TEST 0	PLTV	PLTH	SYNCRV	SPACE 2	SPACE 1	SPACE 0	PTD 9	PTD 8	PTD 7	PTD 6
F2 ₁₆	0	0	0	BLINK 2	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
F3 ₁₆	0	0	0	RB	RG	RR	—	B/F	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
F4 ₁₆	0	0	0	FB	FG	FR	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
F5 ₁₆	0	0	0	BB	BG	BR	EXP	CVF	BCOL	STOP 1	DSPON	RAMERS	BLK 1	BLK 0	BLINK 1	BLINK 0

Fig. 1 Memory constitution (M35040-XXXXP)

Bit Address	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
00 ₁₆	0	0	CF	REV	BLINK	B	G	R	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀
	⋮	⋮	CF	Reverse	Blinking	Character color				Character code						
EF ₁₆	0	0	CF	REV	BLINK	B	G	R	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀
F0 ₁₆	0	0	0	SEPV	PTD 5	PTD 4	PTD 3	PTD 2	PTD 1	PTD 0	PTC 5	PTC 4	PTC 3	PTC 2	PTC 1	PTC 0
F1 ₁₆	0	0	0	TEST 2	TEST 1	TEST 0	PLTV	PLTH	SYNCRV	SPACE 2	SPACE 1	SPACE 0	PTD 9	PTD 8	PTD 7	PTD 6
F2 ₁₆	0	0	0	BLINK 2	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
F3 ₁₆	0	0	0	RB	RG	RR	—	B/F	VSZ 21	VSZ 20	VSZ 11	VSZ 10	HSZ 21	HSZ 20	HSZ 11	HSZ 10
F4 ₁₆	0	0	0	FB	FG	FR	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
F5 ₁₆	0	0	0	BB	BG	BR	EXP	CVF	BCOL	STOP 1	DSPON	RAMERS	BLK 1	BLK 0	BLINK 1	BLINK 0

Fig. 2 Memory constitution (M35041-XXXXP)

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SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen constitution is shown in Figure 3.

Row Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	00 ₁₆	01 ₁₆	02 ₁₆	03 ₁₆	04 ₁₆	05 ₁₆	06 ₁₆	07 ₁₆	08 ₁₆	09 ₁₆	0A ₁₆	0B ₁₆	0C ₁₆	0D ₁₆	0E ₁₆	0F ₁₆	10 ₁₆	11 ₁₆	12 ₁₆	13 ₁₆	14 ₁₆	15 ₁₆	16 ₁₆	17 ₁₆
2	18 ₁₆	19 ₁₆	1A ₁₆	1B ₁₆	1C ₁₆	1D ₁₆	1E ₁₆	1F ₁₆	20 ₁₆	21 ₁₆	22 ₁₆	23 ₁₆	24 ₁₆	25 ₁₆	26 ₁₆	27 ₁₆	28 ₁₆	29 ₁₆	2A ₁₆	2B ₁₆	2C ₁₆	2D ₁₆	2E ₁₆	2F ₁₆
3	30 ₁₆	31 ₁₆	32 ₁₆	33 ₁₆	34 ₁₆	35 ₁₆	36 ₁₆	37 ₁₆	38 ₁₆	39 ₁₆	3A ₁₆	3B ₁₆	3C ₁₆	3D ₁₆	3E ₁₆	3F ₁₆	40 ₁₆	41 ₁₆	42 ₁₆	43 ₁₆	44 ₁₆	45 ₁₆	46 ₁₆	47 ₁₆
4	48 ₁₆	49 ₁₆	4A ₁₆	4B ₁₆	4C ₁₆	4D ₁₆	4E ₁₆	4F ₁₆	50 ₁₆	51 ₁₆	52 ₁₆	53 ₁₆	54 ₁₆	55 ₁₆	56 ₁₆	57 ₁₆	58 ₁₆	59 ₁₆	5A ₁₆	5B ₁₆	5C ₁₆	5D ₁₆	5E ₁₆	5F ₁₆
5	60 ₁₆	61 ₁₆	62 ₁₆	63 ₁₆	64 ₁₆	65 ₁₆	66 ₁₆	67 ₁₆	68 ₁₆	69 ₁₆	6A ₁₆	6B ₁₆	6C ₁₆	6D ₁₆	6E ₁₆	6F ₁₆	70 ₁₆	71 ₁₆	72 ₁₆	73 ₁₆	74 ₁₆	75 ₁₆	76 ₁₆	77 ₁₆
6	78 ₁₆	79 ₁₆	7A ₁₆	7B ₁₆	7C ₁₆	7D ₁₆	7E ₁₆	7F ₁₆	80 ₁₆	81 ₁₆	82 ₁₆	83 ₁₆	84 ₁₆	85 ₁₆	86 ₁₆	87 ₁₆	88 ₁₆	89 ₁₆	8A ₁₆	8B ₁₆	8C ₁₆	8D ₁₆	8E ₁₆	8F ₁₆
7	90 ₁₆	91 ₁₆	92 ₁₆	93 ₁₆	94 ₁₆	95 ₁₆	96 ₁₆	97 ₁₆	98 ₁₆	99 ₁₆	9A ₁₆	9B ₁₆	9C ₁₆	9D ₁₆	9E ₁₆	9F ₁₆	AO ₁₆	A1 ₁₆	A2 ₁₆	A3 ₁₆	A4 ₁₆	A5 ₁₆	A6 ₁₆	A7 ₁₆
8	A8 ₁₆	A9 ₁₆	AA ₁₆	AB ₁₆	AC ₁₆	AD ₁₆	AE ₁₆	AF ₁₆	B0 ₁₆	B1 ₁₆	B2 ₁₆	B3 ₁₆	B4 ₁₆	B5 ₁₆	B6 ₁₆	B7 ₁₆	B8 ₁₆	B9 ₁₆	BA ₁₆	BB ₁₆	BC ₁₆	BD ₁₆	BE ₁₆	BF ₁₆
9	C0 ₁₆	C1 ₁₆	C2 ₁₆	C3 ₁₆	C4 ₁₆	C5 ₁₆	C6 ₁₆	C7 ₁₆	C8 ₁₆	C9 ₁₆	CA ₁₆	CB ₁₆	CC ₁₆	CD ₁₆	CE ₁₆	CF ₁₆	D0 ₁₆	D1 ₁₆	D2 ₁₆	D3 ₁₆	D4 ₁₆	D5 ₁₆	D6 ₁₆	D7 ₁₆
10	D8 ₁₆	D9 ₁₆	DA ₁₆	DB ₁₆	DC ₁₆	DD ₁₆	DE ₁₆	DF ₁₆	E0 ₁₆	E1 ₁₆	E2 ₁₆	E3 ₁₆	E4 ₁₆	E5 ₁₆	E6 ₁₆	E7 ₁₆	E8 ₁₆	E9 ₁₆	EA ₁₆	EB ₁₆	EC ₁₆	ED ₁₆	EE ₁₆	EF ₁₆

The hexadecimal numbers in the boxes show the display RAM address.

Fig. 3 Screen constitution

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REGISTERS DESCRIPTION

(1) Address F0₁₆

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	①	P0 output (port P0). Port data is set by PTD0.	BLNK0 outputs RGB output blanking. Blanking status is determined by BLK0, BLK1, and DSP0 to DSP9 settings.
		1	BLNK0 output. Polarity is set by PTD0.	
1	PTC1	①	P1 output (port P1). Port data is set by PTD1.	
		1	R signal output. Polarity is set by PTD1.	
2	PTC2	①	P2 output (port P2). Port data is set by PTD2.	BLNK1 outputs the blanking of the border size for the G component of RGB output. BLNK1 outputs the blanking of the border size regardless of BLK0 or BLK1.
		1	BLNK1 output. Polarity is set by PTD2.	
3	PTC3	①	P3 output (port P3). Port data is set by PTD3.	
		1	G signal output. Polarity is set by PTD3.	
4	PTC4	①	P4 output (port P4). Port data is set by PTD4.	BLNK2 outputs the blanking of the border size for the B component of RGB output. BLNK2 outputs the blanking of the border size regardless of BLK0 or BLK1.
		1	BLNK2 output. Polarity is set by PTD4.	
5	PTC5	①	P5 output (port P5). Port data is set by PTD5.	
		1	B signal output. Polarity is set by PTD5.	
6	PTD0	①	"L" output (P0 output) or negative polarity output (BLNK0 output).	Port data control
		1	"H" output (P0 output) or positive polarity output (BLNK0 output).	
7	PTD1	①	"L" output (P1 output) or negative polarity output (R signal output).	
		1	"H" output (P1 output) or positive polarity output (R signal output).	
8	PTD2	①	"L" output (P2 output) or negative polarity output (BLNK1 output).	
		1	"H" output (P2 output) or positive polarity output (BLNK1 output).	
9	PTD3	①	"L" output (P3 output) or negative polarity output (G signal output).	
		1	"H" output (P3 output) or positive polarity output (G signal output).	
A	PTD4	①	"L" output (P4 output) or negative polarity output (BLNK2 output).	
		1	"H" output (P4 output) or positive polarity output (BLNK2 output).	
B	PTD5	①	"L" output (P5 output) or negative polarity output (B signal output).	
		1	"H" output (P5 output) or positive polarity output (B signal output).	
C	SEPV	①	Synchronization separated circuit OFF.	Vertical synchronization signal is separated from composite synchronization signal.
		1	Synchronization separated circuit ON.	

Note : The mark ① around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

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(2) Address F1₁₆

DA	Register	Contents		Remarks															
		Status	Function																
0	PTD6	①	"L" output (port P6)	Port data control (port P6 to P9)															
		1	"H" output (port P6)																
1	PTD7	①	"L" output (port P7)																
		1	"H" output (port P7)																
2	PTD8	①	"L" output (port P8)																
		1	"H" output (port P8)																
3	PTD9	①	"L" output (port P9)																
		1	"H" output (port P9)																
4	SPACE0	①	<table><tr><th colspan="3">SPACE</th><th rowspan="2">Number of Lines and Space (□ represents space)</th></tr><tr><th>2</th><th>1</th><th>0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>10</td></tr><tr><td>0</td><td>0</td><td>1</td><td>5 □ 5</td></tr></table>	SPACE			Number of Lines and Space (□ represents space)	2	1	0	0	0	0	10	0	0	1	5 □ 5	Leave one line worth of space in the vertical direction. For example, 5 □ 5 indicates two sets of 5 lines with a line of spaces between lines 5 and 6. A line is 18 ×N horizontal scan lines. N is determined by the character size in the vertical direction as follows: ×1 N=1 ×2 N=2 ×3 N=3 ×4 N=4
		SPACE			Number of Lines and Space (□ represents space)														
2	1	0																	
0	0	0	10																
0	0	1	5 □ 5																
1	<table><tr><td>0</td><td>0</td><td>0</td><td>10</td></tr><tr><td>0</td><td>1</td><td>0</td><td>5 □ □ 5</td></tr></table>	0	0	0	10	0	1	0	5 □ □ 5										
0	0	0	10																
0	1	0	5 □ □ 5																
5	SPACE1	①	<table><tr><td>0</td><td>1</td><td>0</td><td>5 □ □ 5</td></tr><tr><td>0</td><td>1</td><td>1</td><td>5 □ □ □ 5</td></tr></table>	0	1	0	5 □ □ 5	0	1	1	5 □ □ □ 5								
		0	1	0	5 □ □ 5														
0	1	1	5 □ □ □ 5																
1	<table><tr><td>1</td><td>0</td><td>0</td><td>1 □ 8 □ 1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>2 □ 6 □ 2</td></tr></table>	1	0	0	1 □ 8 □ 1	1	0	1	2 □ 6 □ 2										
1	0	0	1 □ 8 □ 1																
1	0	1	2 □ 6 □ 2																
6	SPACE2	①	<table><tr><td>1</td><td>1</td><td>0</td><td>3 □ 4 □ 3</td></tr><tr><td>1</td><td>1</td><td>1</td><td>4 □ 2 □ 4</td></tr></table>	1	1	0	3 □ 4 □ 3	1	1	1	4 □ 2 □ 4								
		1	1	0	3 □ 4 □ 3														
1	1	1	4 □ 2 □ 4																
1	□ represents one line worth of spaces.																		
7	SYNCV	①	Output after port output is set to PTD9.	Selects whether port P9 output is synchronized with vertical synchronization.															
		1	Output after synchronizing port output to V.																
8	PLTH	①	Negative polarity input (HOR pin).	Sets the polarity of HOR pin.															
		1	Positive polarity input (HOR pin).																
9	PLTV	①	Negative polarity input (VERT pin).	Sets the polarity of VERT pin.															
		1	Positive polarity input (VERT pin).																
A	TEST0	①	It should be fixed to "0".																
		1	Can not be used.																
B	TEST1	①	It should be fixed to "0".																
		1	Can not be used.																
C	TEST2	①	It should be fixed to "0".																
		1	Can not be used.																

Note : The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

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(3) Address F2₁₆

DA	Register	Contents		Remarks																	
		Status	Function																		
0	HP0 (LSB)	⓪	If HS is the horizontal display start location, $HS = T \times (4 \sum_{n=0}^5 2^n HP_n + N).$ T : The oscillation cycle of oscillator OSC1, 2 <table><tr><td>HSZ11</td><td>HSZ10</td><td rowspan="2">N</td></tr><tr><td>HSZ21</td><td>HSZ20</td></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table>	HSZ11	HSZ10	N	HSZ21	HSZ20	0	0	9	0	1	10	1	0	11	1	1	12	Horizontal display start location is specified using the 6 bits from HP5 to HP0. Note : HP5 to 0 = (000000₂) and (000001₂) setting is forbidden.
		HSZ11		HSZ10	N																
HSZ21	HSZ20																				
0	0	9																			
0	1	10																			
1	0	11																			
1	1	12																			
1																					
1	HP1	⓪																			
		1																			
2	HP2	⓪																			
		1																			
3	HP3	⓪																			
		1																			
4	HP4	⓪																			
		1																			
5	HP5 (MSB)	⓪																			
		1																			
6	VP0 (LSB)	⓪	If VS is the vertical display start location, $VS = H \times (4 \sum_{n=0}^5 2^n VP_n + 3).$ H : Cycle with the horizontal synchronizing pulse	The vertical start location is specified using the 6 bits from VP5 to VP0. Note1. In case of B/F register is "0".																	
		1																			
7	VP1	⓪																			
		1																			
8	VP2	⓪																			
		1																			
9	VP3	⓪																			
		1																			
A	VP4	⓪																			
		1																			
B	VP5 (MSB)	⓪																			
		1																			
C	BLINK2	⓪	Division of vertical synchronization signal into 1/64. Cycle approximately 1 second	Blinking cycle can be altered																	
		1	Division of vertical synchronization signal into 1/32. Cycle approximately 0.5 second																		

Note : The mark ⓪ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address F3₁₆

DA	Register	Contents		Remarks																																				
		Status	Function																																					
0	HSZ10	⓪	<table><tr><td>HSZ10 \ HSZ11</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1T/1dot</td><td>2T/1dot</td></tr><tr><td>1</td><td>3T/1dot</td><td>4T/1dot</td></tr></table>	HSZ10 \ HSZ11	0	1	0	1T/1dot	2T/1dot	1	3T/1dot	4T/1dot	Character size setting in the horizontal direction for the first line.																											
		HSZ10 \ HSZ11		0	1																																			
0	1T/1dot	2T/1dot																																						
1	3T/1dot	4T/1dot																																						
1																																								
1	HSZ11	⓪																																						
		1																																						
2	HSZ20	⓪		<table><tr><td>HSZ20 \ HSZ21</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1T/1dot</td><td>2T/1dot</td></tr><tr><td>1</td><td>3T/1dot</td><td>4T/1dot</td></tr></table>	HSZ20 \ HSZ21	0	1	0	1T/1dot	2T/1dot	1	3T/1dot		4T/1dot	Character size setting in the horizontal direction for the 2nd line to 10th line.																									
		HSZ20 \ HSZ21			0	1																																		
0	1T/1dot	2T/1dot																																						
1	3T/1dot	4T/1dot																																						
1																																								
3	HSZ21	⓪																																						
		1																																						
4	VSZ10	⓪	<table><tr><td>VSZ10 \ VSZ11</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H/1dot</td><td>2H/1dot</td></tr><tr><td>1</td><td>3H/1dot</td><td>4H/1dot</td></tr></table>		VSZ10 \ VSZ11	0	1	0	1H/1dot	2H/1dot	1	3H/1dot	4H/1dot	Character size setting in the vertical direction for the first line.																										
		VSZ10 \ VSZ11			0	1																																		
0	1H/1dot	2H/1dot																																						
1	3H/1dot	4H/1dot																																						
1																																								
5	VSZ11	⓪																																						
		1																																						
6	VSZ20	⓪		<table><tr><td>VSZ20 \ VSZ21</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H/1dot</td><td>2H/1dot</td></tr><tr><td>1</td><td>3H/1dot</td><td>4H/1dot</td></tr></table>	VSZ20 \ VSZ21	0	1	0	1H/1dot	2H/1dot	1	3H/1dot	4H/1dot		Character size setting in the vertical direction for the 2nd line to 10th line.																									
		VSZ20 \ VSZ21			0	1																																		
0	1H/1dot	2H/1dot																																						
1	3H/1dot	4H/1dot																																						
1																																								
7	VSZ21	⓪																																						
		1																																						
8	B/F	⓪	Synchronize with the leading edge of horizontal synchronization.		Synchronize with the front porch or back porch of the horizontal synchronization signal.																																			
		1	Synchronize with the trailing edge of horizontal synchronization.																																					
9	—	⓪	It should be fixed to "0".																																					
		1	Can not be used.																																					
A	RR	⓪	<table><tr><td>RB</td><td>RG</td><td>RR</td><td>Color</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table>	RB	RG	RR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the color of all blankings.
RB	RG	RR		Color																																				
0	0	0		Black																																				
0	0	1		Red																																				
0	1	0		Green																																				
0	1	1		Yellow																																				
1	0	0		Blue																																				
1	0	1		Magenta																																				
1	1	0		Cyan																																				
1	1	1		White																																				
B	RG	⓪																																						
		1																																						
C	RB	⓪																																						
		1																																						

Note : The mark ⓪ around the status value means the reset status by the "L" level is input to AC pin.

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(5) Address F4₁₆

DA	Register	Contents		Remarks																																				
		Status	Function																																					
0	DSP0	⓪	Line 1 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 1.																																				
		1	Line 1 is in a different display mode (Note 2).																																					
1	DSP1	⓪	Line 2 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 2.																																				
		1	Line 2 is in a different display mode (Note 2).																																					
2	DSP2	⓪	Line 3 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 3.																																				
		1	Line 3 is in a different display mode (Note 2).																																					
3	DSP3	⓪	Line 4 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 4.																																				
		1	Line 4 is in a different display mode (Note 2).																																					
4	DSP4	⓪	Line 5 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 5.																																				
		1	Line 5 is in a different display mode (Note 2).																																					
5	DSP5	⓪	Line 6 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 6.																																				
		1	Line 6 is in a different display mode (Note 2).																																					
6	DSP6	⓪	Line 7 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 7.																																				
		1	Line 7 is in a different display mode (Note 2).																																					
7	DSP7	⓪	Line 8 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 8.																																				
		1	Line 8 is in a different display mode (Note 2).																																					
8	DSP8	⓪	Line 9 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 9.																																				
		1	Line 9 is in a different display mode (Note 2).																																					
9	DSP9	⓪	Line 10 is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 10.																																				
		1	Line 10 is in a different display mode (Note 2).																																					
A	FR	⓪	<table><tr><th>FB</th><th>FG</th><th>FR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table>	FB	FG	FR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the blanking color of the border size.
FB	FG	FR		Color																																				
0	0	0		Black																																				
0	0	1		Red																																				
0	1	0		Green																																				
0	1	1		Yellow																																				
1	0	0	Blue																																					
1	0	1	Magenta																																					
1	1	0	Cyan																																					
1	1	1	White																																					
B	FG	1																																						
		⓪																																						
C	FB	⓪																																						
		1																																						

Note1 : The mark ⓪ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.

Note2 : See the display form.

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(6) Address F5₁₆

DA	Register	Contents		Remarks																																				
		Status	Function																																					
0	BLINK0	①	<table><tr><td>BLINK0 \ BLINK1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Blinking OFF</td><td>Duty 25%</td></tr><tr><td>1</td><td>Duty 50%</td><td>Duty 75%</td></tr></table>	BLINK0 \ BLINK1	0	1	0	Blinking OFF	Duty 25%	1	Duty 50%	Duty 75%	Blinking duty ratio can be altered																											
		BLINK0 \ BLINK1		0	1																																			
0	Blinking OFF	Duty 25%																																						
1	Duty 50%	Duty 75%																																						
1																																								
1	BLINK1	①																																						
		1																																						
2	BLK0	①		<table><tr><td>BLK0 \ BLK1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Blanking OFF</td><td>Character size</td></tr><tr><td>1</td><td>Border size</td><td>Matrix-outline size</td></tr></table>	BLK0 \ BLK1	0	1	0	Blanking OFF	Character size	1	Border size	Matrix-outline size	Display mode variable																										
		BLK0 \ BLK1			0	1																																		
0	Blanking OFF	Character size																																						
1	Border size	Matrix-outline size																																						
1																																								
3	BLK1	①																																						
		1																																						
4	RAMERS	①	RAM not erased		There is no need to reset because there is no register for this bit.																																			
		1	RAM erased																																					
5	DSPON	①	Display OFF		Display can be altered.																																			
		1	Display ON																																					
6	STOP1	①	Oscillation of OSC1, OSC2 for display	OSC1 and OSC2 oscillation switching. To stop the oscillation, set CS pin to "H" level and DSPON (address F5 ₁₆) to "0".																																				
		1	Stop the oscillation of OSC1, OSC2 for display																																					
7	BCOL	①	Blanking of BLK0, BLK1	Sets all raster blanking																																				
		1	All raster blanking																																					
8	CVF	①	R, G, B, BLNK0, BLNK1, and BLNK2 signal output	CO and BLNK are output in association with CF bits in the addresses 00 ₁₆ to EF ₁₆ of the display RAM (DAD).																																				
		1	R, G, B, BLNK0, CO, and BLNK signal output																																					
9	EXP	①	BLNK0 signal outputs blanking regardless of the character color	Select whether to output BLNK0 signal or cut in case of black character.																																				
		1	Cuts BLNK0 signal for black character.																																					
A	BR	①	<table><tr><td>BB</td><td>BG</td><td>BR</td><td>Color</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table>	BB	BG	BR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the blanking color of the Matrix-outline size.
		BB		BG	BR	Color																																		
0	0	0		Black																																				
0	0	1		Red																																				
0	1	0		Green																																				
0	1	1		Yellow																																				
1	0	0		Blue																																				
1	0	1		Magenta																																				
1	1	0		Cyan																																				
1	1	1		White																																				
1																																								
B	BG	①																																						
		1																																						
C	BB	①																																						
		1																																						

MITSUBISHI MICROCOMPUTERS
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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DISPLAY FORM 1

The M35040-XXXFP has blanking 0 to blanking 2 function.

Table 1 shows display form of blanking 0.

Table 2 shows display form of blanking 1 and blanking 2.

Table 1. Display form of blanking 0

BCOL	Standard blanking		When the all of registers DSPI are set to "0".	When some of registers DSPI are set to "1".		BLNK0 output
	BLK1	BLK0		DSPI=0	DSPI=1	
0	0	0	OFF	Border F (RGB)	Character	When the blanking status is blanking off, the BLNK0 output is outline output. B (RGB)
0	0	1	Character	Character	Border F (RGB)	
0	1	0	Border F (RGB)	Border F (RGB)	Matrix-outline B (RGB)	
0	1	1	Matrix-outline B (RGB)	Matrix-outline B (RGB)	Character	
1	0	0	Character	Border F (RGB)	Character	All raster blanking
1	0	1	Character	Character	Border F (RGB)	All raster blanking
1	1	0	Border F (RGB)	Border F (RGB)	Matrix-outline B (RGB)	All raster blanking
1	1	1	Matrix-outline B (RGB)	Matrix-outline B (RGB)	Character	All raster blanking

Note : i = 0 to 9

Table 2. Display form of blanking 1 and blanking 2

BLNK1 output	Blanking for G bit (display RAM)	Border
BLNK2 output	Blanking for B bit (display RAM)	Border

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

Display form 2

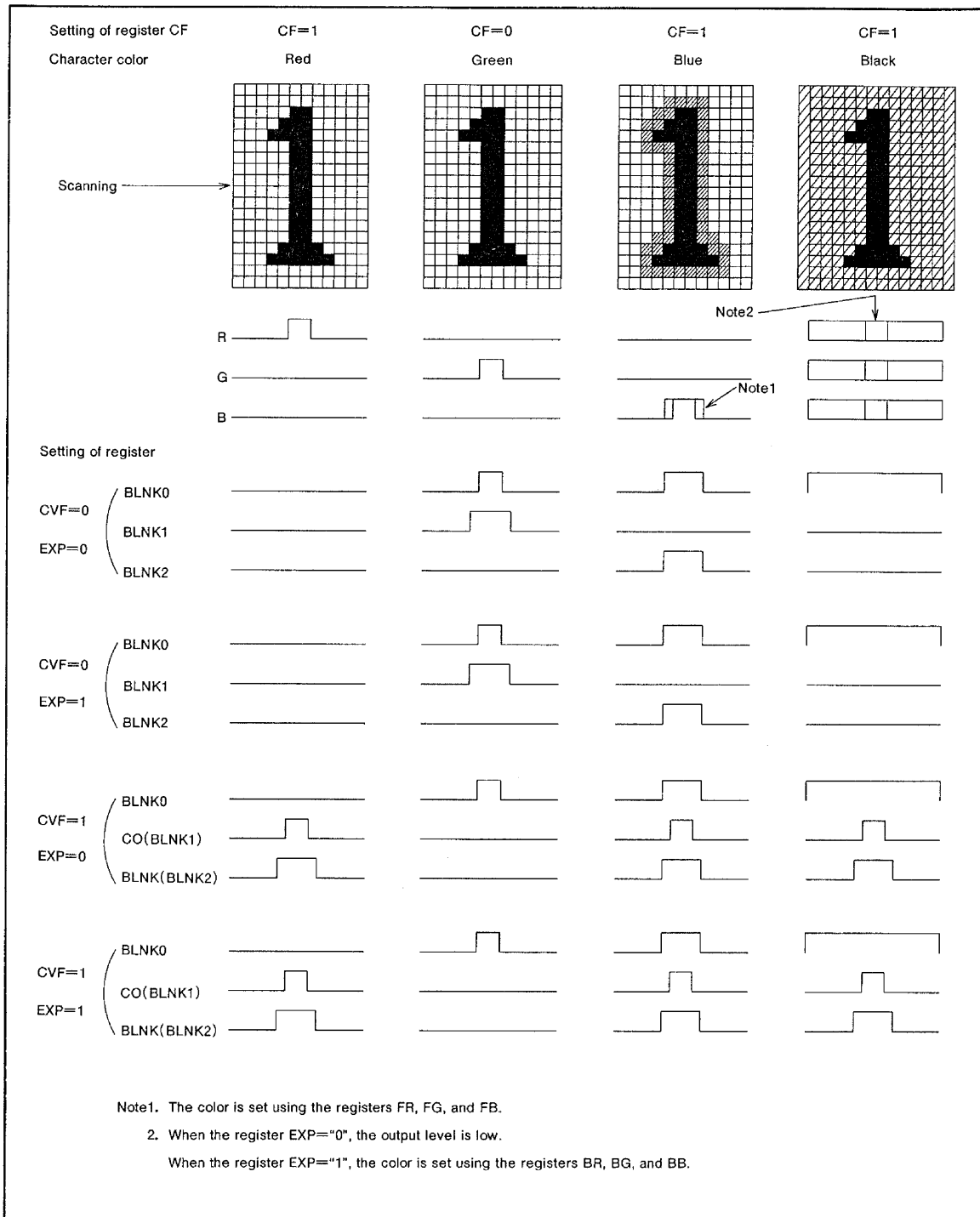


Fig. 4 Display form

MITSUBISHI MICROCOMPUTERS

M35040-XXXFP,M35041-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the serial input function. Example of data setting at

M35040-XXXFP is shown in Figure 5 and example of data setting at M35041-XXXFP is shown in Figure 6.

No.	Memory Contents		DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	
	Address/Data	Addition	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
1	Address (F5 ₁₆)	Setting to address	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	1	
2	Data (F5 ₁₆)	Display OFF	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	
3	Data (00 ₁₆)	Setting to display RAM (addresses 00 ₁₆ to EF ₁₆) and registers (addresses F0 ₁₆ to F5 ₁₆)	0	0	CF	REV	BLINK	B	G	R	0	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	
4	Data (01 ₁₆)		0	0	CF	REV	BLINK	B	G	R	0	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	
⋮			⋮																
242	Data (EF ₁₆)		0	0	CF	REV	BLINK	B	G	R	0	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	
243	Data (F0 ₁₆)		0	0	0	SEPV	PTD	PTD	PTD	PTD	PTD	PTD	PTC	PTC	PTC	PTC	PTC	PTC	PTC
244	Data (F1 ₁₆)		0	0	0	0	0	0	PLTV	PLTH	SYNCR	SPACE		SPACE	SPACE	PTD	PTD	PTD	PTD
245	Data (F2 ₁₆)		0	0	0	BLINK	VP	VP	VP	VP	VP	VP	HP	HP	HP	HP	HP	HP	HP
246	Data (F3 ₁₆)		0	0	0	RB	RG	RR	0	B/F	VSZ	VSZ	VSZ	VSZ	HSZ	HSZ	HSZ	HSZ	HSZ
247	Data (F4 ₁₆)		0	0	0	FB	FG	FR	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP
248	Data (F5 ₁₆)		0	0	0	BB	BG	BR	EXP	CVF	0	0	1	0	BLK	BLK	BLINK	BLINK	BLINK

Fig. 5 Example of data setting at M35040-XXXFP by the serial input function

No.	Memory Contents		DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	
	Address/Data	Addition	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
1	Address (F5 ₁₆)	Setting to address	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	1	
2	Data (F5 ₁₆)	Display OFF	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	
3	Data (00 ₁₆)	Setting to display RAM (addresses 00 ₁₆ to EF ₁₆) and registers (addresses F0 ₁₆ to F5 ₁₆)	0	0	CF	REV	BLINK	B	G	R	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	
4	Data (01 ₁₆)		0	0	CF	REV	BLINK	B	G	R	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	
⋮			⋮																
242	Data (EF ₁₆)		0	0	CF	REV	BLINK	B	G	R	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀	
243	Data (F0 ₁₆)		0	0	0	SEPV	PTD	PTD	PTD	PTD	PTD	PTD	PTC	PTC	PTC	PTC	PTC	PTC	PTC
244	Data (F1 ₁₆)		0	0	0	0	0	0	PLTV	PLTH	SYNCR	SPACE	SPACE	SPACE	PTD	PTD	PTD	PTD	
245	Data (F2 ₁₆)		0	0	0	BLINK	VP	VP	VP	VP	VP	VP	HP	HP	HP	HP	HP	HP	HP
246	Data (F3 ₁₆)		0	0	0	RB	RG	RR	0	B/F	VSZ	VSZ	VSZ	VSZ	HSZ	HSZ	HSZ	HSZ	
247	Data (F4 ₁₆)		0	0	0	FB	FG	FR	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP	DSP
248	Data (F5 ₁₆)		0	0	0	BB	BG	BR	EXP	CVF	0	0	1	0	BLK	BLK	BLINK	BLINK	0

Fig. 6 Example of data setting at M35041-XXXFP by the serial input function

MITSUBISHI MICROCOMPUTERS
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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

SERIAL DATA INPUT TIMING

- (1) Serial data should be input with the LSB first.
- (2) The address consists of 16 bits.
- (3) The data consists of 16 bits.
- (4) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.

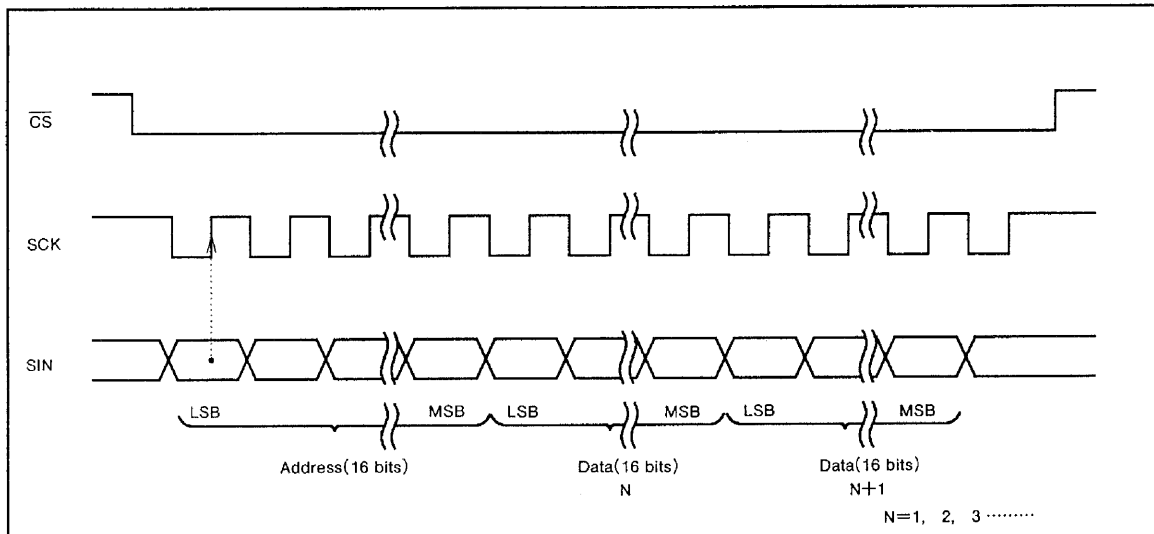


Fig. 7 Serial input timing

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

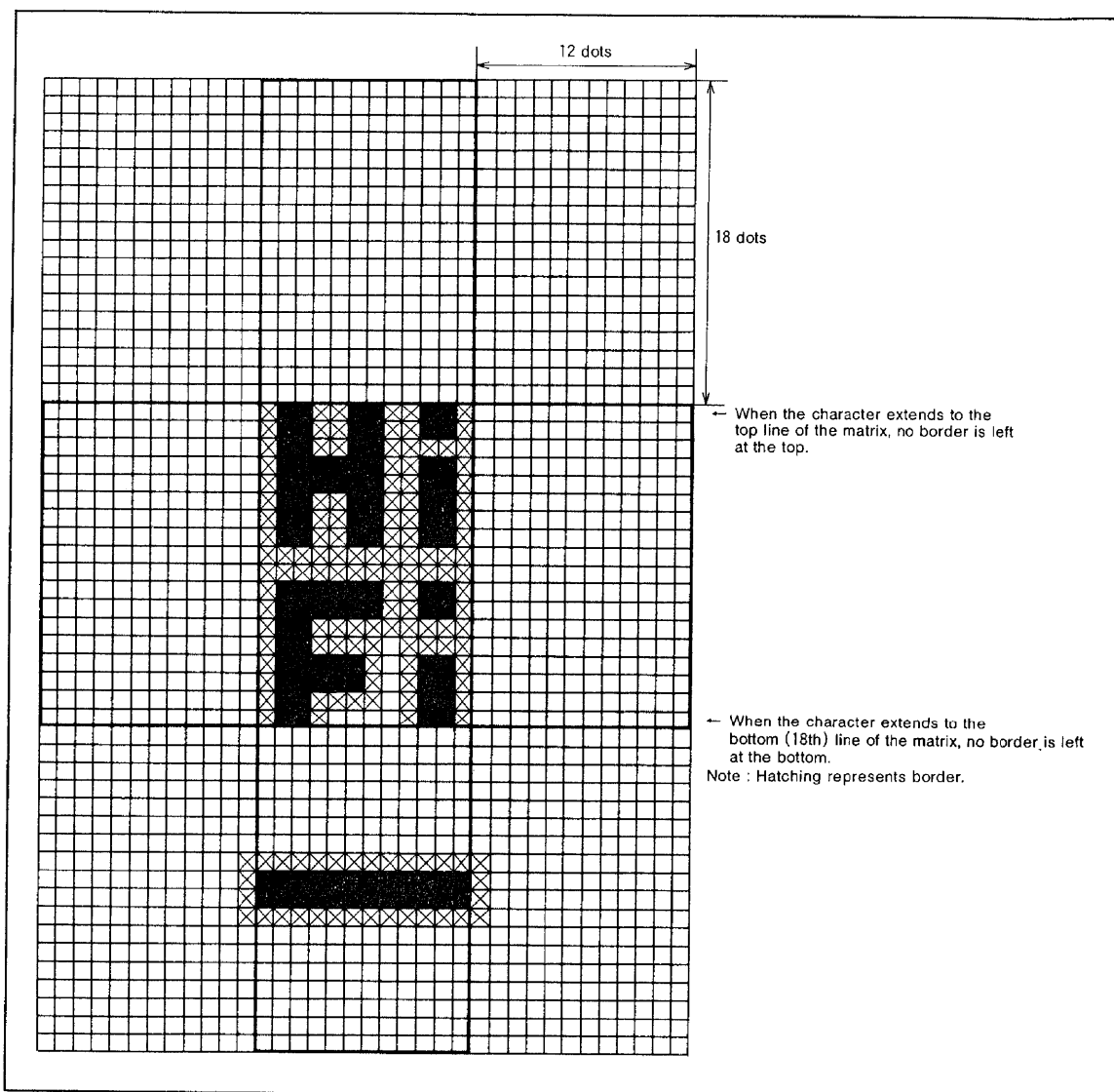


Fig. 8 Character font and border

Character code FF_{16} is fixed as blank, without a background.

MITSUBISHI MICROCOMPUTERS
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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

Timing Requirements ($T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 5 \pm 0.5\text{V}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_w(\text{SCK})$	SCK width	200	—	—	ns	See Figure 9
$t_{su}(\overline{\text{CS}})$	CS setup time	200	—	—	ns	
$t_h(\overline{\text{CS}})$	CS hold time	2	—	—	μs	
$t_{su}(\text{SIN})$	SIN setup time	200	—	—	ns	
$t_h(\text{SIN})$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	10	—	—	μs	

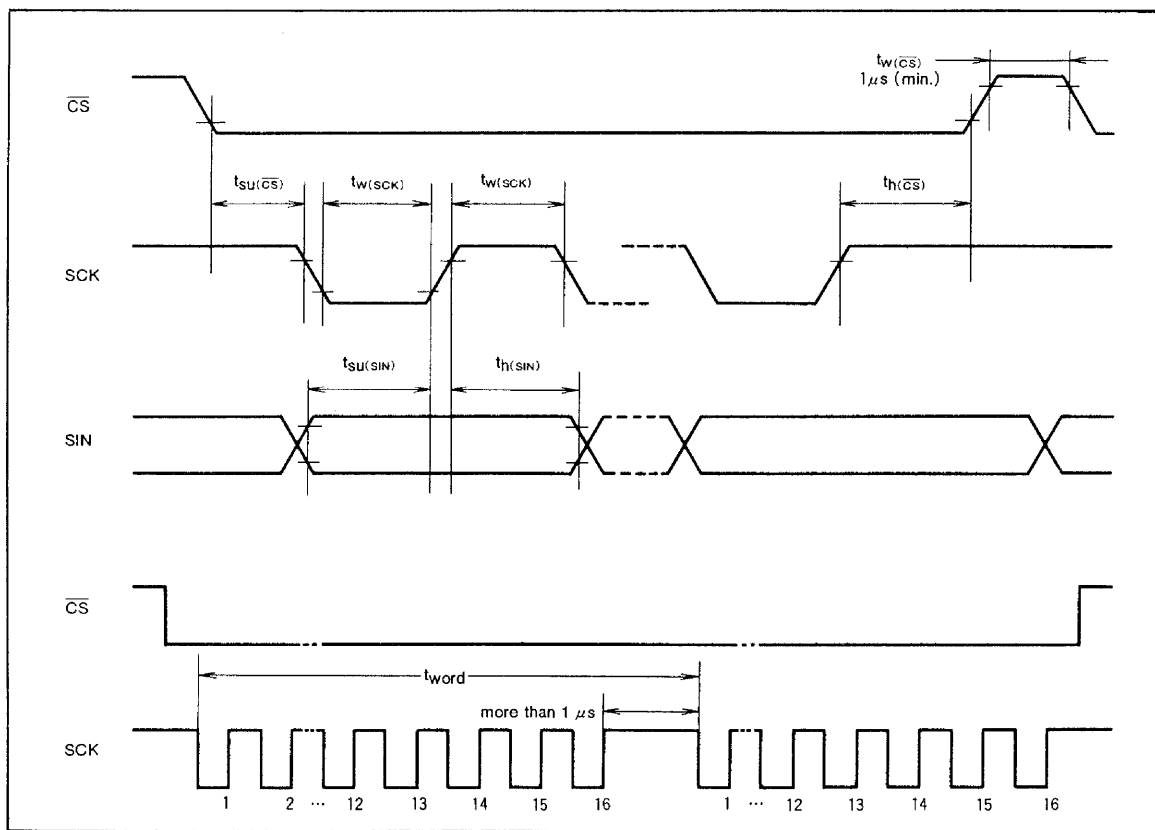


Fig. 9 Serial input timing requirements

MITSUBISHI MICROCOMPUTERS
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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	-0.3 to 6.0	V
V_I	Input voltage		$V_{SS}-0.3 \leq V_I \leq V_{DD}+0.3$	V
V_O	Output voltage		$V_{SS} \leq V_O \leq V_{DD}$	V
P_d	Power dissipation	$T_a=25^\circ\text{C}$	150	mW
T_{opr}	Operating temperature		-20 to 70	$^\circ\text{C}$
T_{stg}	Storage temperature		-40 to 125	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($V_{DD}=5\text{V}$, $T_a=-20$ to 70°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply voltage	3.0	5.0	5.5	V
V_{IH}	"H" level input voltage SIN, SCK, $\overline{\text{CS}}$, $\overline{\text{AC}}$, HOR, VERT	$0.8V_{DD}$	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage SIN, SCK, $\overline{\text{CS}}$, $\overline{\text{AC}}$, HOR, VERT	0	0	$0.2V_{DD}$	V
f_{OSC1}	Oscillating frequency for display	6.3	7.0	7.7	MHz

ELECTRICAL CHARACTERISTICS ($V_{DD}=5\text{V}$, $f_{OSC1}=7.0\text{MHz}$, $T_a=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	$T_a=-20$ to 70°C	3.0	5.0	5.5	V
I_{DD}	Supply current	$V_{DD}=5.5\text{V}$	—	10	20	mA
V_{OH}	"H" level output voltage, P0 to P9	$V_{DD}=4.5\text{V}$, $I_{OH}=0.4\text{mA}$	3.5	—	—	V
V_{OL}	"L" level output voltage, P0 to P9	$V_{DD}=4.5\text{V}$, $I_{OL}=0.4\text{mA}$	—	—	0.4	V
R_I	Pull-up resistance SCK, AC, CS, SIN		10	30	100	$\text{k}\Omega$

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

Note for Supplying Power

Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35040-XXXFP/M35041-XXXFP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin is hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 10.

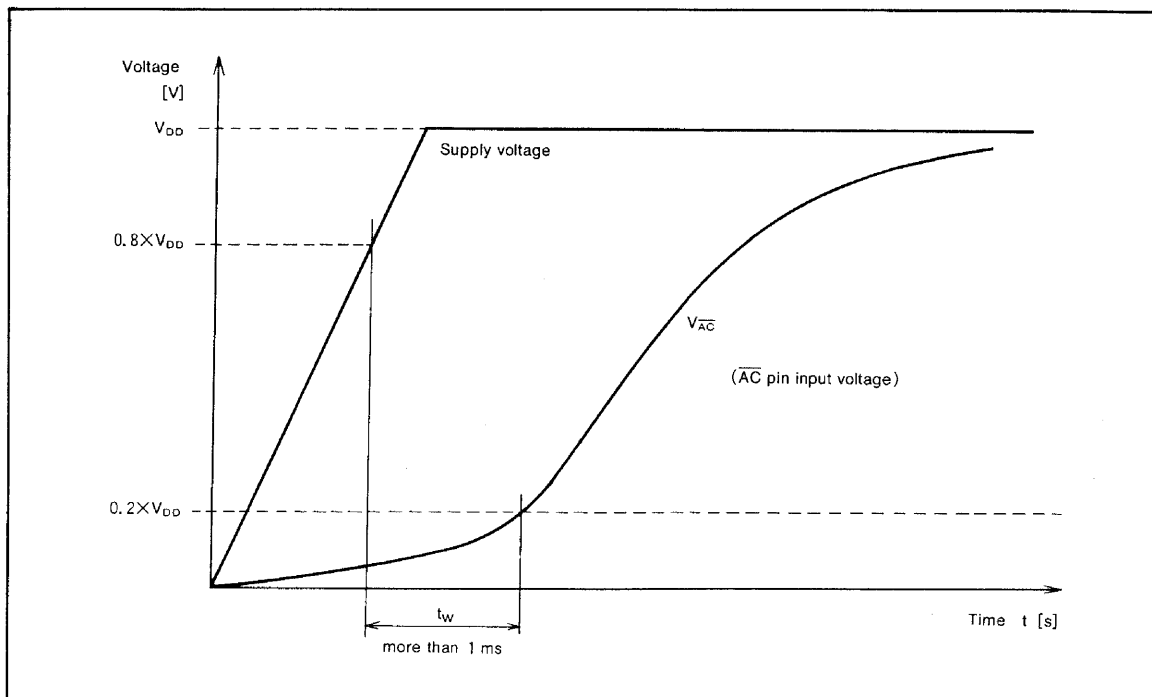


Fig. 10 Timing of power supplying to $\overline{AC}$ pin

After supplying the power (V_{DD} and V_{SS}) to M35040-XXXFP/M35041-XXXFP and the supply voltage becomes more than $0.8 \times V_{DD}$, it needs to keep V_{IL} time; t_w of the $\overline{AC}$ pin for more than 1ms.

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{DD} pin and V_{SS} pin using a heavy wire.

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

STANDARD ROM TYPE : M35040-001FP

M35040-001FP is a standard ROM type of M35040-XXXFP.

The character patterns are fixed to the contents of Figure 11 to 13.

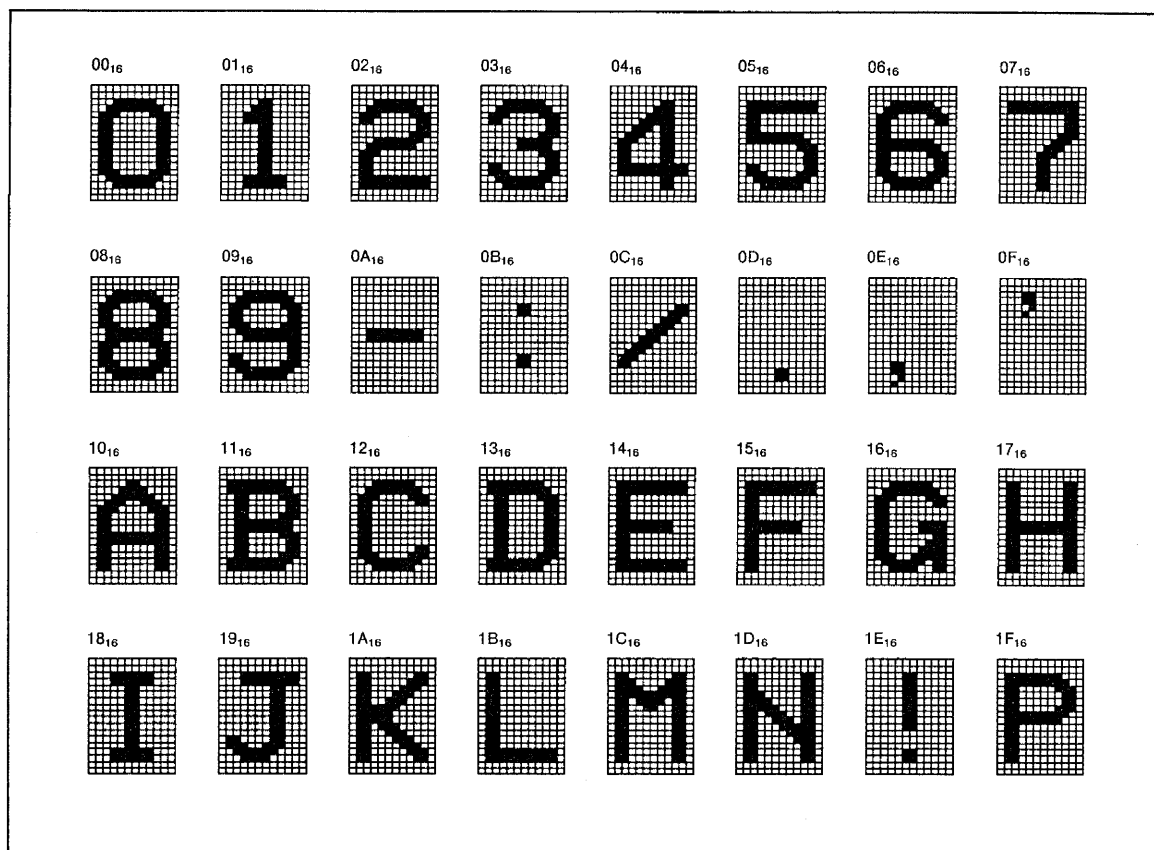


Fig. 11 M35040-001FP character patterns (1)

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SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

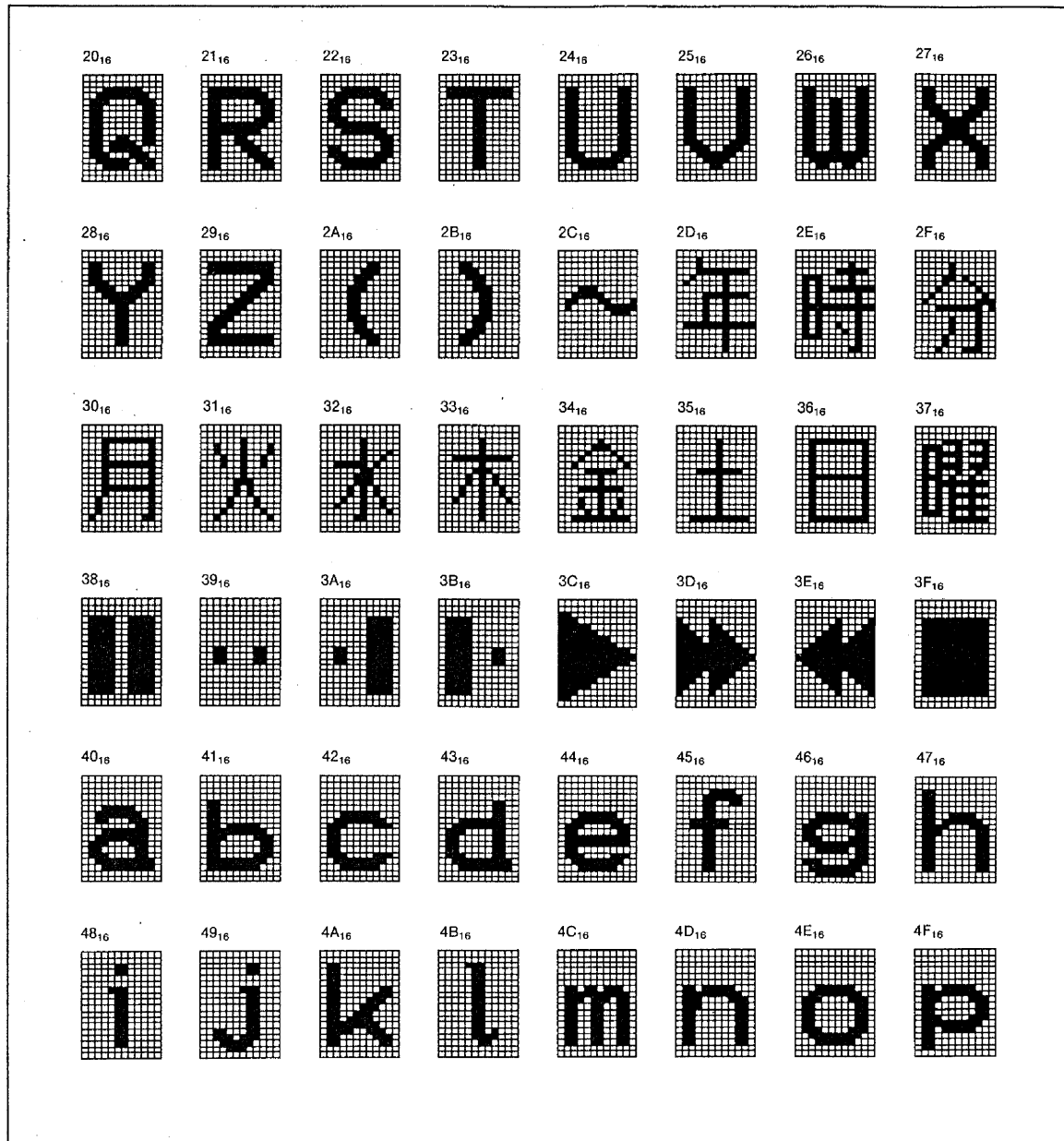


Fig. 12 M35040-001FP character patterns (2)

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M35040-XXFP,M35041-XXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

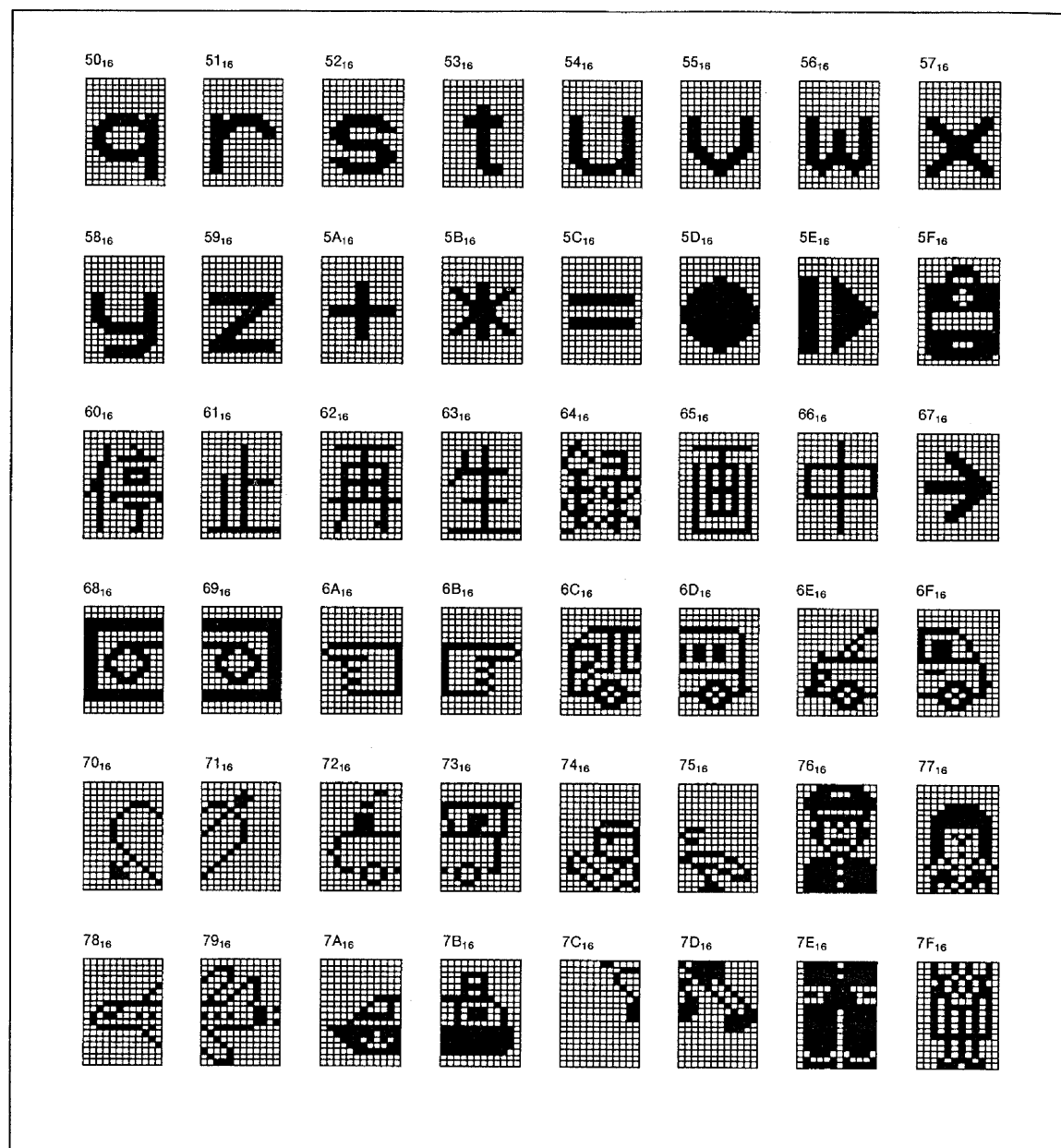


Fig. 13 M35040-001FP character patterns (3)

MITSUBISHI MICROCOMPUTERS
M35040-XXXFP, M35041-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

STANDARD ROM TYPE : M35041-001FP

M35041-001FP is a standard ROM type of M35041-XXXFP.
The character patterns are fixed to the contents of Figure 14 to 19.

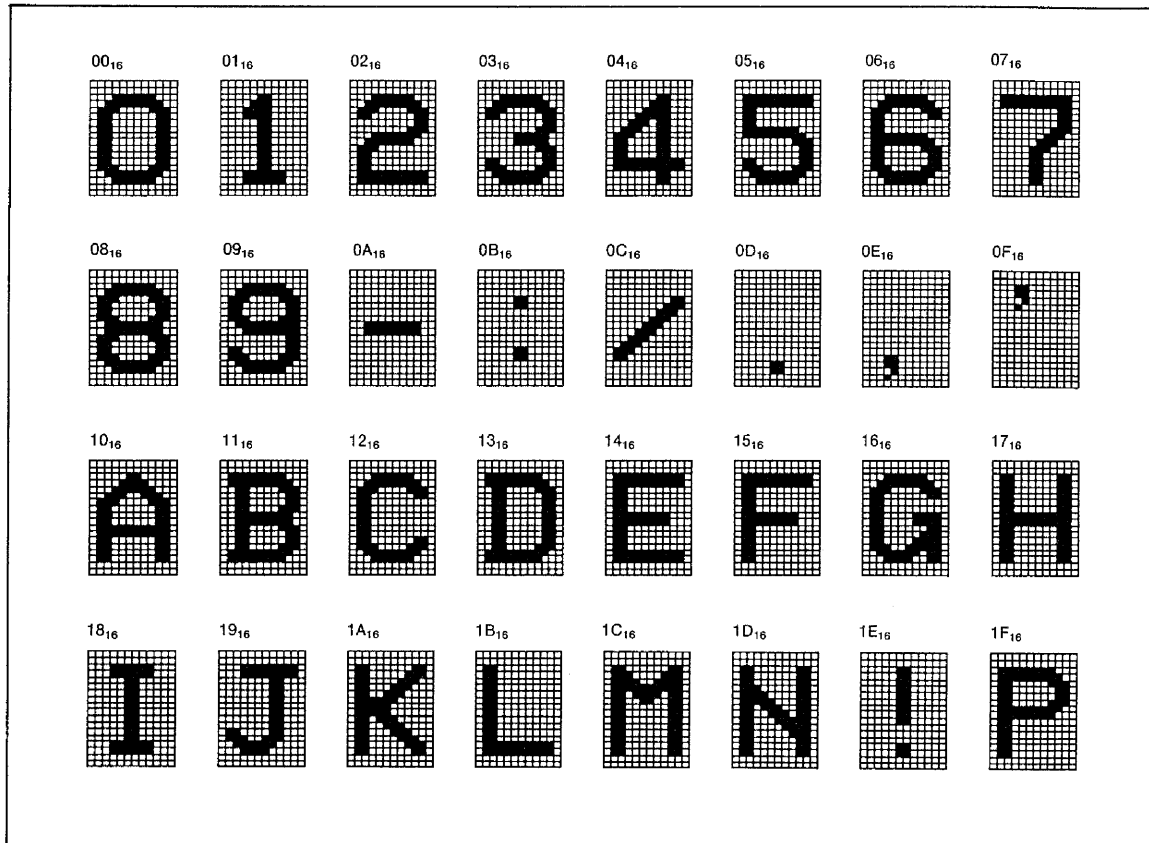


Fig. 14 M35041-001FP character patterns (1)

MITSUBISHI MICROCOMPUTERS
M35040-XXXFP, M35041-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

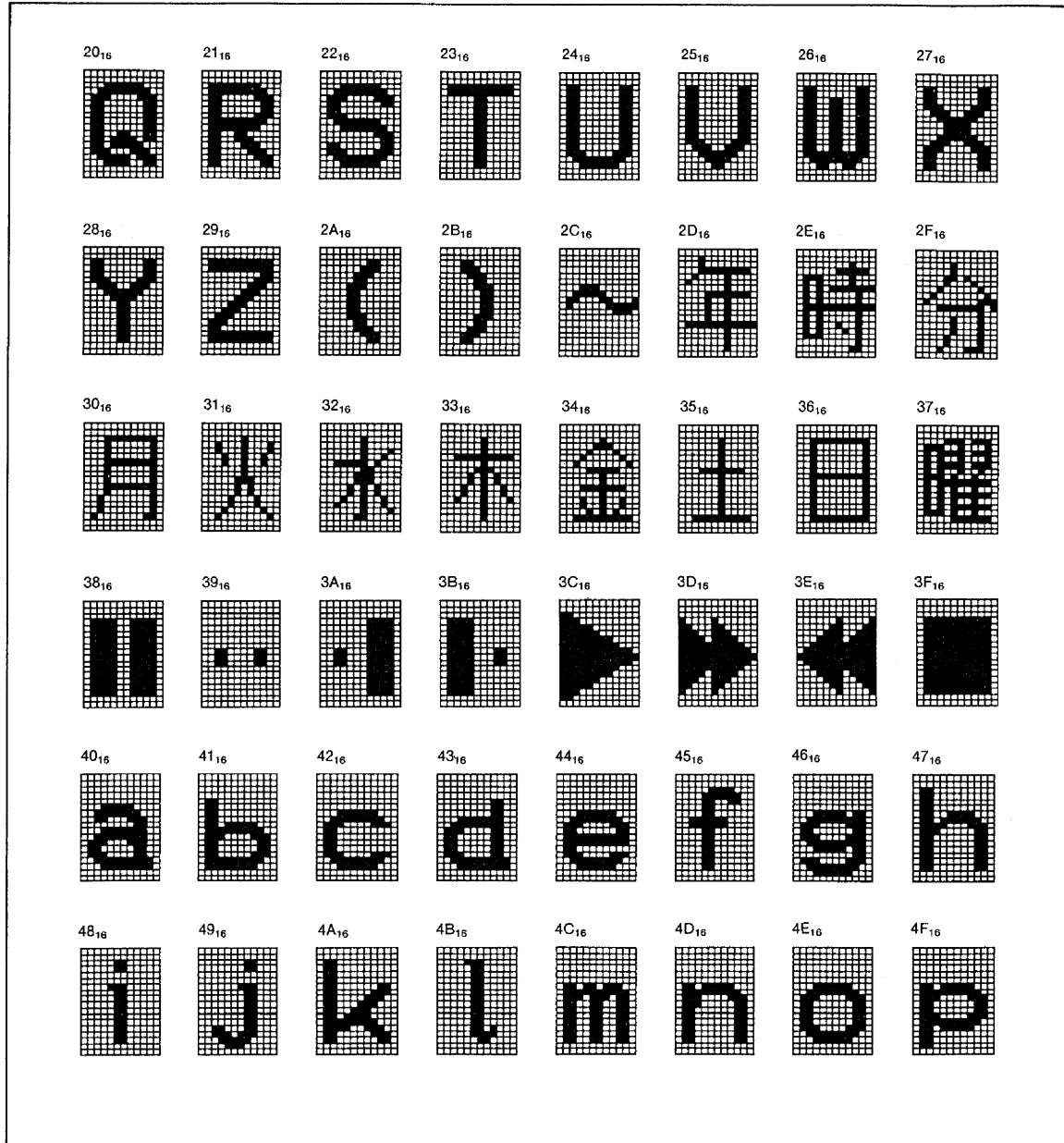


Fig. 15 M35041-001FP character patterns (2)

mitsubishi microcomputers
M35040-XXXFP, M35041-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

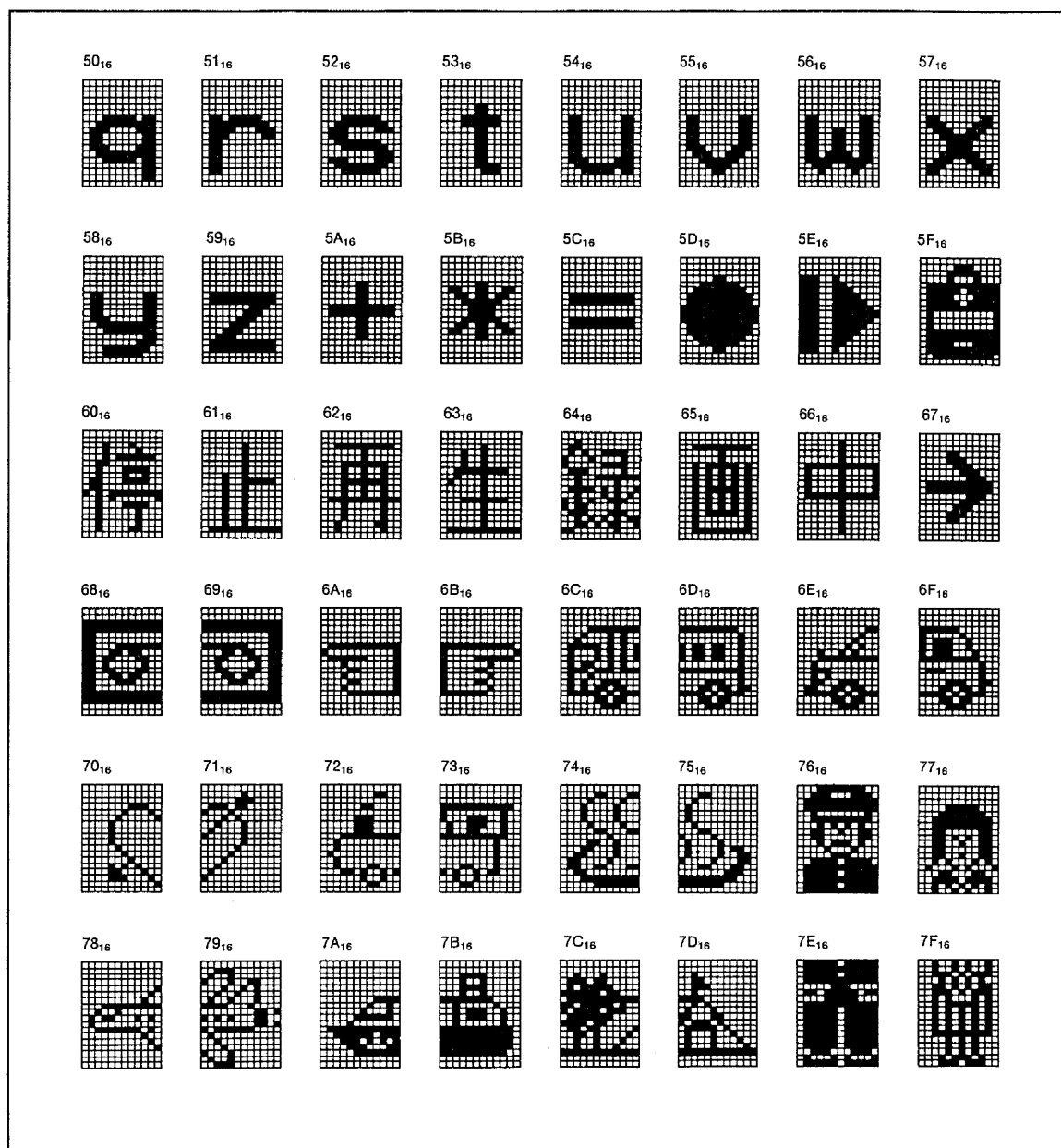


Fig. 16 M35041-001FP character patterns (3)

MITSUBISHI MICROCOMPUTERS
M35040-XXXFP,M35041-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

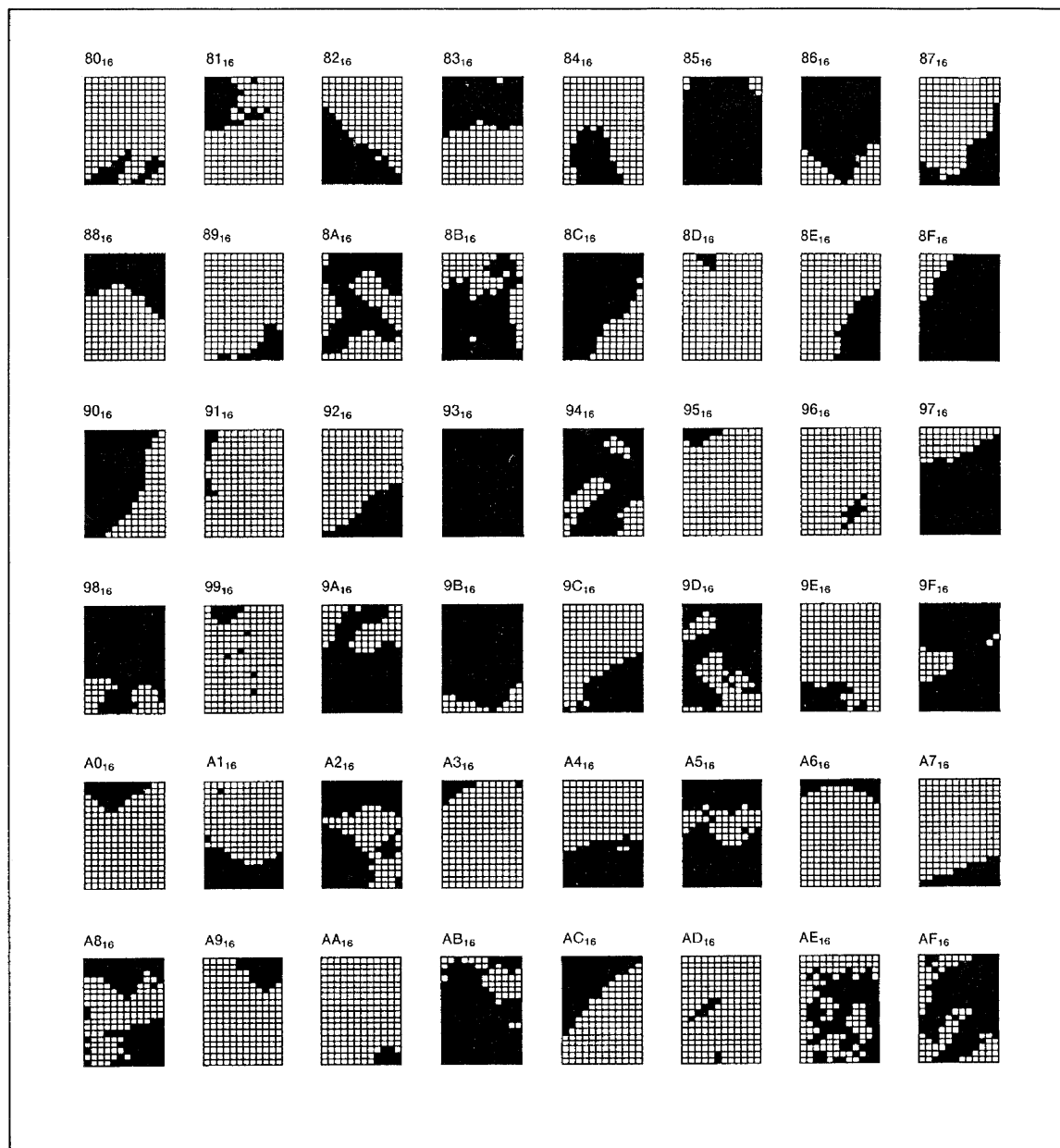


Fig. 17 M35041-001FP character patterns (4)

MITSUBISHI MICROCOMPUTERS
M35040-XXXFP, M35041-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

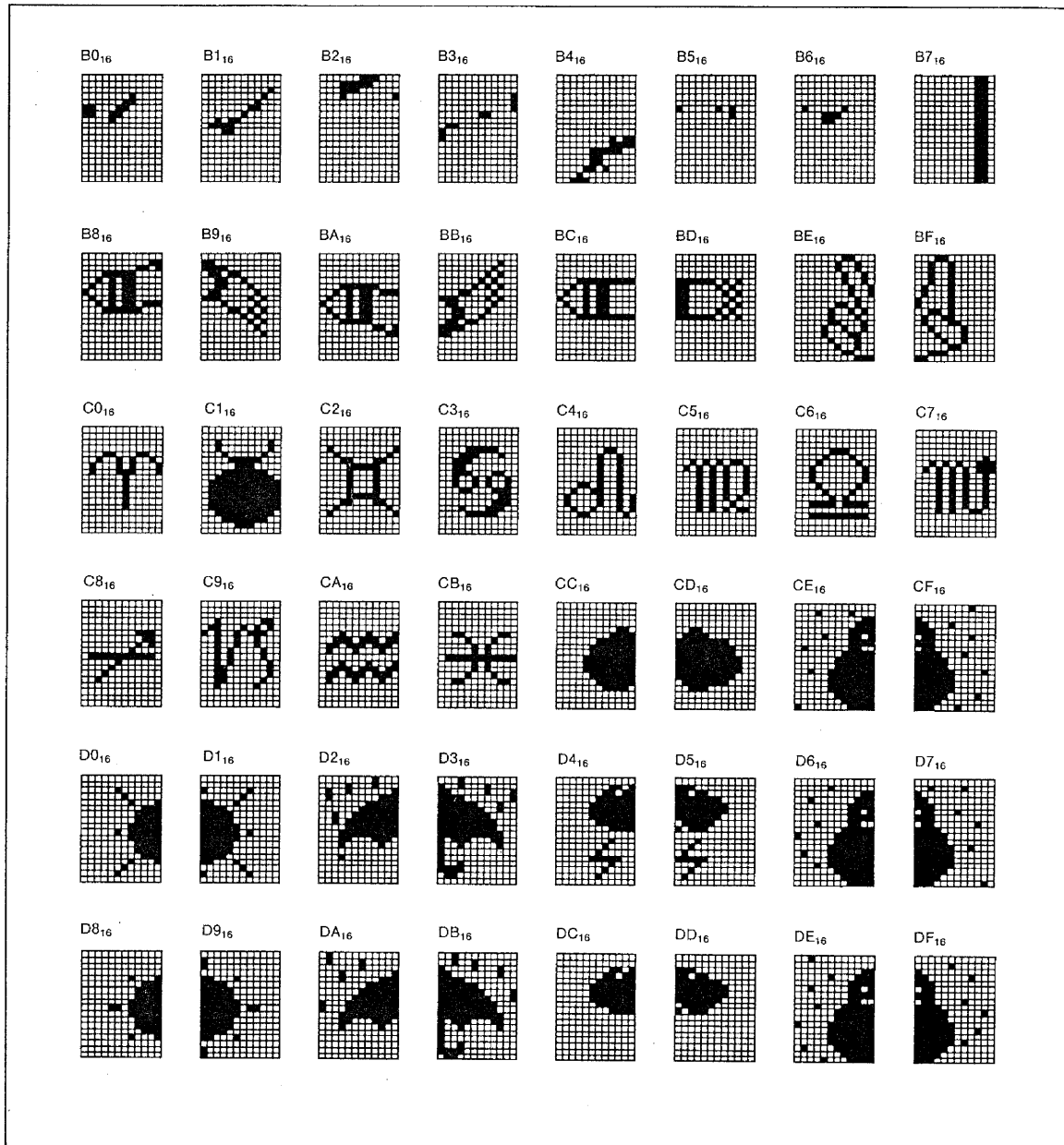


Fig. 18 M35041-001FP character patterns (5)

MITSUBISHI MICROCOMPUTERS
M35040-XXXFP, M35041-XXXFP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

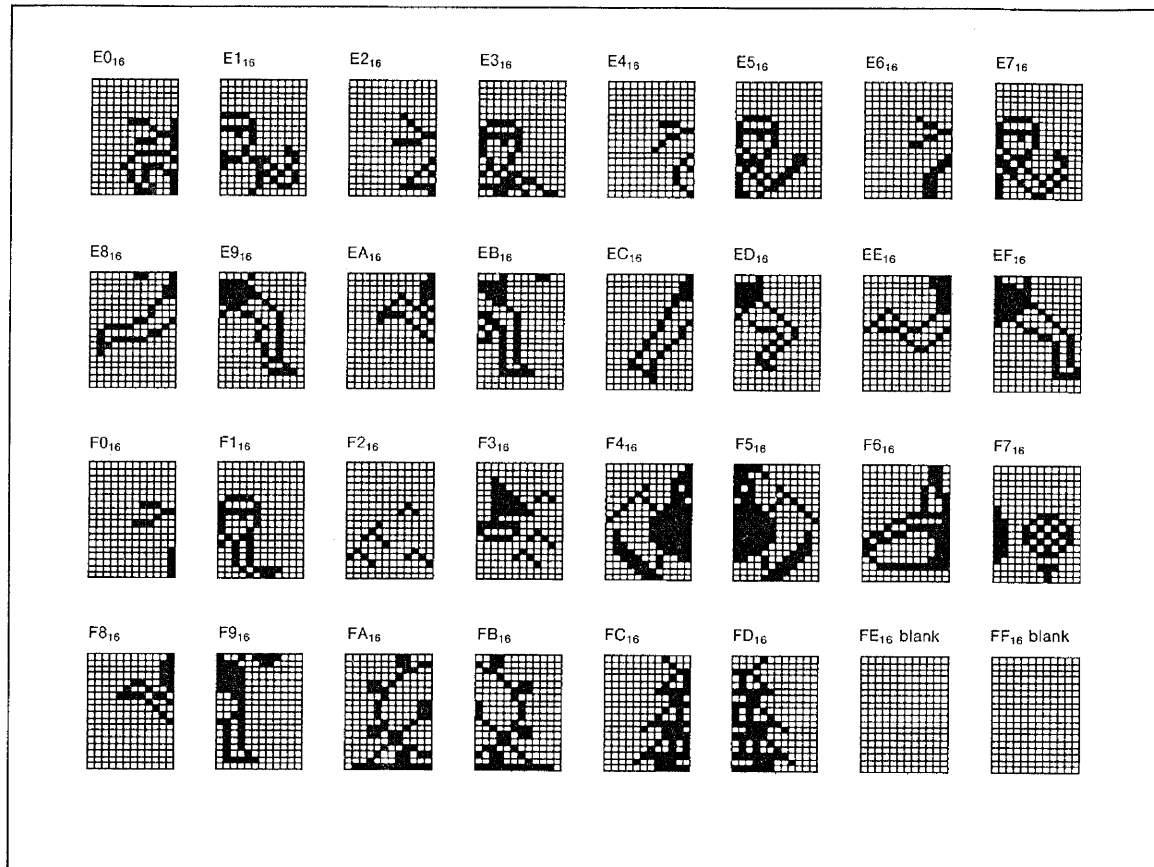


Fig. 19 M35041-001FP character patterns (6)