

# **RM805**

## Power Amplifier Module, 3.5 Volts, Broadband

The RM805 Power Amplifier (PA) is a fully matched 28-pin surface mount module designed for Private Mobile Radio (PMR), Wireless Local Loop (WLL), and Time Division Multiple Access/Advanced Mobile Phone Service (TDMA/AMPS) mobile units operating in the 806-849 MHz cellular bandwidth. Microwave Monolithic Integrated Circuits (MMICs), comprised of Gallium Arsenide (GaAs) and CMOS, contain all active circuitry in the module, which includes on-board bias circuitry as well as input and interstage matching circuits. The output match is realized off-chip within the module package to optimize efficiency and high power performance ( $P_{3db\_sat}\cong 35.8~dBm$ ) into a  $50~\Omega$  load.

This device, manufactured with Skyworks' GaAs Heterojunction Bipolar Transistor (HBT) and silicon CMOS processes, provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the RM805 can be supplied directly from a single cell lithium-ion or other suitable battery with a nominal output 3.5 Volts.

No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

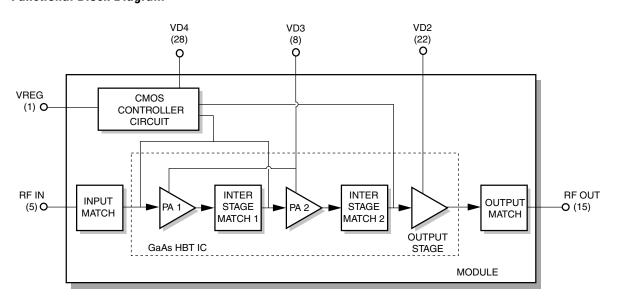
#### **Distinguishing Features**

- Low voltage positive bias supply
- Good linearity
- · High efficiency
- Dual mode operation
- · Large dynamic range
- 28-pin LCC package (10 x 13.97 x 1.7 mm)
- Power down control

### **Applications**

- PMR (806-825 MHz)
- TETRA (806–825 MHz)
- TDMA (824–849 MHz)
- AMPS (824-849 MHz)
- Wireless Local Loop

## **Functional Block Diagram**



Electrical Specifications RM803

Power Amplifier Module, 3.5 Volts, Broadband

## **Electrical Specifications**

The following tables list the electrical characteristics of the RM805 Power Amplifier. Table 1 lists the absolute maximum rating for continuous operation. Table 2 lists the recommended operating conditions for achieving the electrical performance listed in Table 3, which depicts the electrical performance of the RM805 Power Amplifier over the recommended operating conditions.

Table 1. Absolute Maximum Ratings<sup>(1)</sup>

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power <sup>(2)</sup>	Pin	_	-8.0	11.0	dBm
Supply Voltage	Vcc	_	3.5	6.9 <sup>(3)</sup>	Volts
Regulation Voltage	Vreg	0.0	2.75	Vcc <sup>(4)</sup>	Volts
Case Operating Temperature	Tc	-30	+25	+110	°C
Storage Temperature	Tstg	<b>-</b> 55	_	+125	°C

#### NOTE(S):

**Table 2. Recommended Operating Conditions** 

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage	Vcc	3.0	3.5	4.4	Volts
Regulation Voltage	Vreg	2.65	2.75	2.85	Volts
Operating Frequency	Fo	806	_	849	MHz
Continuous RMS Output Power	PoRMS		29.0	31.0	dBm
Operating Temperature	То	-30	+25	+85	°C

<sup>(1)</sup> No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.

<sup>(2)</sup> Pulsed operation at 25% duty cycle.

<sup>(3)</sup> When amplifier is biased off (Vreg = 0 V)

<sup>(4)</sup> Voltage on Vreg pin may not exceed the applied Vcc voltage.

Table 3. Electrical Specifications for TDMA/AMPS Nominal Operating Conditions<sup>(1)</sup>

Characteristics	Condition	Symbol	Minimum	Typical	Maximum	Unit
Quiescent current	Vreg = 2.75	Iq	332	370	450	mA
Gain	Po = 29 dBm	Gp	35.5	38.0	40.0	dB
Saturated Output Power	Duty Cycle ≤ 25% Gain Compression ≤ 3 dB	P3dB sat	35.3	35.8	_	dBm
Power Added Efficiency	Po = 29 dBm Po = P3dB sat	PAEa PAEd	21.0 48.0	23.0 52.0		% %
Harmonic Levels Second Third Fourth	Po ≤ P3db sat Po ≤ P3db sat Po ≤ P3db sat	AFo2 AFo3 AFo4	_ _ _	-10.0 -30.0 -30.0	_ _ _	dBm dBm dBm
Noise Power in RX Band Fc + 30 MHz, BW = 18 kHz	Po ≤ 29 dBm	RxBN	_	_	-85.0	dBm/Hz
Noise Figure	_	NF	_	8.0	_	dB
Input Voltage Standing Wave Ratio	_	VSWR	_	1.3:1	2.0:1	_
Stability (Spurious output)		S	10.0:1	_	-36.0	dBm
Ruggedness – No damage	Po ≤ 29 dBm	Ru	15.0:1	_	_	VSWR

NOTE(S):

(1) Vcc = +3.5 V, Vreg = +2.75 V, Freq = 815 MHz, Tc = 25 °C, Vreg pulsed at 25% duty cycle, unless otherwise specified.

# **Evaluation Board Description**

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the RM805, the evaluation board schematic and assembly diagram are included for preliminary analysis and design. Figure 1 shows the basic schematic of the board for the 806 MHz to 849 MHz range and Figure 2 illustrates the board layout.

Figure 1. Evaluation Board Schematic

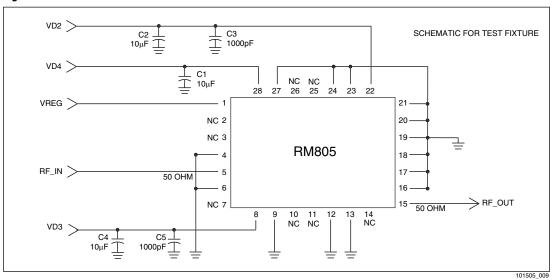
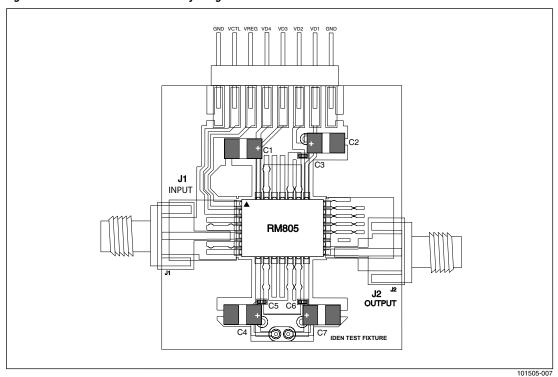


Figure 2. Evaluation Board Assembly Diagram

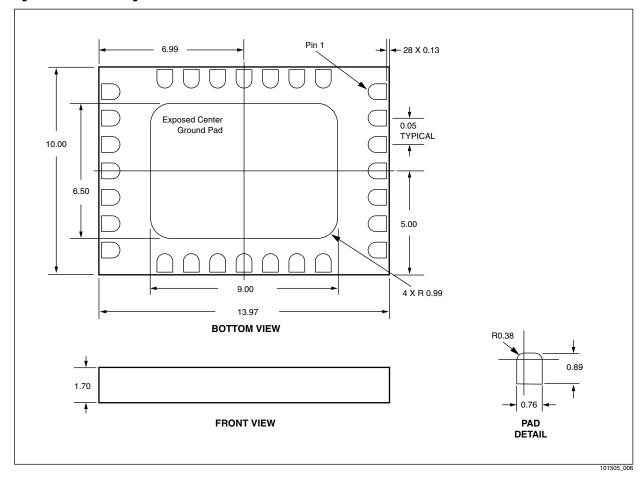


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# **Package Dimensions and Pin Descriptions**

The RM805 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board.

Figure 3. RM805 Package Dimensions



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Table 4. Pin Names and Descriptions

1 VREG1 Regulated bias enable control voltage, 0.0=Off, 2.75V=On 2 VCNTL Reserved for gain adjust control, currently a floating pad 3 GND1 Low Inductance Ground Connection 4 GND2 Low Inductance Ground Connection 5 RFIN 806-849 MHz RF input signal (typically -8 dBm) 50 Ohm 6 GND3 Low Inductance Ground Connection	
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7 VDF00 Decembed for additional VDF0 1 1 1 1 1 1 1 1 1	
7 VREG2 Reserved for additional VREG signal, currently a floating pad	
8 VD3 Supply voltage for driver collector bias (typically 3.5V)	
9 GND4 Low Inductance Ground Connection	
10 RSVD Used to identify device, Skyworks pad must float	
11 GND5 Low Inductance Ground Connection	
12 GND6 Low Inductance Ground Connection	
13 GND7 Low Inductance Ground Connection	
14 VD1 Unused supply voltage, currently a floating pad	
15 RFOUT 806-849 MHz RF output signal (typically +29 dBm) 50 Ohm	
16 GND8 Low Inductance Ground Connection	
17 GND9 Low Inductance Ground Connection	
18 GND10 Low Inductance Ground Connection	
19 GND11 Low Inductance Ground Connection	
20 GND12 Low Inductance Ground Connection	
21 GND13 Low Inductance Ground Connection	
22 VD2 Supply voltage for output (final) stage collector bias (typically 3.5V)	
GND14 Low Inductance Ground Connection	
24 GND15 Low Inductance Ground Connection	
25 GND16 Low Inductance Ground Connection	
26 GND17 Low Inductance Ground Connection	
27 GND18 Low Inductance Ground Connection	
28 VD4 Supply voltage for base bias circuitry to all stages (typically 3.5V)	

NOTE(S): Center attachment pad must have a low inductance and low thermal resistance connection to the customer's printed circuit board ground plane.

## **Package and Handling Information**

Because of its sensitivity to moisture absorption, this device package is baked and vacuum packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The RM805 is capable of withstanding an MSL 3/225 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 225 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 225 °C for more than 10 seconds. For details on both attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J–STD–020A*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to *Application Note: Tape and Reel, Document Number 101568*.

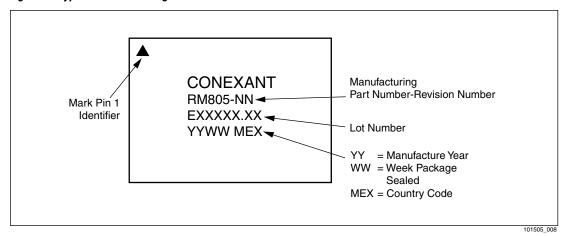


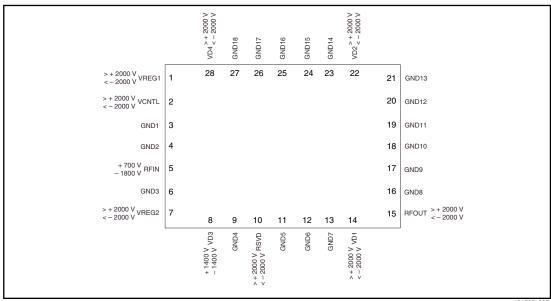
Figure 4. Typical Case Markings

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## **Electrostatic Discharge Sensitivity**

The RM805 is a Class I device. Figure 5 lists the Electrostatic Discharge (ESD) immunity level for each pin of the RM805 product. The numbers in Figure 5 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation. The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. Since 2000 volts represents the maximum measurement limit of the test equipment used, pins marked > 2000 V pass 2000V ESD stress.

Figure 5. ESD Sensitivity Areas



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Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards which fail devices only after "the pin fails the electrical specification limits" or "the pin becomes completely non-functional". Skyworks employs most stringent criteria, fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in Table 5.

Table 5. Precautions for GaAs ICs with ESD Thresholds Greater Than 200V But Less Than 2000V

Personnel Grounding Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges	Facility Relative Humidity Control and Air Ionizers Dissipative Floors (less than $10^9~\Omega$ to GND)	
Protective Workstation	Protective Packaging & Transportation	
Dissipative Table Tops	Bags and Pouches (Faraday Shield)	
Protective Test Equipment (Properly Grounded)	Protective Tote Boxes (Conductive Static Shielding)	
Grounded Tip Soldering Irons	Protective Trays	
Conductive Solder Suckers	Grounded Carts	
Static Sensors	Protective Work Order Holders	

## **Ordering Information**

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
RM805	RM805-15	15	10.0 x 13.97 x 1.7mm	–30 °C to +85 °C

## **Revision History**

Revision	Level	Date	Description
А		May 2001	Initial Release
В		August 2001	Revise: Product Description/Applications
С		June 17, 2002	Revise: ESD data; Update: References Information

### References

Application Note: Tape and Reel, Document Number 101568

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752

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