19-3680; Rev 1; 12/07

EVALUATION KIT AVAILABLE

10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset

General Description

The MAX9225/MAX9226 serializer/deserializer chipset reduces wiring by serializing 10 bits onto a single differential pair. Ten bits are serialized in each cycle of the parallel input clock resulting in a 100Mbps to 200Mbps net serial-data rate. The MAX9225 serializes the 8-bit YUV, HSYNC and VSYNC outputs from a camera mounted in the flip part of the phone, reducing wiring through the hinge to the baseband processor in the base of the phone. The 2-wire serial interface uses low-current differential signaling (LCDS) for low EMI, high common-mode noise immunity, and ground-shift tolerance. The MAX9225/MAX9226 automatically identify the word boundary in the serial data in case of signal interruption. The MAX9226 power-down is controlled by the MAX9225. The MAX9225/MAX9226 consume 3.5µA or less in power-down mode.

The MAX9225 serializer operates from a single +2.375V to +3.465V supply and accepts +1.71V to +3.465V inputs. The MAX9226 deserializer operates from a +2.375V to +3.465V core supply and has a separate output buffer supply (V_{DDO}), allowing +1.71V to +3.465V output high levels.

The MAX9225/MAX9226 are specified over the -40°C to +85°C extended temperature range and are available in 16-pin TQFN (3mm x 3mm x 0.8mm) packages with an exposed paddle.

Applications

Cell Phone Cameras

Digital Cameras

Features

- **Ideal for Serializing Cell Phone Camera Parallel Interface**
- **MAX9225 Serializes 8-Bit YUV, HSYNC, and VSYNC**
- **LCDS Rejects Common-Mode Noise**
- **Automatic Location of Word Boundary After Signal Interruption**
- **Power-Down Control Through the Serial Link**
- **Power-Down Supply Current**
  0.5µA (max) for MAX9225
  3.0µA (max) for MAX9226
- **+2.375V to +3.465V Core Supply Voltage**
- **Parallel I/O Interfaces Directly to 1.8V to 3.3V Logic**
- **±15kV Human Body Model ESD Protection**
- **-40°C to +85°C Operating Temperature Range**

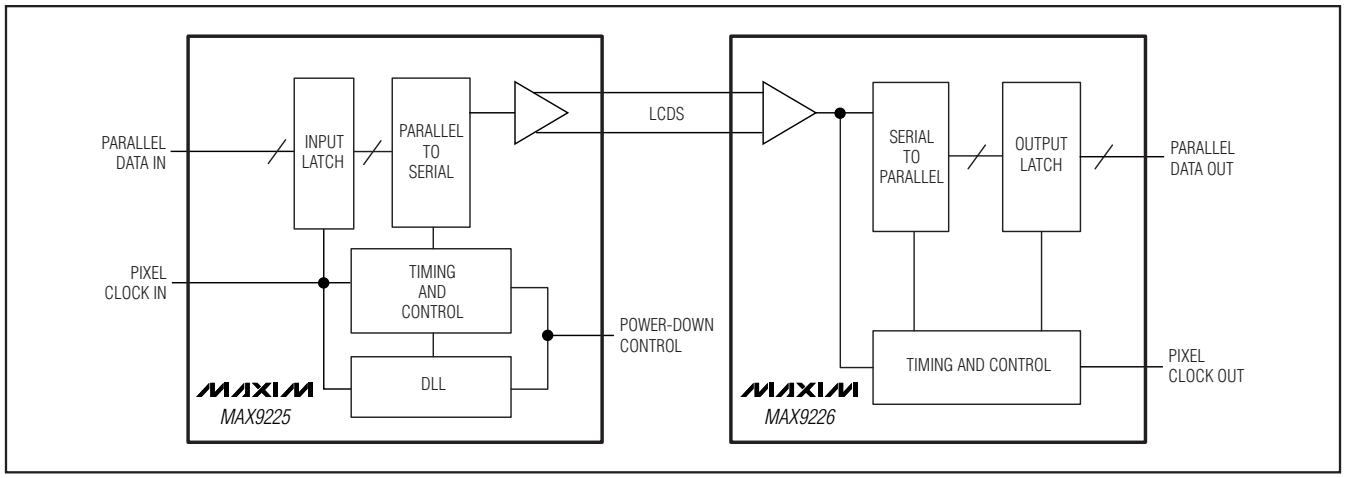
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE	TOP MARK
MAX9225ETE	-40°C to +85°C	16 TQFN-EP*	T1633-4	ADO
MAX9225ETE+	-40°C to +85°C	16 TQFN-EP*	T1633-4	ADO
MAX9226ETE	-40°C to +85°C	16 TQFN-EP*	T1633-4	ADX
MAX9226ETE+	-40°C to +85°C	16 TQFN-EP*	T1633-4	ADX

+Denotes lead-free package.
**EP = Exposed paddle.*

Pin Configurations appear at end of data sheet.

Typical Application Circuit



10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.5V to +4.0V
V_{DDO} to GND.....-0.5V to +4.0V
Serial Interface (SDO+, SDO-, SDI+, SDI-) to GND .....-0.5V to +4.0V
Single-Ended Inputs (DIN_, PCLKIN, $\overline{PWRDN}$) to GND .....-0.5V to (V_{DD} + 0.5V)
Single-Ended Outputs (DOUT_, PCLKOUT) to GND .....-0.5V to (V_{DDO} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (3mm x 3mm x 0.8mm)
Multilayer PCB (derate 20.8mW/°C above +70°C).....1667mW
Single-Layer PCB (derate 15.6mW/°C above +70°C).....1250mW
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C
ESD Protection (Human Body Model)
SDO+, SDO-, SDI+, SDI- to GND .....> ±15kV
All Other Pins to GND .....> ±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (MAX9225)

(V_{DD} = +2.375V to +3.465V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +2.5V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (PCLKIN, DIN_, $\overline{PWRDN}$)							
High-Level Input Voltage	V_{IH}			1.19		V_{DD} + 0.3	V
Low-Level Input Voltage	V_{IL}			-0.3		+0.3	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DD}		-20		+20	µA
		-0.3V ≤ V_{IN} < 0V		-100		+100	
		V_{DD} < V_{IN} ≤ (V_{DD} + 0.3V)					
LCDS OUTPUT (SDO+, SDO-)							
Differential Output Current	I_{ODH}	High level		575	643	880	µA
	I_{ODL}	Low level		200	229	300	
Output Short-Circuit Current	I_{OS}	Shorted to 0V or V_{DD}				880	µA
POWER SUPPLY							
Supply Current	I_{DD}	V_{DD} = 2.5V	PCLKIN = 10MHz, 100Mbps		4.7	8.2	mA
			PCLKIN = 20MHz, 200Mbps		6.2	8.2	
Worst-Case Pattern Supply Current	I_{DDW}	V_{DD} = 2.5V, Figure 1	PCLKIN = 10MHz, 100Mbps		4.7	10.6	mA
			PCLKIN = 20MHz, 200Mbps		6.2	10.6	
Power-Down Supply Current	I_{DDZ}	All inputs = low				0.5	µA

DC ELECTRICAL CHARACTERISTICS (MAX9226)

(V_{DD} = +2.375V to +3.465V, V_{DDO} = +1.71V to +3.465V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = V_{DDO} = +2.5V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED OUTPUTS (PCLKOUT, DOUT_)							
High-Level Output Voltage	V_{OH}	V_{DDO} = +2.375V to +3.465V, I_{OH} = -1mA		0.8 x V_{DDO}			V
Low-Level Output Voltage	V_{OL}	V_{DDO} = +2.375V to +3.465V, I_{OL} = 1mA				0.2	V
Output Short-Circuit Current	I_{OS}	Output shorted to ground	V_{DDO} = 2.375V	-2			mA
			V_{DDO} = 3.135V	-9			
			V_{DDO} = 3.465V			-25	
LCDS INPUT (SDI+, SDI-)							
Differential Input-Current Threshold	I_{ID}				400		µA
Common-Mode Input Current	I_{IC}			-300	±400	+300	µA
Differential Input Impedance	Z_{ID}	I_{IC} = 0µA, V_{DD} = 3.3V ±5%		69	90	114	Ω
		I_{IC} = 0µA, V_{DD} = 2.8V ±5%		82	108	137	
		I_{IC} = 0µA, V_{DD} = 2.5V ±5%		95	125	161	
		I_{IC} = ±300µA, V_{DD} = 3.3V ±5%		67	91	117	
		I_{IC} = ±300µA, V_{DD} = 2.8V ±5%		86	108	141	
Common-Mode Input Impedance	Z_{IC}	I_{IC} = ±300µA		90	167	375	Ω
Input Capacitance	C_{IN}	SDI+ or SDI- to ground			2		pF
POWER SUPPLY							
Supply Current	I_{TOT}	V_{DD} = V_{DDO} = 2.5V (Note 4)	PCLKOUT = 10MHz, 100Mbps		8.4	12	mA
			PCLKOUT = 20MHz, 200Mbps		9.1	12	
Worst-Case Pattern Supply Current	I_{TOTW}	C_L = 5pF, V_{DD} = V_{DDO} = 2.5V, Figure 2 (Note 4)	PCLKOUT = 10MHz, 100Mbps		9.7	12	mA
			PCLKOUT = 20MHz, 200Mbps		11.6	13	
Power-Down Supply Current	I_{TOTZ}	(Note 4)			0.3	3.0	µA
Supply Difference	V_{SD}	MAX9225 V_{DD} to MAX9226 V_{DD}		-5		+5	%
GROUND POTENTIAL							
Ground Difference	V_{GD}	MAX9225 to MAX9226 ground difference		-0.2		+0.2	V

10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset

AC ELECTRICAL CHARACTERISTICS (MAX9225)

(V_{DD} = +2.375V to +3.465V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +2.5V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PCLKIN INPUT REQUIREMENTS (Figure 3)						
Input Rise Time	t_R				2	ns
Input Fall Time	t_F				2	ns
PCLKIN Period	t_P		50		100	ns
High-Level Pulse Width	t_{PWH}		0.3 x t_P		0.7 x t_P	ns
Low-Level Pulse Width	t_{PWL}		0.3 x t_P		0.7 x t_P	ns
Setup Time	t_S		3			ns
Hold Time	t_H		1			ns

AC ELECTRICAL CHARACTERISTICS (MAX9226)

(V_{DD} = V_{DDO} = +2.375V to +3.465V, C_L = 5pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = V_{DDO} = +2.5V, T_A = +25°C.) (Notes 3, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PCLKOUT Period	t_P	Figure 4	50		100	ns
High-Level Pulse Width	t_{PWH}	Figure 4	0.4 x t_P		0.6 x t_P	ns
Low-Level Pulse Width	t_{PWL}	Figure 4	0.4 x t_P		0.6 x t_P	ns
Data Valid Before PCLKOUT	t_{VB}	Figure 4	5			ns
Data Valid After PCLKOUT	t_{VA}	Figure 4	5			ns
SERIALIZER AND DESERIALIZER LINK						
Power-Up Time	t_{PU1}	From V_{DD} = V_{DDO} = 2.375V when supplies are ramping up			11,264 x t_P	ns
	t_{PU2}	From $\overline{PWRDN}$ low to high			4096 x t_P	
Power-Down Time	t_{PWRDN}	From $\overline{PWRDN}$ high to low		2.8	10	µs

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +85°C.

Note 3: Parameters are guaranteed by design and characterization and are not production tested. Limits are set at ±6 sigma.

Note 4: $I_{TOT} = I_{DD} + I_{DDO}$.

Note 5: C_L includes probe and test jig capacitance.

Test Circuits/Timing Diagrams

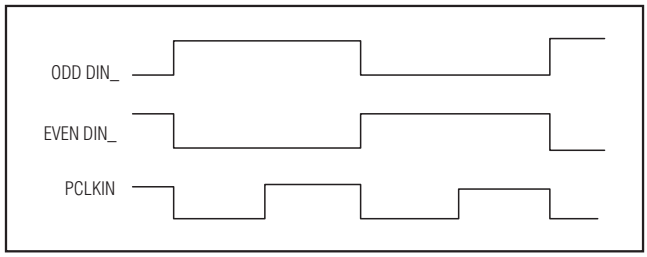


Figure 1. Serializer Worst-Case Switching Pattern

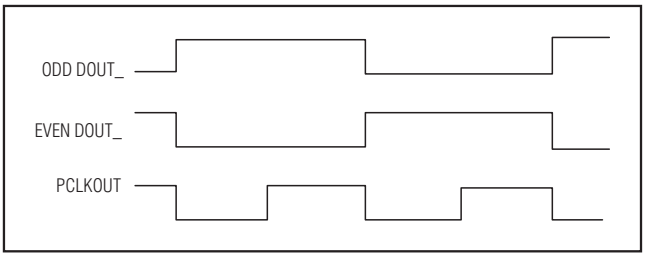


Figure 2. Deserializer Worst-Case Switching Pattern

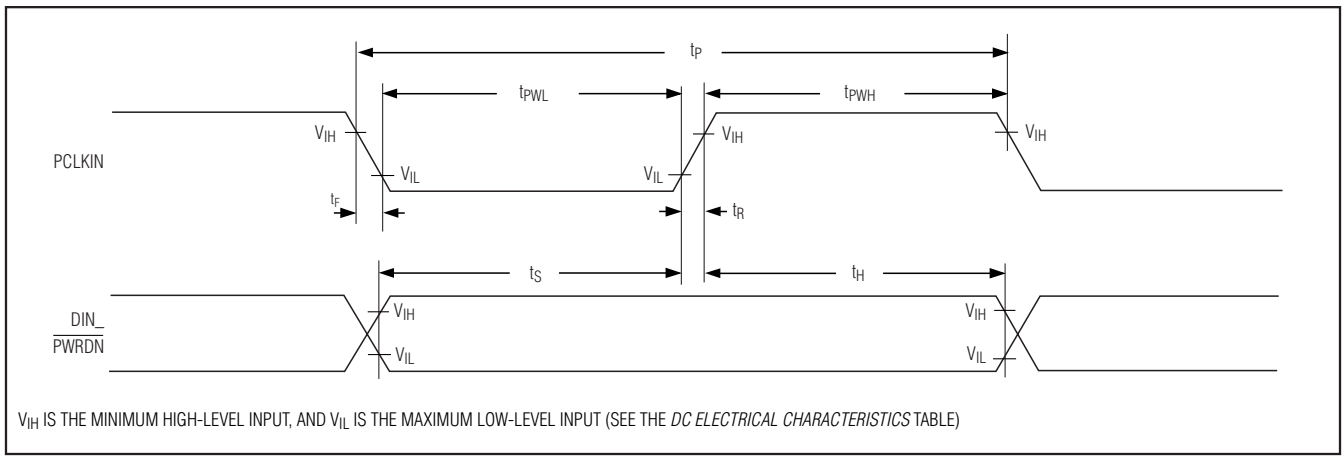


Figure 3. Serializer Input Timing

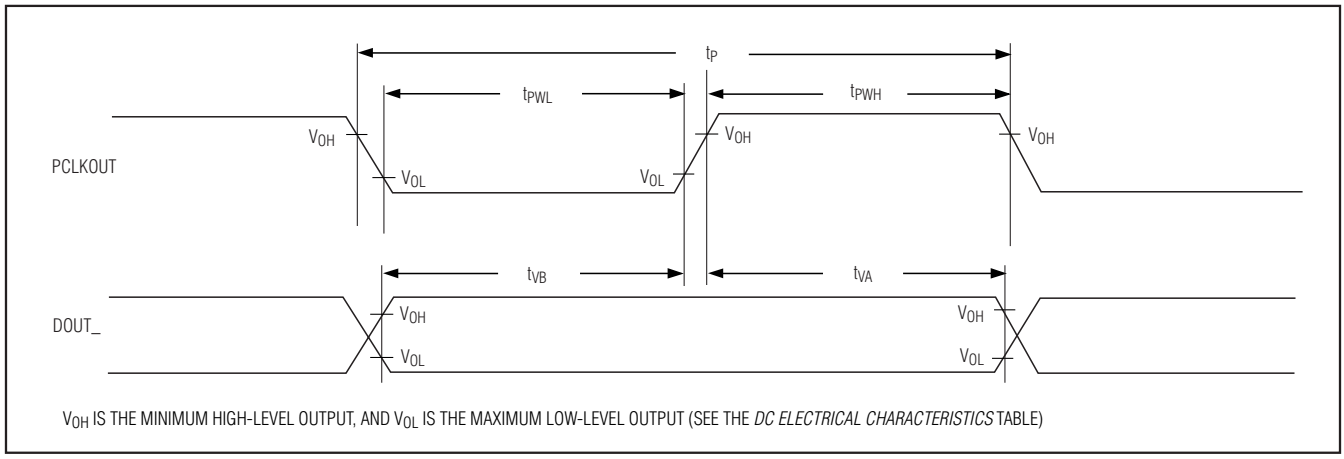


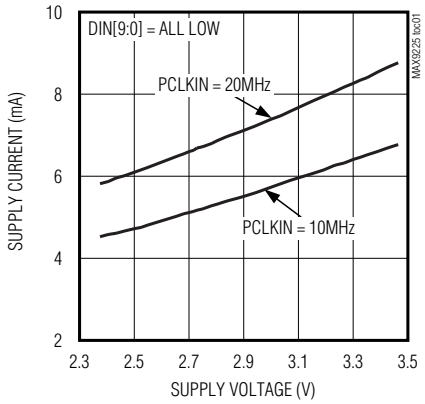
Figure 4. Deserializer Output Timing

10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset

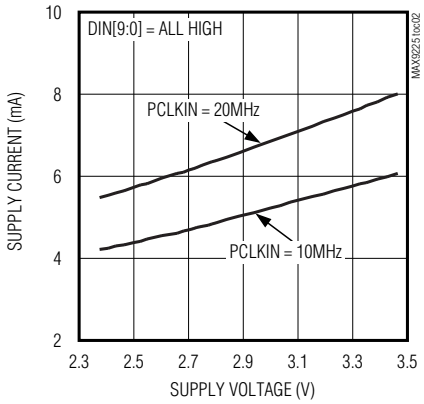
Typical Operating Characteristics

(V_{DD} = V_{DDO} = +2.8V, logic input levels = 0 to +2.8V, logic output load C_L = 5pF, T_A = +25°C, unless otherwise noted.)

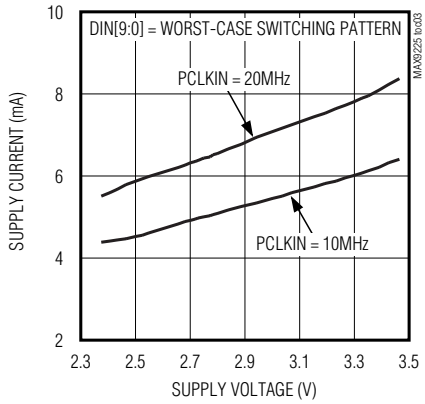
MAX9225
SUPPLY CURRENT vs. SUPPLY VOLTAGE



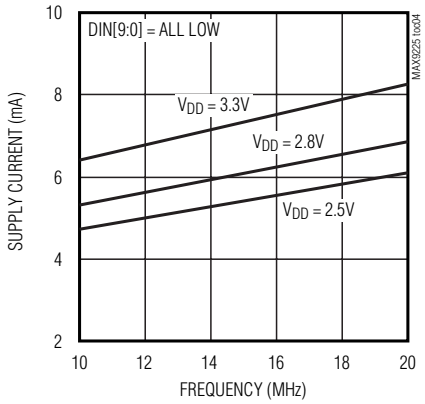
MAX9225
SUPPLY CURRENT vs. SUPPLY VOLTAGE



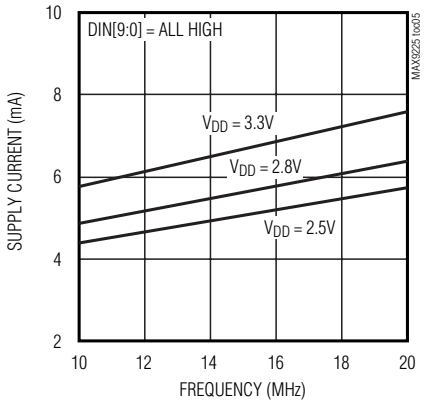
MAX9225
SUPPLY CURRENT vs. SUPPLY VOLTAGE



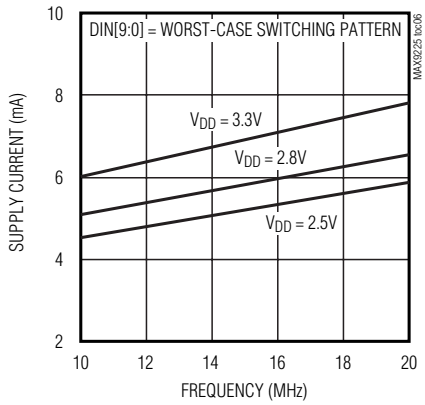
MAX9225
SUPPLY CURRENT vs. FREQUENCY



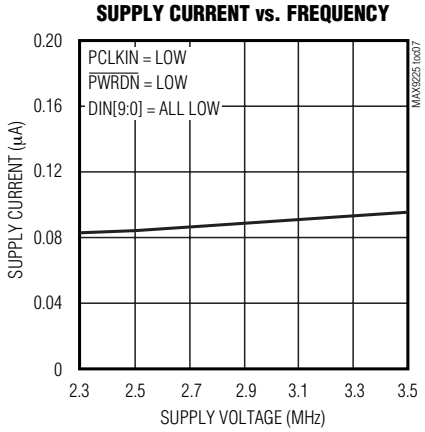
MAX9225
SUPPLY CURRENT vs. FREQUENCY



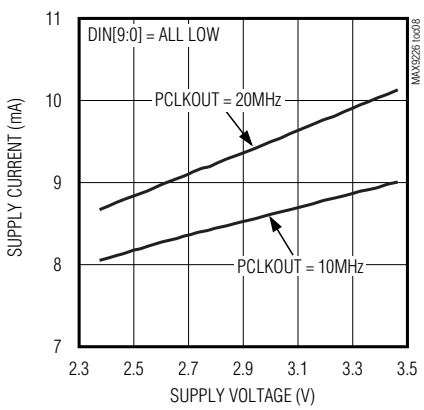
MAX9225
SUPPLY CURRENT vs. FREQUENCY



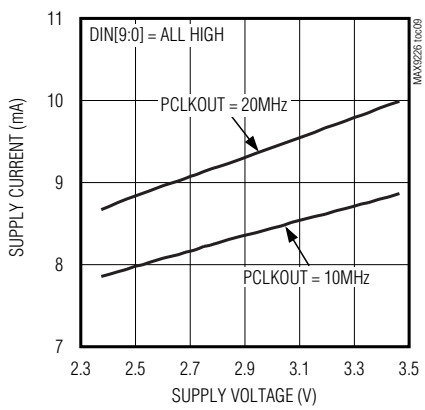
MAX9225 POWER-DOWN
SUPPLY CURRENT vs. FREQUENCY



MAX9226
SUPPLY CURRENT vs. SUPPLY VOLTAGE



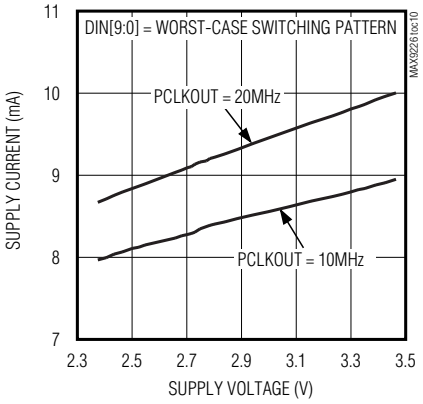
MAX9226
SUPPLY CURRENT vs. SUPPLY VOLTAGE



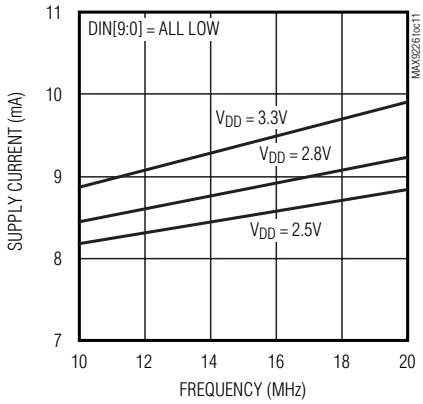
Typical Operating Characteristics (continued)

(V_{DD} = V_{DDO} = +2.8V, logic input levels = 0 to +2.8V, logic output load C_L = 5pF, T_A = +25°C, unless otherwise noted.)

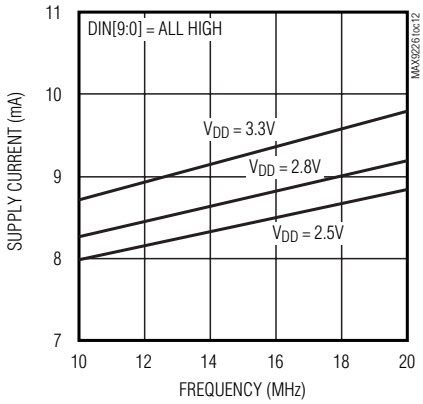
MAX9226
SUPPLY CURRENT vs. SUPPLY VOLTAGE



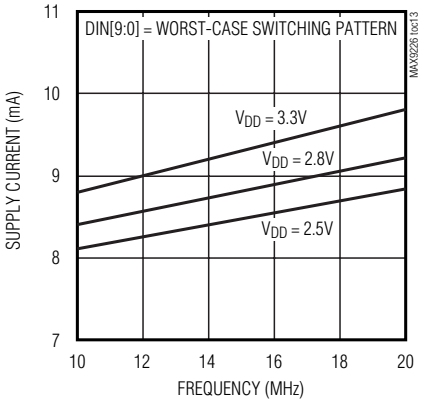
MAX9226
SUPPLY CURRENT vs. FREQUENCY



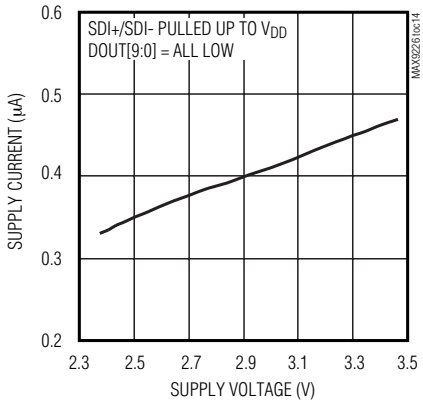
MAX9226
SUPPLY CURRENT vs. FREQUENCY



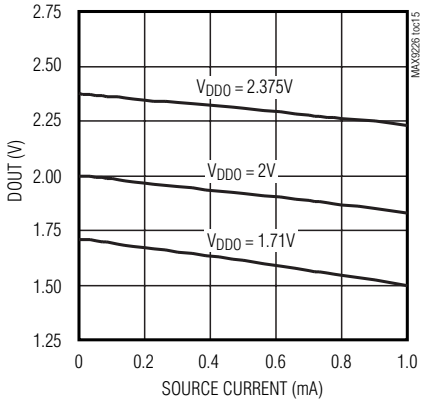
MAX9226
SUPPLY CURRENT vs. FREQUENCY



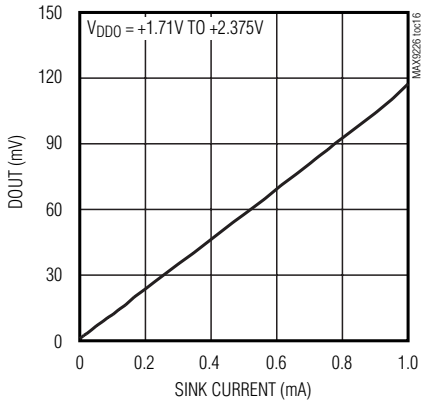
MAX9226 POWER-DOWN
SUPPLY CURRENT vs. FREQUENCY



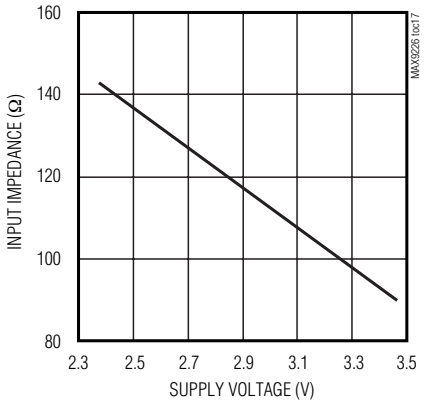
MAX9226 DOUT OUTPUT-HIGH VOLTAGE
vs. SOURCE CURRENT



MAX9226 DOUT OUTPUT-LOW VOLTAGE
vs. SINK CURRENT



MAX9226 DIFFERENTIAL INPUT
IMPEDANCE vs. SUPPLY VOLTAGE



10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset

Pin Description (MAX9225)

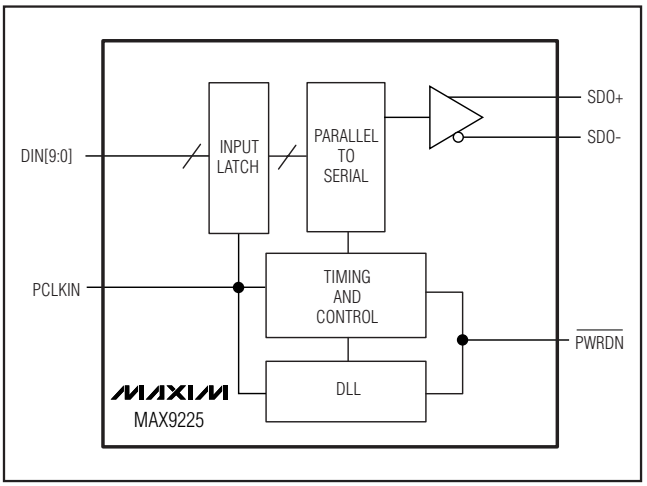
PIN	NAME	FUNCTION
1–7, 14, 15, 16	DIN6–DIN0, DIN9, DIN8, DIN7	Single-Ended Parallel Data Inputs. The 10 data bits are loaded into the input latch on the rising edge of PCLKIN. 1.71V to 3.465V tolerant. Internally pulled down to GND.
8	PCLKIN	Parallel Clock Input. The rising edge of PCLKIN (typically the pixel clock) latches the parallel data input. Internally pulled down to GND.
9	$\overline{PWRDN}$	Power-Down Input. Pull $\overline{PWRDN}$ low to place the MAX9225/MAX9226 in power-down mode. Drive $\overline{PWRDN}$ high for normal operation. Internally pulled down to GND.
10	SDO-	Inverting LCDS Serial-Data Output
11	SDO+	Noninverting LCDS Serial-Data Output
12	GND	Ground
13	V_{DD}	Core Supply Voltage. Bypass to GND with 0.1µF and 0.01µF capacitors in parallel as close to the device as possible with the smallest value capacitor closest to the supply pin.
—	EP	Exposed Paddle. Connect EP to ground.

Pin Description (MAX9226)

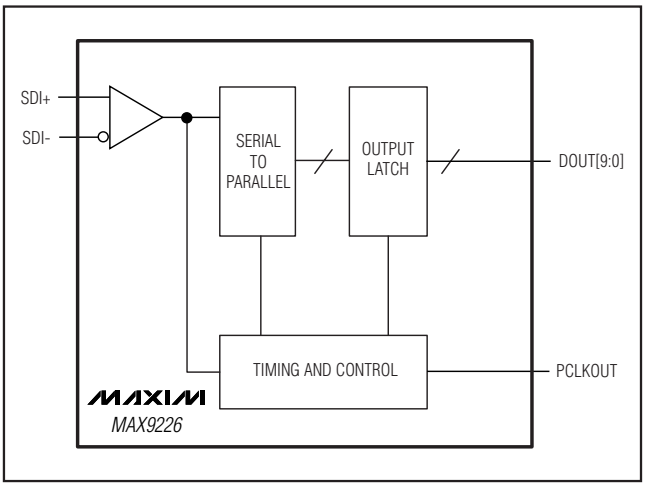
PIN	NAME	FUNCTION
1	GND	Ground
2	SDI+	Noninverting LCDS Serial-Data Input
3	SDI-	Inverting LCDS Serial-Data Input
4	V_{DD}	Core Supply Voltage. Bypass to GND with 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
5	PCLKOUT	Parallel Clock Output. Parallel output data are valid on the rising edge of PCLKOUT (typically the pixel clock).
6–15	DOUT0–DOUT9	Single-Ended Parallel Data Output. DOUT[9:0] are valid on the rising edge of PCLKOUT.
16	V_{DDO}	Output Supply Voltage. Bypass to GND with 0.1µF and 0.01µF capacitors in parallel as close to the device as possible with the smallest value capacitor closest to the supply pin.
—	EP	Exposed Paddle. Connect EP to ground.

10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset

Functional Diagram (MAX9225)



Functional Diagram (MAX9226)



Detailed Description

The MAX9225 serializer operates at a 10MHz-to-20MHz parallel clock frequency, serializing 10 bits of parallel input data DIN[9:0] in each cycle of the parallel clock. DIN[9:0] are latched on the rising edge of PCLKIN. The data and internally generated serial clock are combined and transmitted through SDO+/SDO- using multilevel LCDS. The MAX9226 deserializer receives the LCDS signal on SDI+/SDI-. The deserialized data and recovered parallel clock are available at DOUT[9:0] and PCLKOUT. Output data is valid on the rising edge of PCLKOUT.

Bit 0 (DIN[0]) is transmitted first. Boundary bits OH1 and OH2 are used by the MAX9226 deserializer to identify the word boundary. OH1 is the inverse polarity of data bit 9 (DIN[9]), and OH2 is the inverse polarity of OH1. Therefore, at least two level transitions are guaranteed in one word. The clock is recovered from the serial input.

Serial word format:

0	1	2	3	4	5	6	7	8	9	OH1	OH2

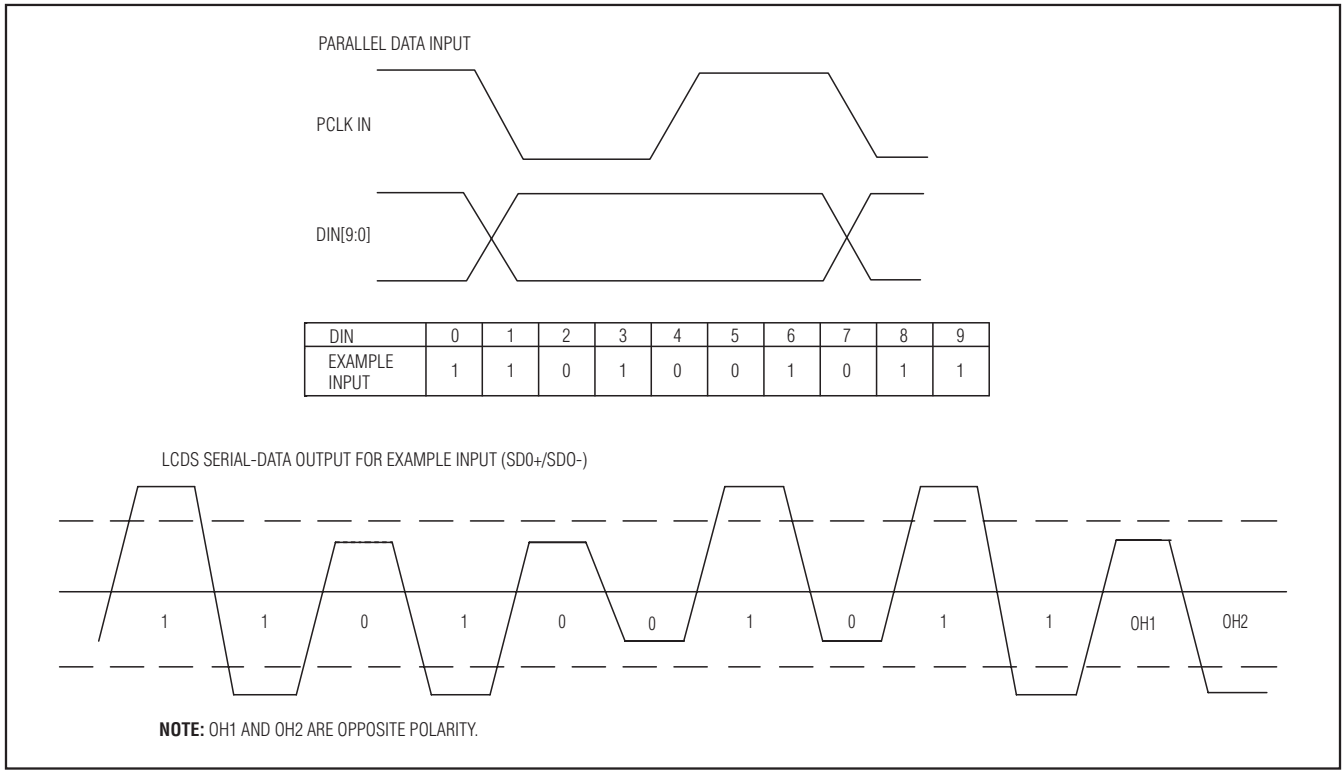
LCDS

The MAX9225/MAX9226 use a proprietary multilevel LCDS interface. Figure 5 provides a representation of the data and clock in the multilevel LCDS interface. This interface offers advantages over other chipsets, such as requiring only one differential pair as the transmission medium, the inherently aligned data and clock, and much smaller current levels than the 4mA typically found in traditional LVDS interfaces.

MAX9225/MAX9226 Handshaking

The handshaking function of the MAX9225/MAX9226 provides bidirectional communication between the two devices in case a word boundary error is detected. Prior to data transmission, the MAX9225 serializer adds boundary bits (OH) to the end of the latched word. These boundary bits are the inverse of the last bit of the latched word. During data transmission, the MAX9226 deserializer continuously monitors the state of the boundary bits of each word. If a word boundary error is detected, the serial link is pulled up to V_{DD} and the MAX9226 powers down. The MAX9225 detects the pullup of the serial link and powers down for 1.0µs. After 1.0µs, the MAX9225 powers up, causing the power-up of the MAX9226. Then the word boundary is reestablished, and data transfer resumes. The handshaking function is disabled when $\overline{PWRDN}$ is pulled low.

10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset



DIN	0	1	2	3	4	5	6	7	8	9
EXAMPLE INPUT	1	1	0	1	0	0	1	0	1	1

Figure 5. Multilevel LCDS Output Representation

Applications Information

PCLKIN Latch Edge

The parallel data input of the MAX9225 serializer is latched on the rising edge of PCLKIN. Figure 3 shows the serializer input timing.

PCLKOUT Strobe

The serial-data output of the MAX9226 deserializer is valid on the rising edge of PCLKOUT. Figure 4 shows the deserializer output timing.

Power-Down and Power-Up

Driving $\overline{PWRDN}$ low puts the MAX9225 in power-down mode and sends a pulse to power down the MAX9226. In power-down mode, the DLL is stopped, SDO+/SDO- are high impedance to ground and differential, and the LCDS link is weakly biased around (V_{DD} - 0.8V). With $\overline{PWRDN}$ and all inputs low, the combined MAX9225/MAX9226 supply current is reduced to 3.5µA or less.

Driving $\overline{PWRDN}$ high starts DLL lock to PCLKIN and initiates a MAX9226 power-up sequence. The MAX9225 LCDS output is not driven until the DLL locks. 11,264 clock cycles are required for the power-up and link synchronization before valid DIN can be latched. See Figure 6 for an overall power-up and power-down timing diagram. For normal operation, PCLKIN must be running and settled before driving $\overline{PWRDN}$ high.

If V_{DD} = 0, the LCDS outputs are high impedance to ground and differential.

Ground-Shift Tolerance

The MAX9225/MAX9226 are designed to function normally in the event of a slight shift in ground potential. However, the MAX9226 deserializer ground must be within ±0.2V relative to the MAX9225 serializer ground to maintain proper operation.

MAX9226 Output Buffer Supply (V_{DDO})

The MAX9226 parallel outputs are powered from V_{DDO}, which accepts a +1.71V to +3.465V supply, allowing direct interface to inputs with 1.8V to 3.3V logic levels.

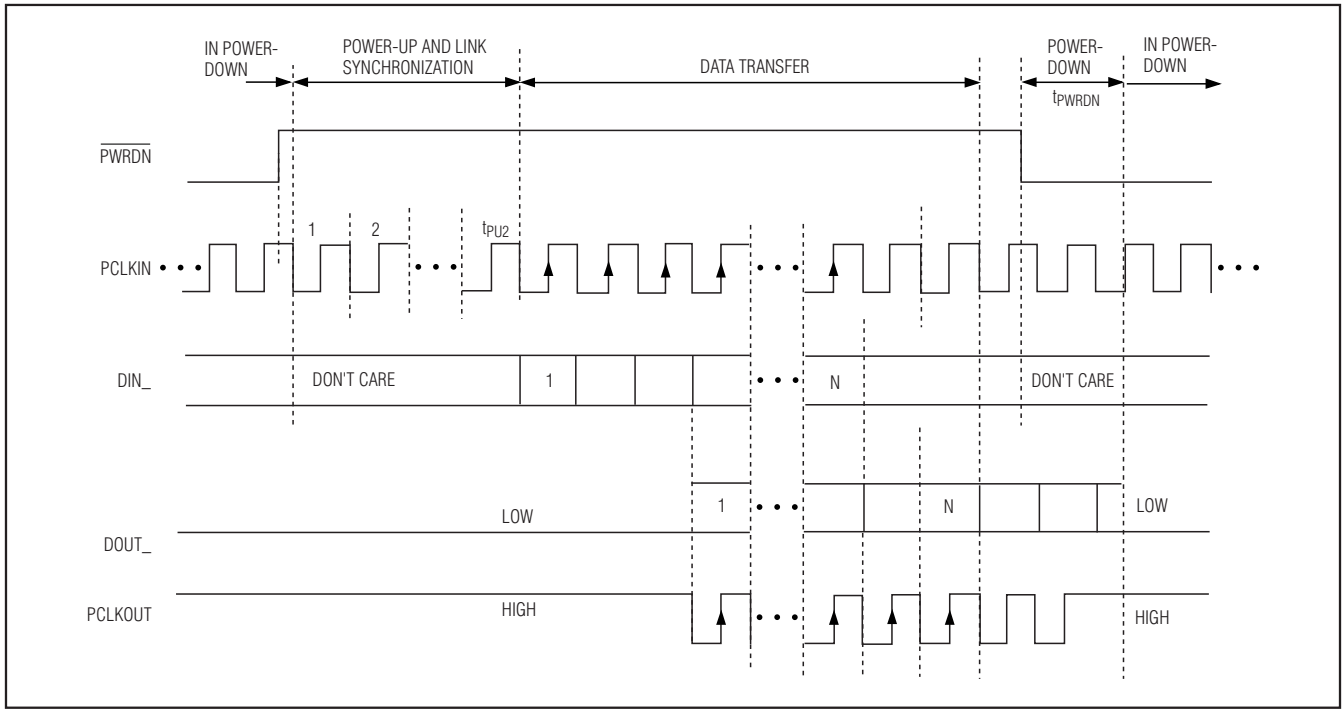


Figure 6. MAX9225/MAX9226 Power-Up/Power-Down Sequence

Flex Cable, PCB Interconnect, and Connectors

Interconnect for LCDS typically has a differential impedance of 100Ω. Use interconnect and connectors that have matched differential impedance to minimize impedance discontinuities.

Board Layout and Supply Bypassing

Separate the LVTTL/LVCMOS and LCDS signals to prevent crosstalk. A PCB or flex with separate layers for power, ground, and signals is recommended.

Bypass each V_{DD} and V_{DDO} pin with high-frequency, surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

ESD Protection

The MAX9225/MAX9226 are rated for ±15kV ESD protection using the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 7).

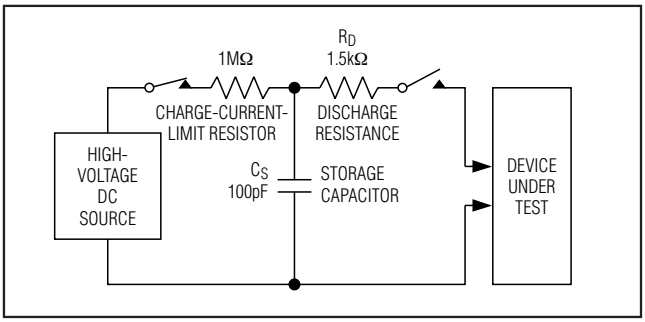


Figure 7. Human Body Model ESD Test Circuit

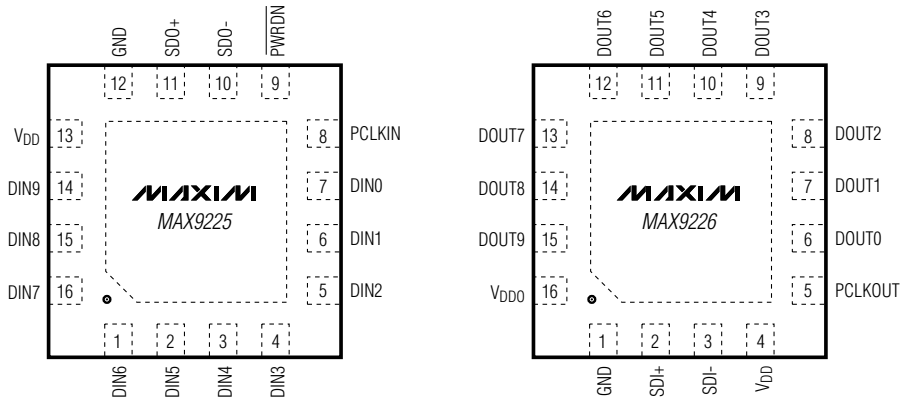
Chip Information

PROCESS: CMOS

10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset

Pin Configurations

TOP VIEW

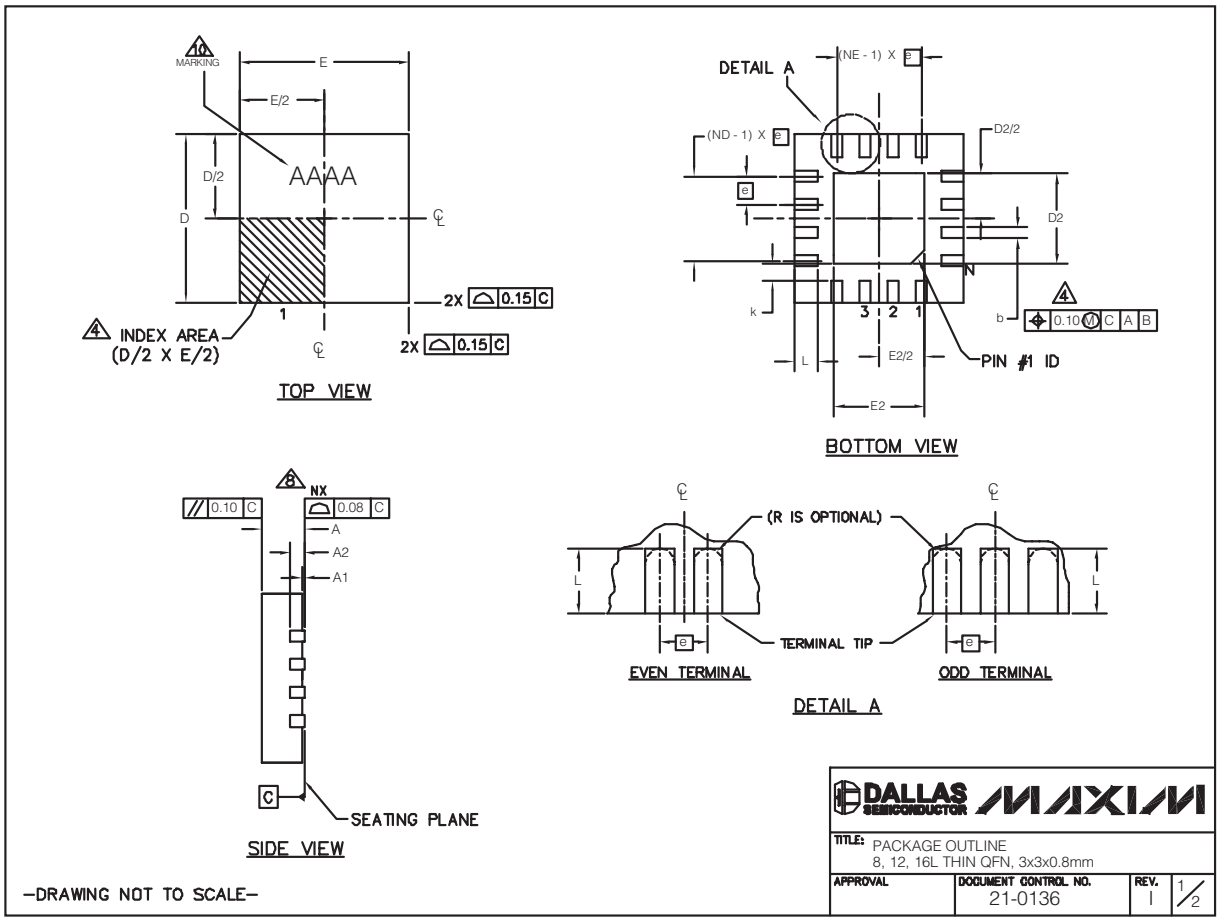


10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS .
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE 8, 12, 16L THIN QFN, 3x3x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	I	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/06	Initial release	—
1	12/07	Changed max output short-circuit current from -20 to -25 in EC table; various style changes.	2, 3, 11