

TC74AC32P, TC74AC32F, TC74AC32FN, TC74AC32FT

Quad 2-Input OR Gate

The TC74AC32 is an advanced high speed CMOS 2-INPUT OR GATE fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output.

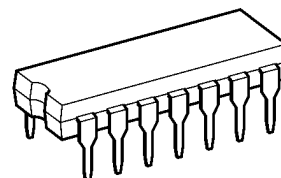
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $t_{pd} = 4.1 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 4 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$
Capability of driving 50Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC \text{ (opr)}} = 2 \text{ to } 5.5 \text{ V}$
- Pin and function compatible with 74F32

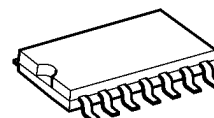
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74AC32P



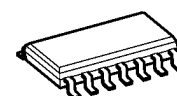
DIP14-P-300-2.54

TC74AC32F



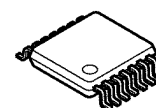
SOP14-P-300-1.27A

TC74AC32FN



SOL14-P-150-1.27

TC74AC32FT

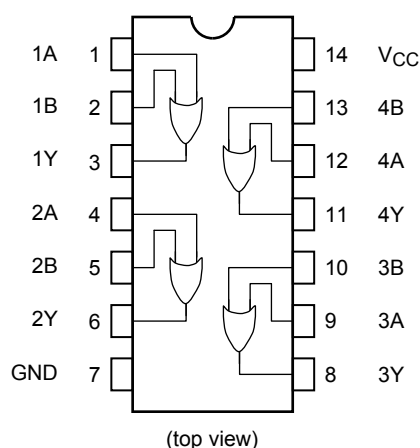


TSSOP14-P-0044-0.65A

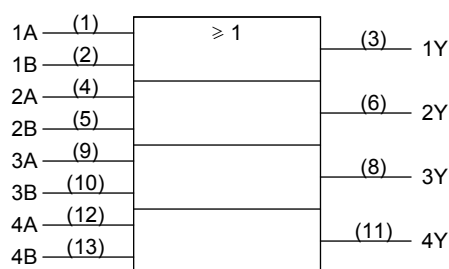
Weight

DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)

Pin Assignment



IEC Logic Symbol



Truth Table

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±50	mA
DC output current	I_{OUT}	±50	mA
DC V_{CC} /ground current	I_{CC}	±100	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit
				Min	Typ.	Max	Min	Max	
High-level input voltage	V_{IH}	—	2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low-level input voltage	V_{IL}	—	2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High-level output voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -75 \text{ mA}$ (Note)	2.0 3.0 4.5 3.0 4.5 5.5	1.9 2.9 4.4 2.58 3.94 —	2.0 3.0 4.5 — — —	— — — — — —	1.9 2.9 4.4 2.48 3.80 3.85	— — — — — —	V
Low-level output voltage	V_{OL}	$V_{IN} = V_{IL}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 75 \text{ mA}$ (Note)	2.0 3.0 4.5 3.0 4.5 5.5	— — — — — —	0.0 0.0 0.0 — — —	0.1 0.1 0.1 0.36 0.36 —	— — — — — —	0.1 0.1 0.1 0.44 0.44 1.65	V
Input leakage current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	4.0	—	40.0	μA

Note: This spec indicates the capability of driving 50 Ω transmission lines.
One output should be tested at a time for a 10 ms maximum duration.

AC Characteristics ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	Min	Typ.	Max	Min	Max
Propagation delay time	t _{pLH}	—	3.3 ± 0.3	—	6.1	10.3	1.0	11.9
	t _{pHL}		5.0 ± 0.5	—	5.2	7.4	1.0	8.5
Input capacitance	C _{IN}	—	—	—	5	10	—	10
Power dissipation capacitance	C _{PD}	(Note)	—	—	64	—	—	—

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

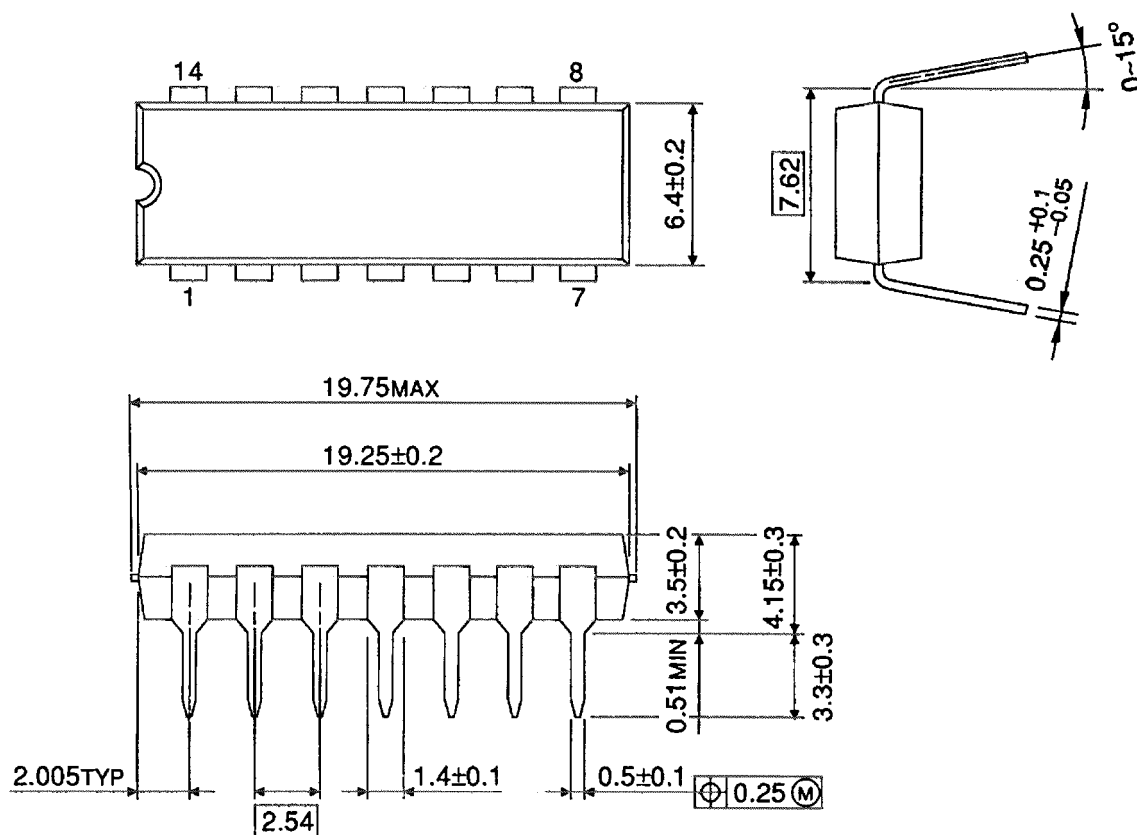
Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

Package Dimensions

DIP14-P-300-2.54

Unit : mm

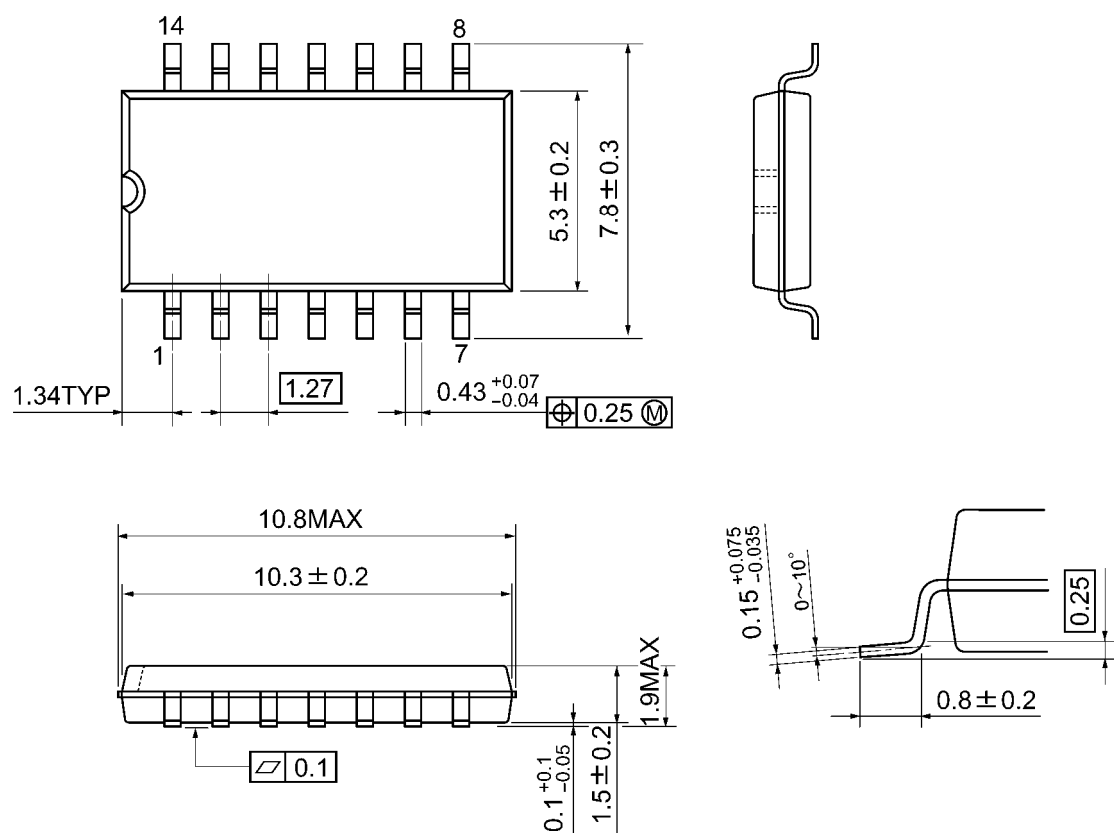


Weight: 0.96 g (typ.)

Package Dimensions

SOP14-P-300-1.27A

Unit: mm

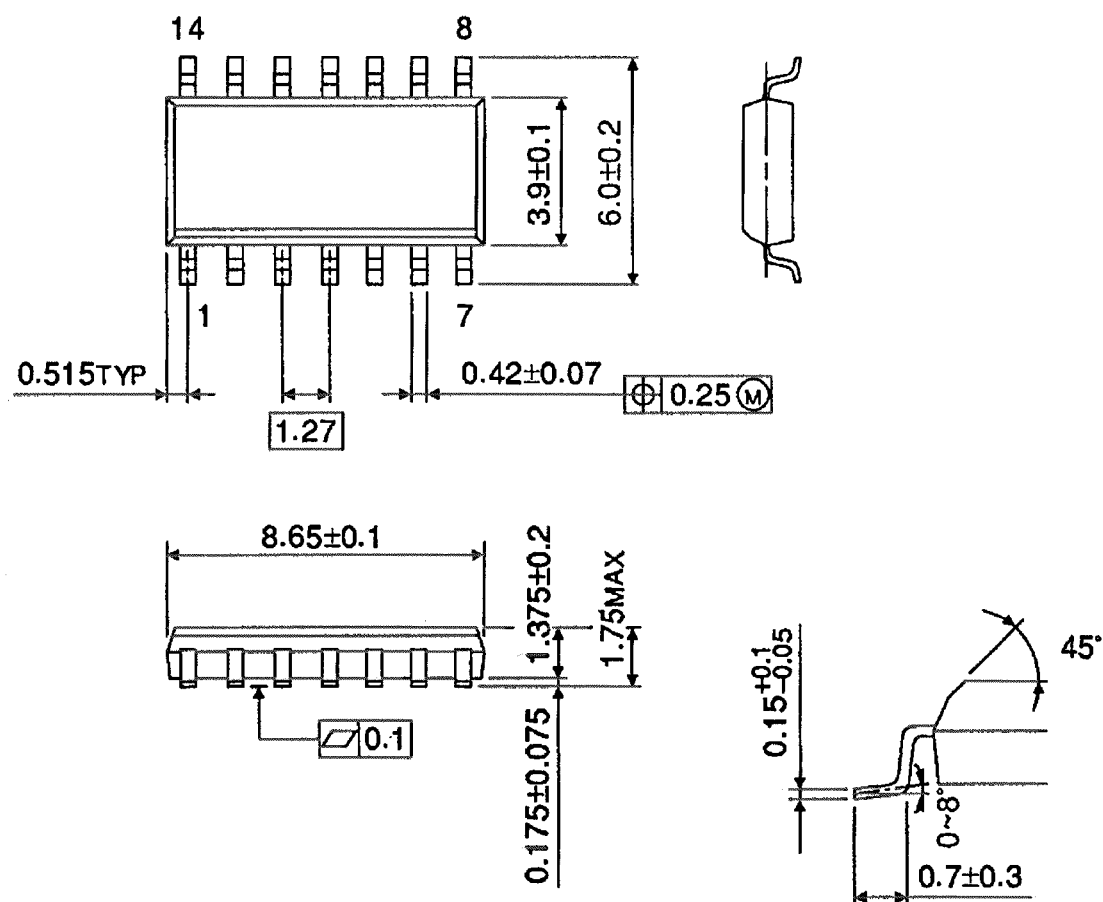


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



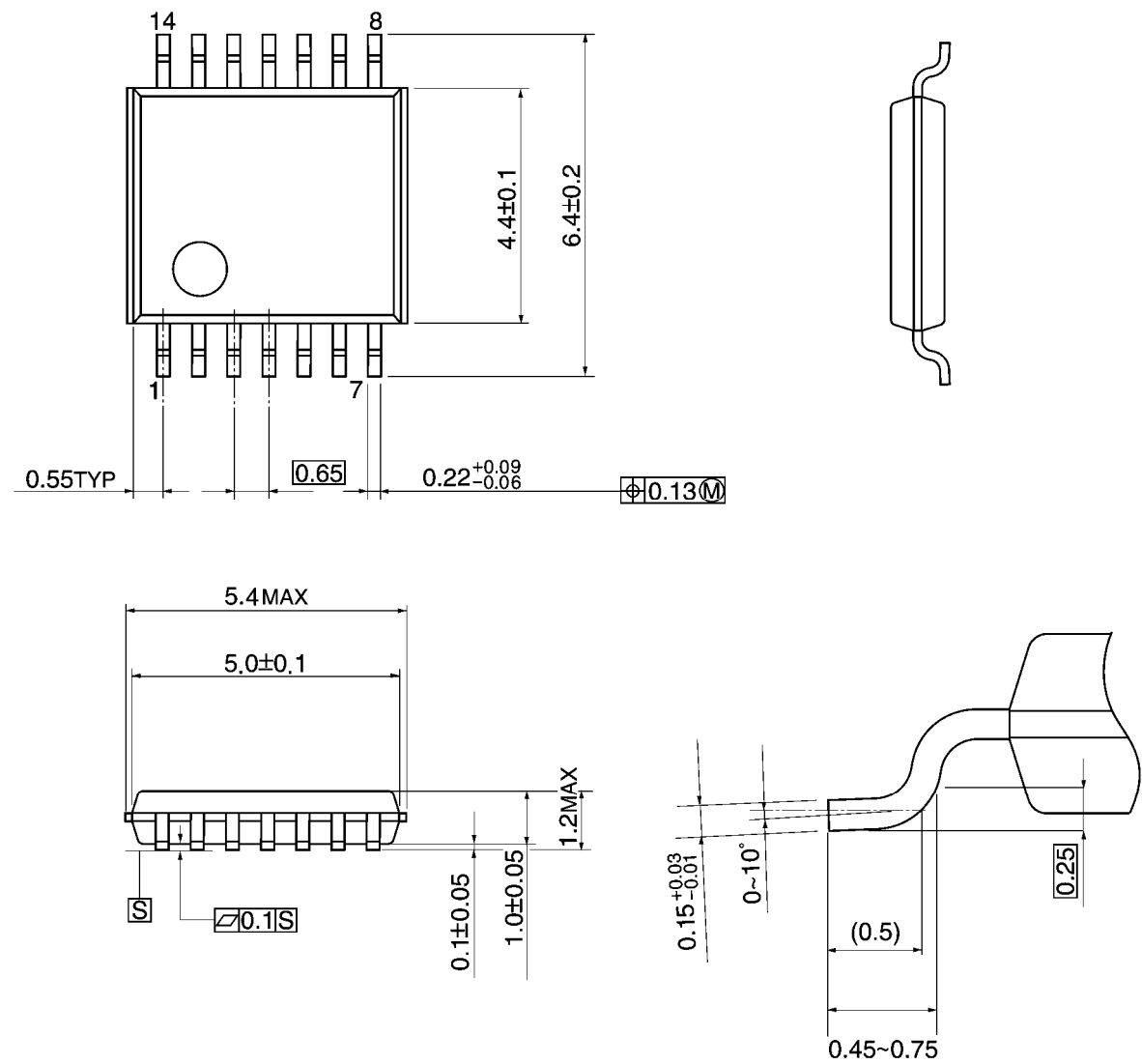
Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

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