

- Organization . . . 2097152 × 8
- Single 5 V Power Supply (±10% Tolerance)
- Performance Ranges:

| | ACCESS TIME | ACCESS TIME | ACCESS TIME | EDO CYCLE |
|------------|------------------|------------------|-----------------|------------------|
| | t _{RAC} | t _{CAC} | t _{AA} | t _{HPC} |
| | MAX | MAX | MAX | MIN |
| '41x809-60 | 60 ns | 15 ns | 30 ns | 25 ns |
| '41x809-70 | 70 ns | 18 ns | 35 ns | 30 ns |
| '41x809-80 | 80 ns | 20 ns | 40 ns | 35 ns |

- Extended Data Out (EDO) Operation
- CAS-Before-RAS (CBR) Refresh
- High-Impedance State Unlatched Output
- High-Reliability Plastic 28-Lead (DZ Suffix)
400-Mil-Wide Surface-Mount Small-Outline
J-Lead (SOJ) Package
- Operating Free-Air Temperature Range
0°C to 70°C
- Fabricated Using Enhanced Performance
Implanted CMOS (EPIC™) Technology by
Texas Instruments (TI™)

AVAILABLE OPTIONS

| DEVICE | POWER SUPPLY | REFRESH CYCLES |
|-----------|-----------------|-------------------|
| TMS416809 | 5 V | 4096 in 64 ms |
| TMS417809 | 5 V | 2048 in 32 ms |

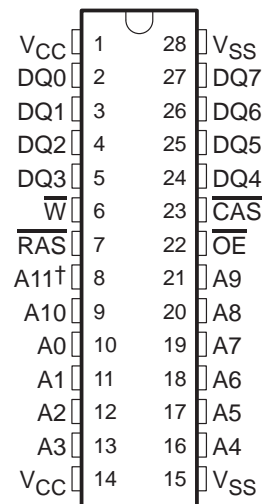
description

The TMS41x809 series is a set of high-speed, 16777216-bit dynamic random-access memories (DRAMs) organized as 2097152 words of eight bits each. It employs TI's state-of-the-art EPIC technology for high performance, reliability, and low power.

These devices feature maximum $\overline{\text{RAS}}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS41x809 is offered in a 28-lead plastic surface-mount SOJ package (DZ suffix). This package is characterized for operation from 0°C to 70°C.

DZ PACKAGE
(TOP VIEW)



† A11 is NC (no internal connection) for TMS417809.

PIN NOMENCLATURE

| | |
|------------------------|------------------------|
| A0–A11 | Address Inputs |
| DQ0–DQ7 | Data In/Data Out |
| CAS | Column-Address Strobe |
| NC | No Internal Connection |
| $\overline{\text{OE}}$ | Output Enable |
| RAS | Row-Address Strobe |
| VCC | 5 V Supply† |
| VSS | Ground |
| W | Write Enable |

† See Available Options Table.



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TMS416809, TMS417809

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operation

extended data out

Extended data out (EDO) allows data output rates up to 40 MHz for 60-ns devices. When keeping the same row address while selecting random column addresses, the time for row-address setup and hold, and for address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP} , the maximum \overline{RAS} low time.

Extended data out does not place the data in/data out pins (DQs) into the high-impedance state with the rising edge of \overline{CAS} . The output remains valid for the system to latch the data. After \overline{CAS} goes high, the DRAM decodes the next address. \overline{OE} and \overline{W} can control the output impedance. Descriptions of \overline{OE} and \overline{W} further explain EDO operation benefit.

address: A0–A11 (TMS416809) and A0–A10 (TMS417809)

Twenty-one address bits are required to decode 1 of 2097152 storage-cell locations. For the TMS416809, 12 row-address bits are set up on A0 through A11 and latched onto the chip by the row-address strobe (\overline{RAS}). Nine column-address bits are set up on A0 through A8. For the TMS417809, 11 row-address bits are set up on inputs A0 through A10 and latched onto the chip by \overline{RAS} . Ten column-address bits are set up on A0 through A9. All addresses must be stable on or before the falling edge of \overline{RAS} and \overline{CAS} . \overline{RAS} is similar to a chip enable because it activates the sense amplifiers as well as the row decoder. \overline{CAS} is used as a chip select, activating the output buffers and latching the address bits into the column-address buffers.

output enable (\overline{OE})

\overline{OE} controls the impedance of the output buffers. While \overline{CAS} and \overline{RAS} are low and \overline{W} is high, \overline{OE} can be brought low or high and the DQs transition between valid data and high impedance (see Figure 7). There are two methods for placing the DQs into the high-impedance state and maintaining that state during \overline{CAS} high time. The first method is to transition \overline{OE} high before \overline{CAS} transitions high and keep \overline{OE} high for t_{CHO} (hold time, \overline{OE} from \overline{CAS}) past the \overline{CAS} transition. This disables the DQs and they remain disabled, regardless of \overline{OE} , until \overline{CAS} falls again. The second method is to have \overline{OE} low as \overline{CAS} transitions high. Then \overline{OE} can pulse high for a minimum of t_{OEP} (precharge time, \overline{OE}) anytime during \overline{CAS} high time, disabling the DQs regardless of further transitions on \overline{OE} until \overline{CAS} falls again (see Figure 7).

write enable (\overline{W})

The read or write mode is selected through \overline{W} . A logic high on \overline{W} selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When \overline{W} goes low prior to \overline{CAS} (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with \overline{OE} grounded. If \overline{W} goes low in an extended-data-out read cycle, the DQs are disabled so long as \overline{CAS} is high (see Figure 8).

data in/data out (DQ0–DQ7)

Data is written during a write or a read-modify-write cycle. Depending on the mode of operation, the later falling edge of \overline{CAS} or \overline{W} strobes data into the on-chip data latch with setup and hold times referenced to the later edge. The DQs drive valid data after all access times are met and remain valid except in cases described in the \overline{W} and \overline{OE} descriptions.

\overline{RAS} -only refresh

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A refresh operation must be performed at least once every 64 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A \overline{RAS} -only operation can be used by holding \overline{CAS} at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a \overline{RAS} -only refresh.



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A refresh operation must be performed at least once every 32 ms to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$ -only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$ -only refresh.

hidden refresh

A hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$ -only refresh cycle. The external address is ignored, and the refresh address is generated internally.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (CBR) refresh

CBR refresh is performed by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored, and the refresh address is generated internally.

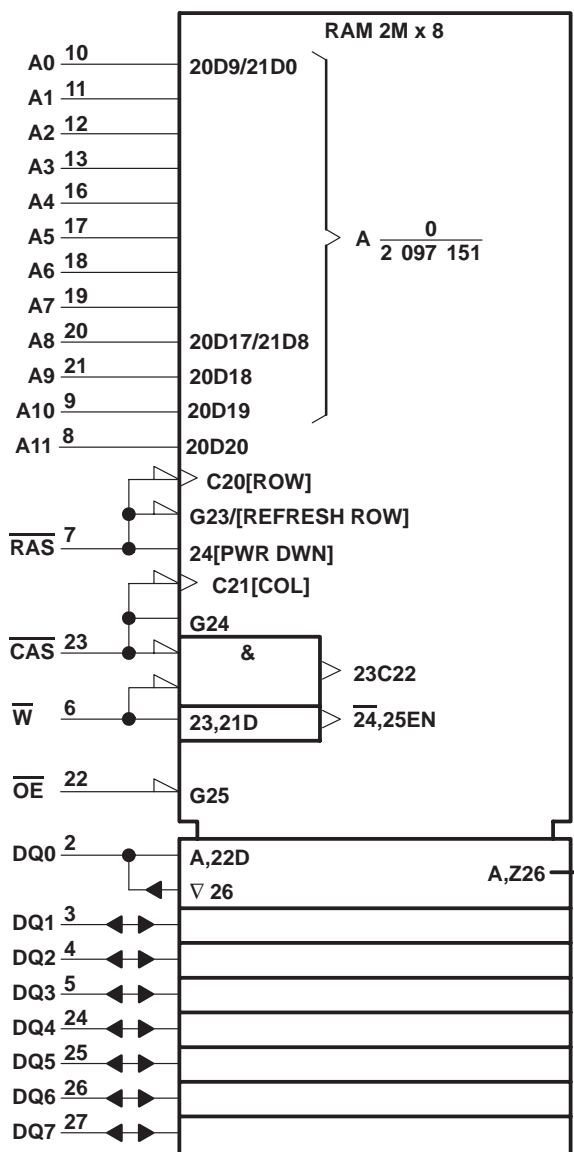
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. These eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$ -only or CBR) cycle.

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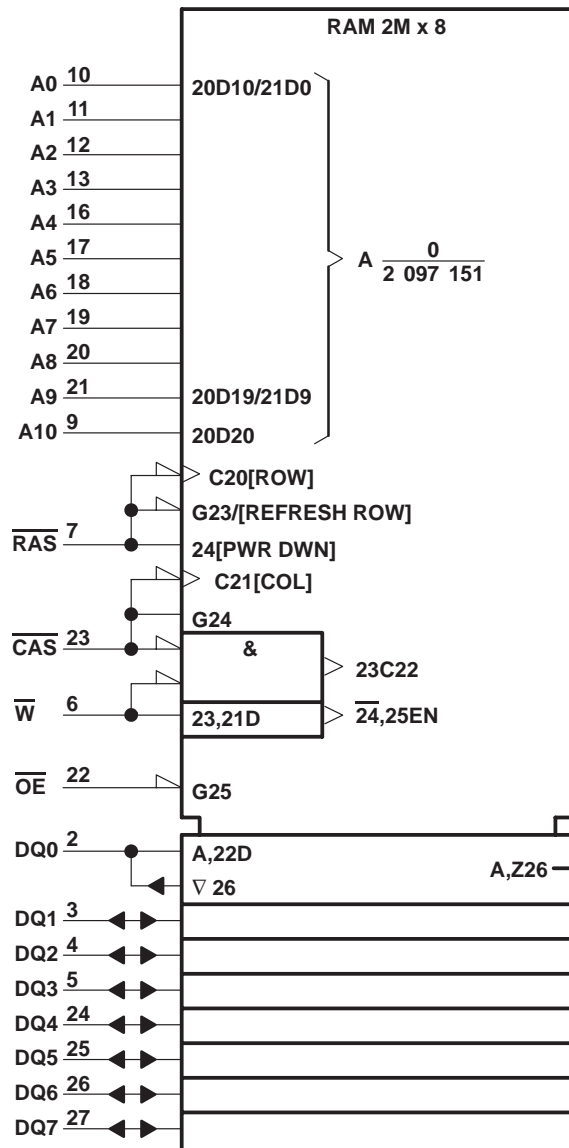
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logic symbol (TMS416809)†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

logic symbol (TMS417809)†



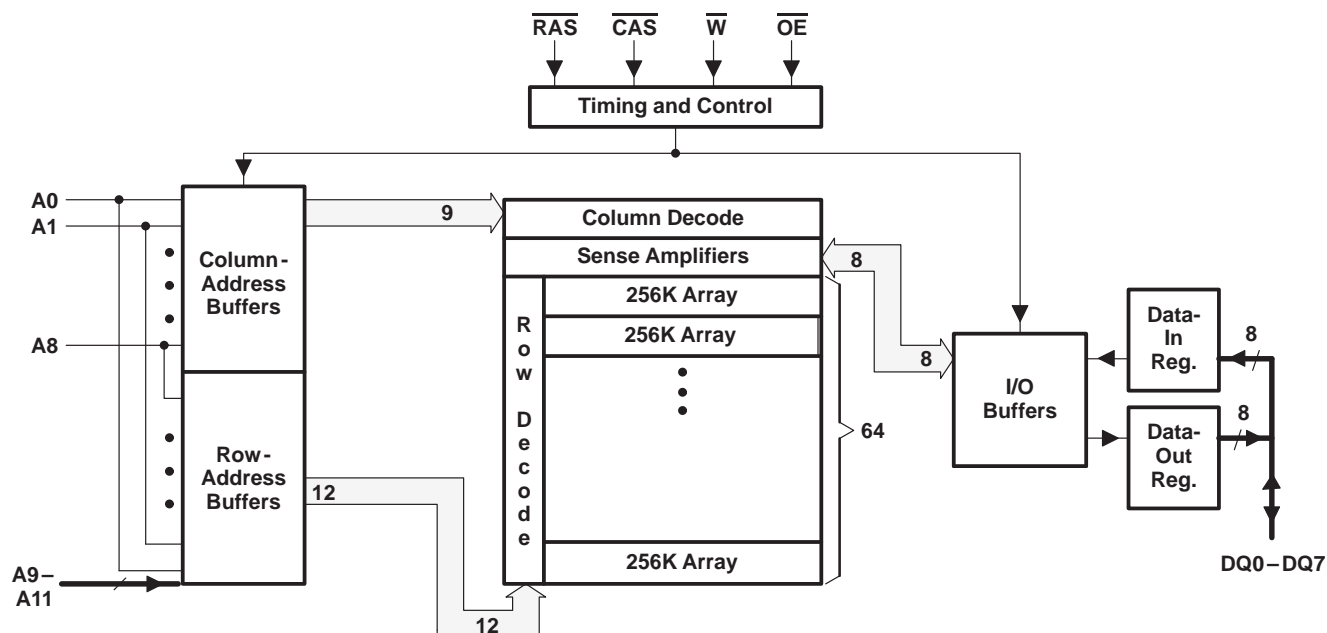
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

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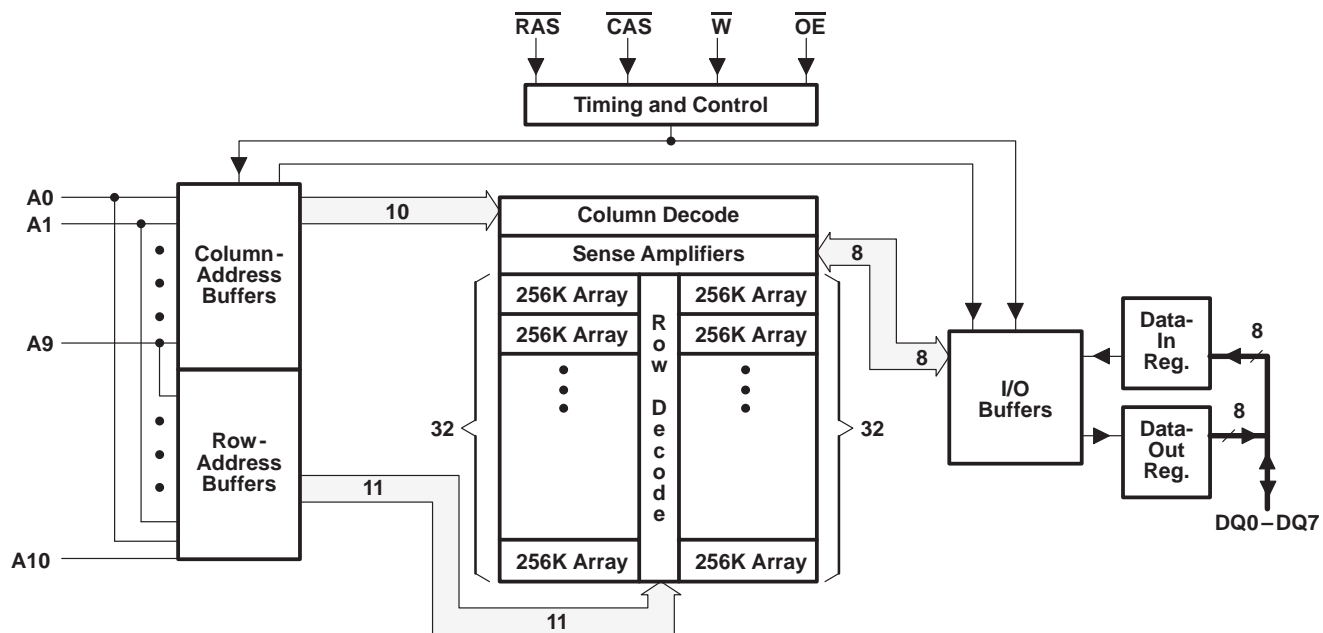
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functional block diagram (TMS416809)



functional block diagram (TMS417809)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | – 1 V to 7 V |
| Voltage range on any pin (see Note 1) | – 1 V to 7 V |
| Short-circuit output current | 50 mA |
| Power dissipation | 1 W |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | – 55°C to 125°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|-----|-----|-----|------|
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{SS} Supply voltage | | 0 | | V |
| V_{IH} High-level input voltage | 2.4 | | 6.5 | V |
| V_{IL} Low-level input voltage (see Note 2) | – 1 | | 0.8 | V |
| T_A Operating free-air temperature | 0 | | 70 | °C |

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS416809

| PARAMETER | TEST CONDITIONS† | '416809-60 | | '416809-70 | | '416809-80 | | UNIT |
|---|--|------------|------|------------|------|------------|------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} High-level output voltage | I _{OH} = – 5 mA | 2.4 | | 2.4 | | 2.4 | | V |
| V _{OL} Low-level output voltage | I _{OL} = 4.2 mA | | 0.4 | | 0.4 | | 0.4 | V |
| I _I Input current (leakage) | V _{CC} = 5.5 V, V _I = 0 V to 6.5 V, All others = 0 V to V _{CC} | | ± 10 | | ± 10 | | ± 10 | μA |
| I _O Output current (leakage) | V _{CC} = 5.5 V, V _O = 0 V to V _{CC} , CAS high | | ± 10 | | ± 10 | | ± 10 | μA |
| I _{CC1} ‡§ Read- or write-cycle current | V _{CC} = 5.5 V, Minimum cycle | | 80 | | 70 | | 60 | mA |
| I _{CC2} Standby current | V _{IH} = 2.4 V (TTL), After 1 memory cycle, RAS and CAS high | | 2 | | 2 | | 2 | mA |
| | V _{IH} = V _{CC} – 0.2 V (CMOS), After 1 memory cycle, RAS and CAS high | | 1 | | 1 | | 1 | mA |
| I _{CC3} ‡§ Average refresh current (RAS-only refresh or CBR) | V _{CC} = 5.5 V, Minimum cycle, RAS cycling, CAS high (RAS only), RAS low after CAS low (CBR) | | 80 | | 70 | | 60 | mA |
| I _{CC4} ‡¶ Average EDO current | V _{CC} = 5.5 V, t _{HPC} = MIN, RAS low, CAS cycling | | 90 | | 80 | | 70 | mA |

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RAS}} = V_{IL}$

¶ Measured with a maximum of one address change while $\text{CAS} = V_{IH}$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TMS417809

| PARAMETER | TEST CONDITIONS† | '417809-60 | | '417809-70 | | '417809-80 | | UNIT |
|---------------------|---|---|-----|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | High-level output voltage | I _{OH} = – 5 mA | | 2.4 | | 2.4 | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 4.2 mA | | 0.4 | | 0.4 | | V |
| I _I | Input current (leakage) | V _{CC} = 5.5 V, V _I = 0 V to 6.5 V, All others = 0 V to V _{CC} | | ± 10 | | ± 10 | | µA |
| I _O | Output current (leakage) | V _{CC} = 5.5 V, V _O = 0 V to V _{CC} , CAS high | | ± 10 | | ± 10 | | µA |
| I _{CC1} ‡§ | Read- or write-cycle current | V _{CC} = 5.5 V, Minimum cycle | | 110 | | 100 | | mA |
| I _{CC2} | Standby current | V _{IH} = 2.4 V (TTL), After 1 memory cycle, RAS and CAS high | | 2 | | 2 | | mA |
| | | V _{IH} = V _{CC} – 0.2 V (CMOS), After 1 memory cycle, RAS and CAS high | | 1 | | 1 | | mA |
| I _{CC3} ‡§ | Average refresh current (RAS-only refresh or CBR) | V _{CC} = 5.5 V, RAS cycling, Minimum cycle, CAS high (RAS only), RAS low after CAS low (CBR) | | 110 | | 100 | | mA |
| I _{CC4} ‡¶ | Average EDO current | V _{CC} = 5.5 V, RAS low, t _{HPC} = MIN, CAS cycling | | 90 | | 80 | | mA |

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while $\overline{\text{RAS}} = V_{IL}$

¶ Measured with a maximum of one address change while CAS = V_{IH}

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capacitance over recommended ranges of supply voltage and operating free-air temperature, $f = 1$ MHz (see Note 3)

| PARAMETER | | MIN | MAX | UNIT |
|-------------|--|-----|-----|------|
| $C_{i(A)}$ | Input capacitance, A0–A11† | | 5 | pF |
| $C_{i(OE)}$ | Input capacitance, \overline{OE} | | 7 | pF |
| $C_{i(RC)}$ | Input capacitance, \overline{CAS} and \overline{RAS} | | 7 | pF |
| $C_{i(W)}$ | Input capacitance, \overline{W} | | 7 | pF |
| C_o | Output capacitance | | 7 | pF |

† A11 is NC (no internal connection) for TMS417809.

NOTE 3: $V_{CC} = \text{NOM supply voltage} \pm 10\%$, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

| PARAMETER | '41x809-60 | | '41x809-70 | | '41x809-80 | | UNIT |
|-----------|---|-----|------------|-----|------------|-----|------|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{AA} | Access time from column address | | 30 | 35 | 40 | | ns |
| t_{CAC} | Access time from \overline{CAS} | | 15 | 18 | 20 | | ns |
| t_{CPA} | Access time from \overline{CAS} precharge | | 35 | 40 | 45 | | ns |
| t_{RAC} | Access time from \overline{RAS} | | 60 | 70 | 80 | | ns |
| t_{OEA} | Access time from \overline{OE} | | 15 | 18 | 20 | | ns |
| t_{CLZ} | Delay time, \overline{CAS} to output in low impedance | | 0 | 0 | 0 | | ns |
| t_{REZ} | Output buffer turn off delay from \overline{RAS} (see Note 5) | | 3 | 15 | 3 | 20 | ns |
| t_{CEZ} | Output buffer turn off delay from \overline{CAS} (see Note 5) | | 3 | 15 | 3 | 20 | ns |
| t_{OEZ} | Output buffer turn off delay from \overline{OE} (see Note 5) | | 3 | 15 | 3 | 20 | ns |
| t_{WEZ} | Output buffer turn off delay from \overline{W} (see Note 5) | | 3 | 15 | 3 | 20 | ns |

NOTES: 4. With ac parameters, it is assumed that $t_T = 5$ ns.

5. Maximum t_{REZ} , t_{CEZ} , t_{OEZ} , and t_{WEZ} are specified when the output is no longer driven.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

| | '41x809-60 | | '41x809-70 | | '41x809-80 | | UNIT |
|------------|---|-----|------------|-------|------------|-------|------|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{HPC} | Cycle time, EDO page mode, read-write | | 25 | 30 | 35 | | ns |
| t_{PRWC} | Cycle time, EDO read-write | | 80 | 90 | 100 | | ns |
| t_{CSH} | Delay time, \overline{RAS} active to \overline{CAS} precharge | | 50 | 55 | 60 | | ns |
| t_{CHO} | Hold time, \overline{OE} from \overline{CAS} | | 10 | 10 | 10 | | ns |
| t_{DOH} | Hold time, output from \overline{CAS} | | 3 | 3 | 3 | | ns |
| t_{CAS} | Pulse duration, \overline{CAS} active | | 10 | 10000 | 15 | 10000 | ns |
| t_{WPE} | Pulse duration, \overline{W} active (output disable only) | | 5 | 5 | 5 | | ns |
| t_{OCH} | Setup time, \overline{OE} before \overline{CAS} | | 10 | 10 | 10 | | ns |
| t_{CP} | Pulse duration, \overline{CAS} precharge | | 5 | 5 | 5 | | ns |
| t_{OEP} | Precharge time, \overline{OE} | | 5 | 5 | 5 | | ns |

NOTE 4: With ac parameters, it is assumed that $t_T = 5$ ns.

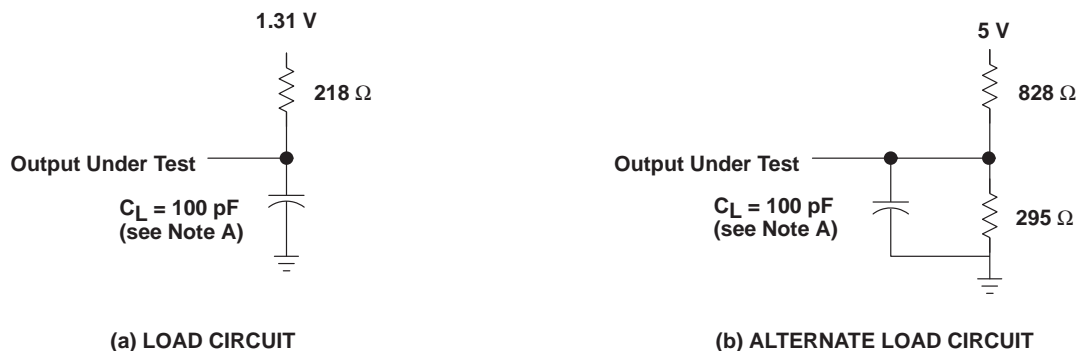


timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

| | | '41x809-60 | | '41x809-70 | | '41x809-80 | | UNIT |
|-------------------|--|------------|---------|------------|---------|------------|---------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{RC} | Cycle time, random read or write | 110 | | 130 | | 150 | | ns |
| t _{RWC} | Cycle time, read-write | 150 | | 175 | | 200 | | ns |
| t _{RASP} | Pulse duration, $\overline{\text{RAS}}$ active, fast page mode (see Note 6) | 60 | 100 000 | 70 | 100 000 | 80 | 100 000 | ns |
| t _{RAS} | Pulse duration, $\overline{\text{RAS}}$ active, non-page mode (see Note 6) | 60 | 10 000 | 70 | 10 000 | 80 | 10 000 | ns |
| t _{RP} | Pulse duration, RAS precharge | 40 | | 50 | | 60 | | ns |
| t _{WP} | Pulse duration, write command | 10 | | 10 | | 10 | | ns |
| t _{ASC} | Setup time, column address | 0 | | 0 | | 0 | | ns |
| t _{ASR} | Setup time, row address | 0 | | 0 | | 0 | | ns |
| t _{DS} | Setup time, data in (see Note 7) | 0 | | 0 | | 0 | | ns |
| t _{RCS} | Setup time, read command | 0 | | 0 | | 0 | | ns |
| t _{CWL} | Setup time, write command before $\overline{\text{CAS}}$ precharge | 10 | | 12 | | 15 | | ns |
| t _{RWL} | Setup time, write command before $\overline{\text{RAS}}$ precharge | 10 | | 12 | | 15 | | ns |
| t _{WCS} | Setup time, write command before $\overline{\text{CAS}}$ active (early-write only) | 0 | | 0 | | 0 | | ns |
| t _{CSR} | Setup time, $\overline{\text{CAS}}$ referenced to $\overline{\text{RAS}}$ (CBR refresh only) | 5 | | 5 | | 5 | | ns |
| t _{CAH} | Hold time, column address | 10 | | 12 | | 15 | | ns |
| t _{DH} | Hold time, data in (see Note 7) | 10 | | 12 | | 15 | | ns |
| t _{RAH} | Hold time, row address | 10 | | 10 | | 10 | | ns |
| t _{RCH} | Hold time, read command referenced to $\overline{\text{CAS}}$ (see Note 8) | 0 | | 0 | | 0 | | ns |
| t _{RRH} | Hold time, read command referenced to $\overline{\text{RAS}}$ (see Note 8) | 0 | | 0 | | 0 | | ns |
| t _{WCH} | Hold time, write command during $\overline{\text{CAS}}$ active (early-write only) | 10 | | 12 | | 15 | | ns |
| t _{ROH} | Hold time, $\overline{\text{RAS}}$ referenced to $\overline{\text{OE}}$ | 10 | | 10 | | 10 | | ns |
| t _{CHR} | Hold time, $\overline{\text{CAS}}$ referenced to $\overline{\text{RAS}}$ (CBR refresh only) | 15 | | 15 | | 20 | | ns |
| t _{OEH} | Hold time, $\overline{\text{OE}}$ command | 15 | | 18 | | 20 | | ns |
| t _{AWD} | Delay time, column address to write command (read-write only) | 55 | | 63 | | 70 | | ns |
| t _{CRP} | Delay time, $\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ | 0 | | 0 | | 0 | | ns |
| t _{CWD} | Delay time, $\overline{\text{CAS}}$ to write command (read-write only) | 40 | | 46 | | 50 | | ns |
| t _{OED} | Delay time, $\overline{\text{OE}}$ to data in | 15 | | 18 | | 20 | | ns |
| t _{RAD} | Delay time, $\overline{\text{RAS}}$ to column address | 15 | 30 | 15 | 35 | 15 | 40 | ns |
| t _{RAL} | Delay time, column address to RAS precharge | 30 | | 35 | | 40 | | ns |
| t _{CAL} | Delay time, column address to $\overline{\text{CAS}}$ precharge | 20 | | 25 | | 30 | | ns |
| t _{RCD} | Delay time, $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ (see Note 9) | 20 | 45 | 20 | 52 | 20 | 60 | ns |
| t _{RPC} | Delay time, $\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ | 0 | | 0 | | 0 | | ns |
| t _{RSH} | Delay time, $\overline{\text{CAS}}$ active to RAS precharge | 10 | | 12 | | 15 | | ns |
| t _{RWD} | Delay time, $\overline{\text{RAS}}$ to write command (read-write only) | 85 | | 98 | | 110 | | ns |
| t _{REF} | Refresh time interval | '416809 | 64 | | 64 | | 64 | ms |
| | | '417809 | 32 | | 32 | | 32 | |
| t _T | Transition time | 2 | 30 | 2 | 30 | 2 | 30 | ns |

- NOTES:
4. With ac parameters, it is assumed that $t_T = 5$ ns.
 6. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
 7. Referenced to the later of $\overline{\text{CAS}}$ or $\overline{\text{W}}$ in write operations
 8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
 9. The maximum value is specified only to ensure access time.

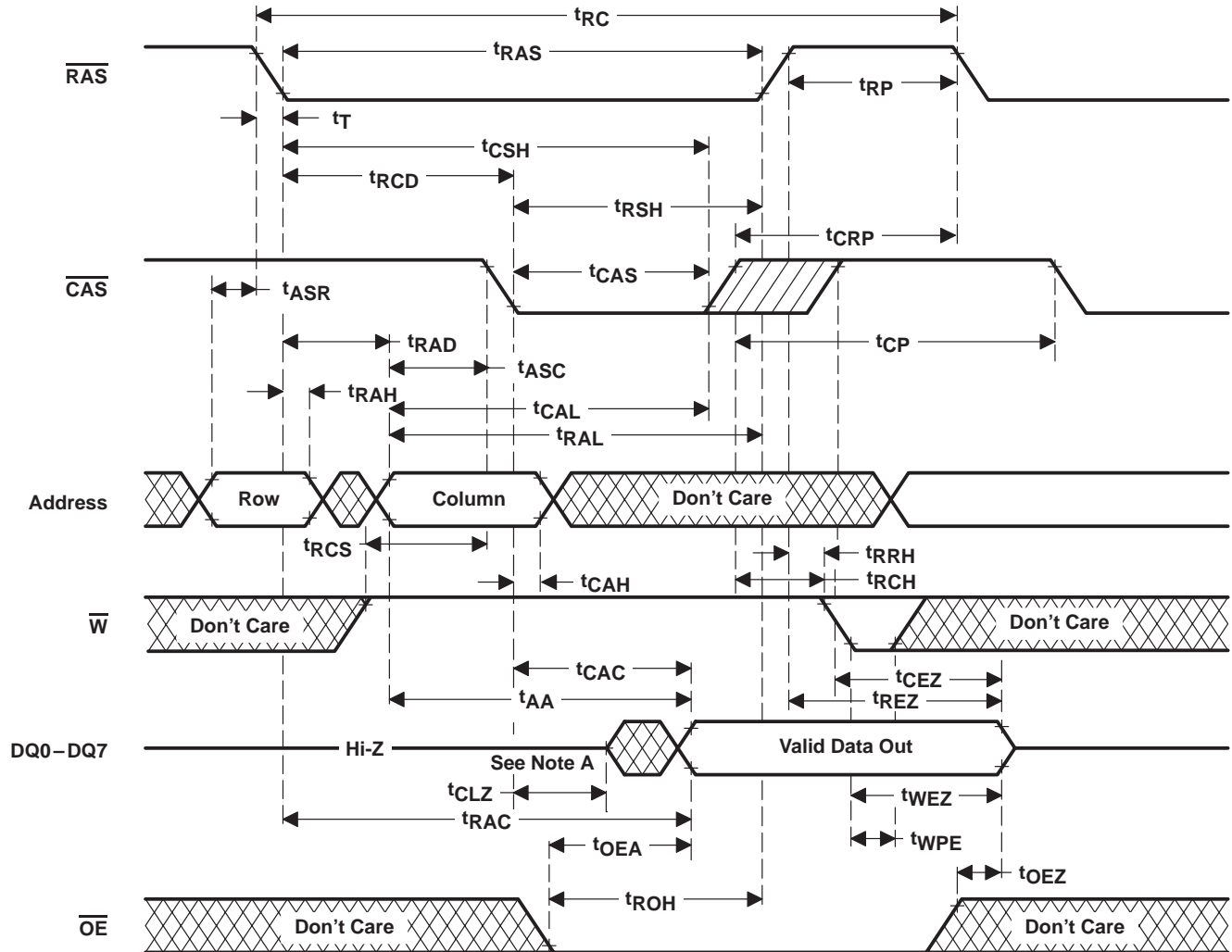
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

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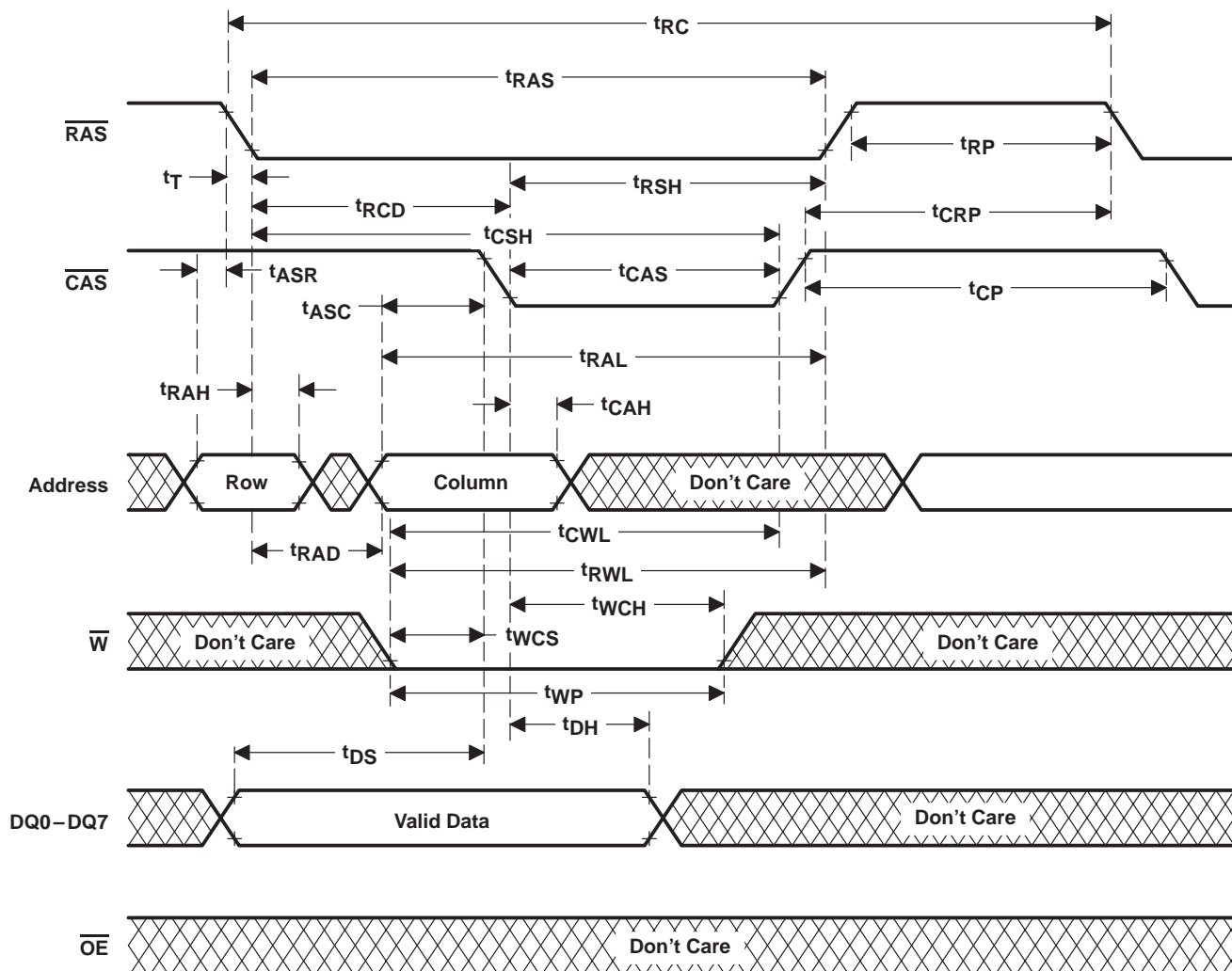


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

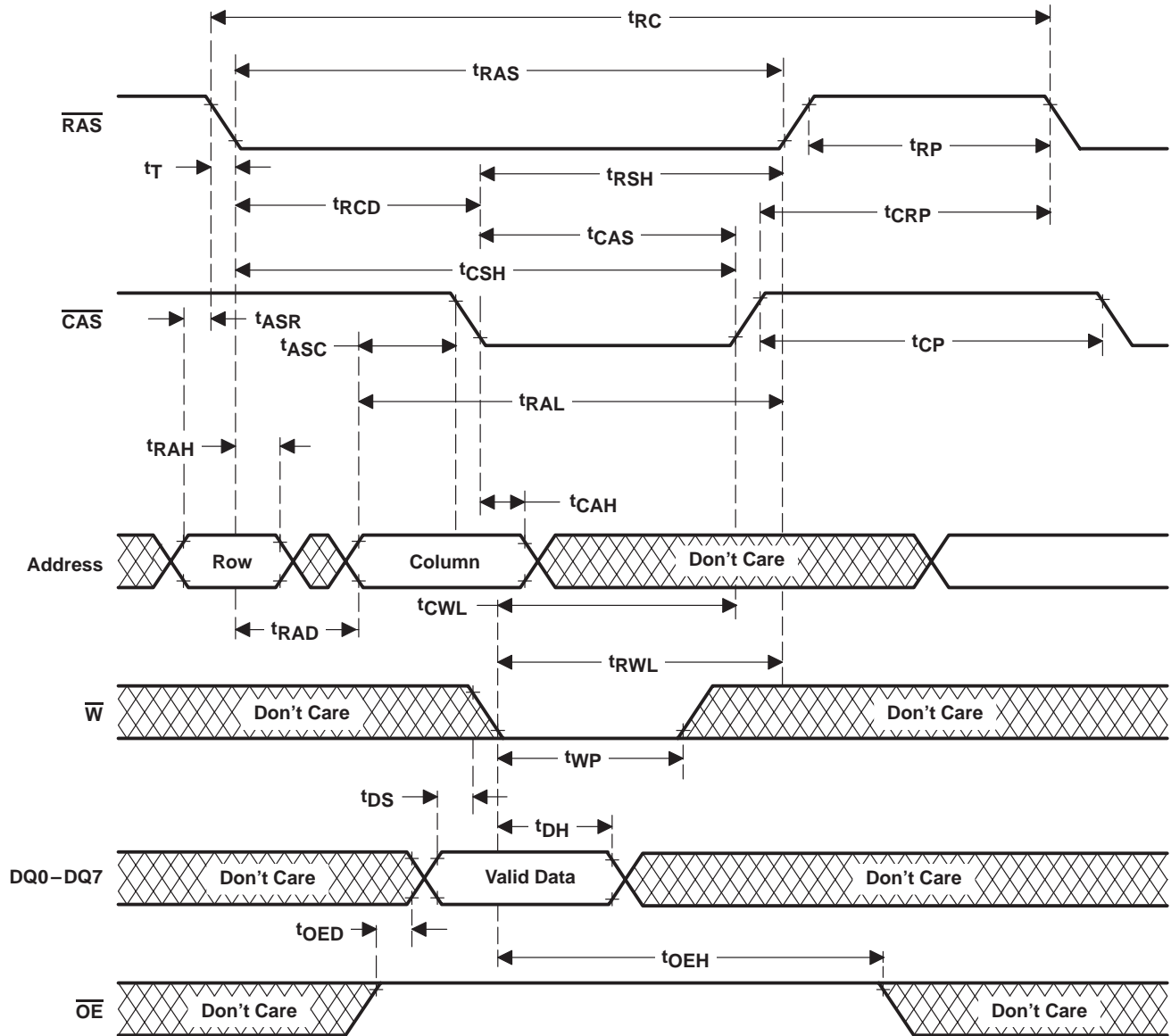
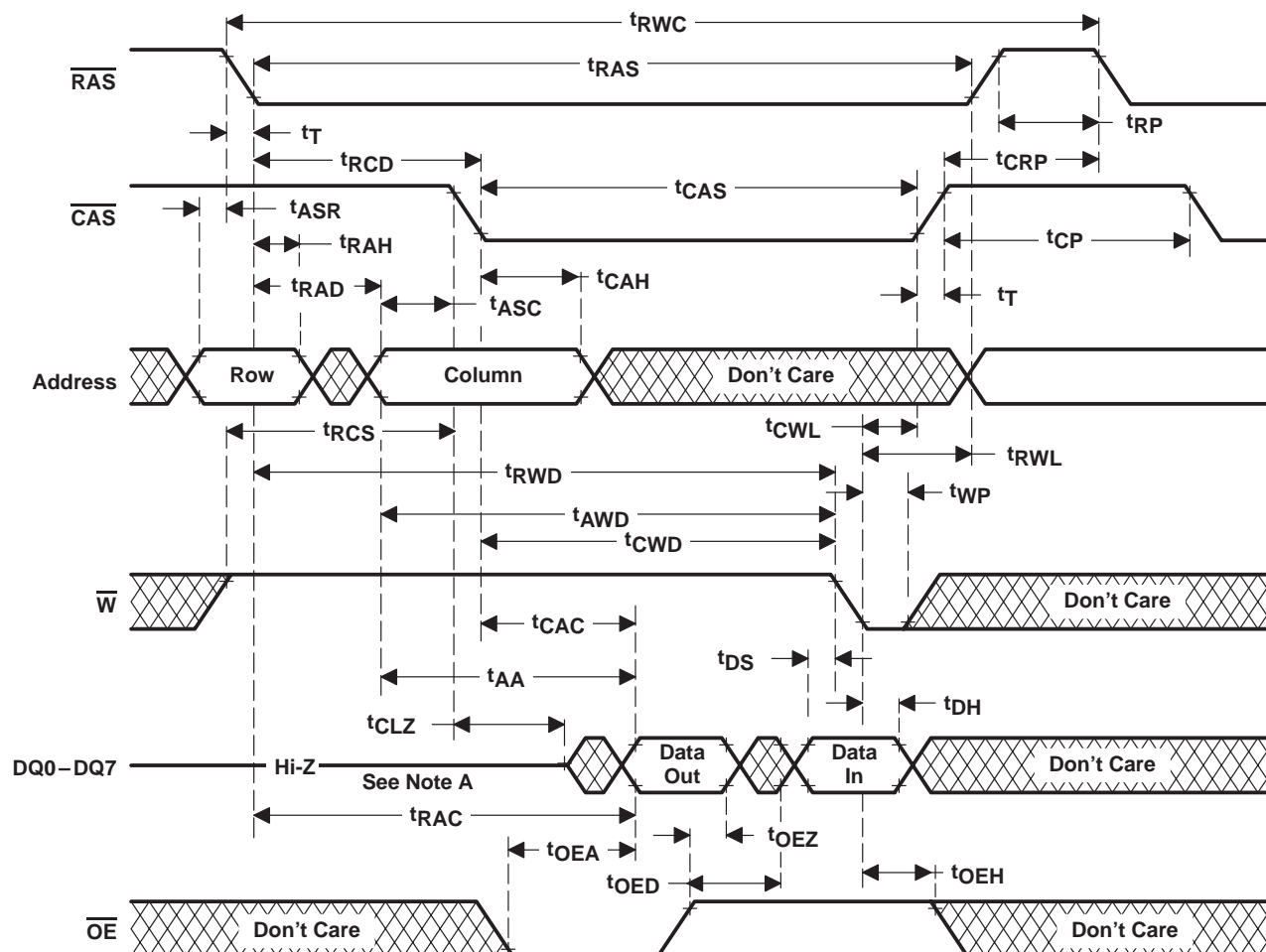


Figure 4. Write-Cycle Timing

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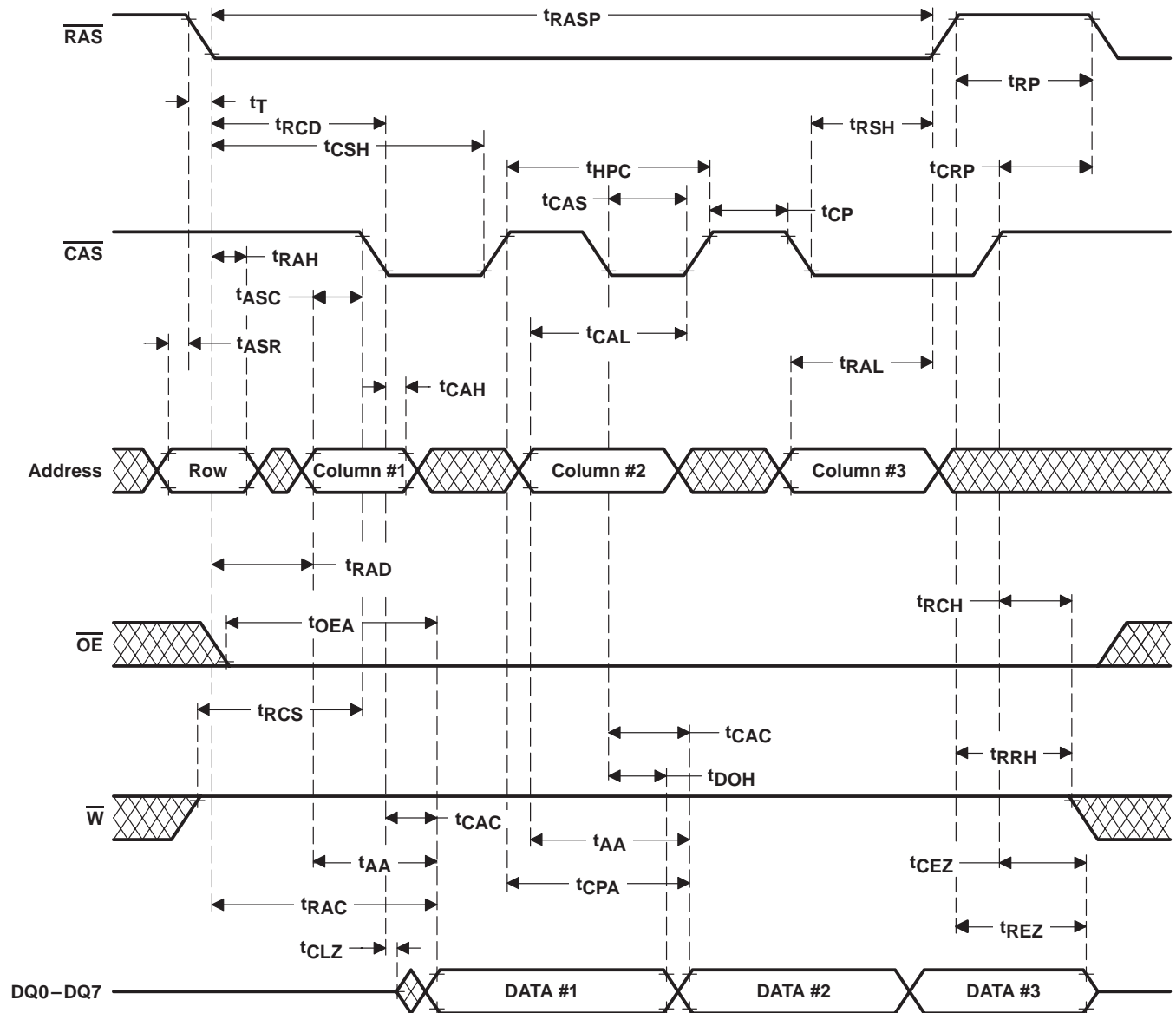
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. Access time is t_{CPA} - or t_{AA} -dependent.

Figure 6. Extended-Data-Out Read Cycle

TMS416809, TMS417809

2097152-WORD BY 8-BIT HIGH-SPEED DRAMS

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PARAMETER MEASUREMENT INFORMATION

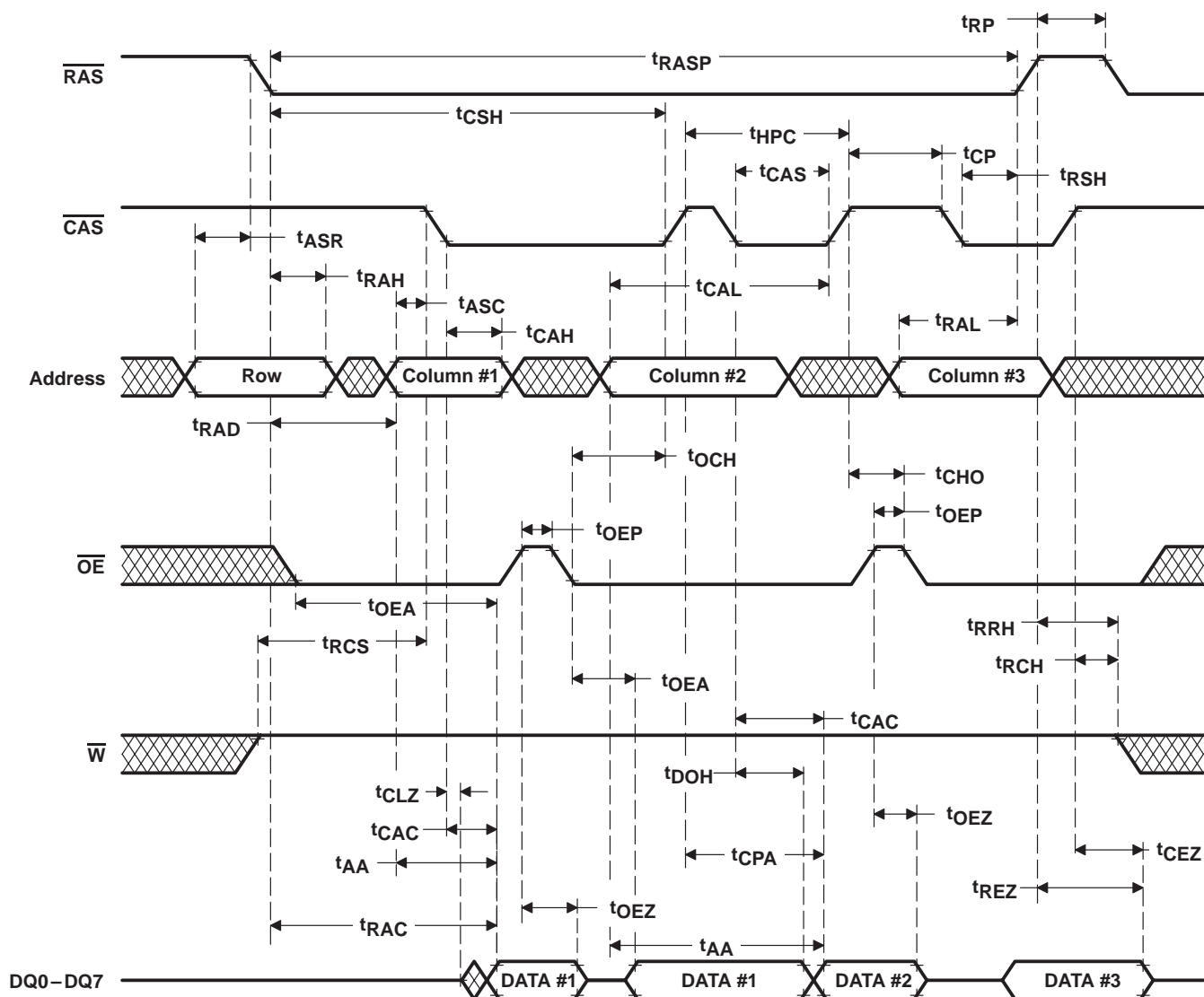


Figure 7. Extended-Data-Out Read-Cycle With \overline{OE} Control

PARAMETER MEASUREMENT INFORMATION

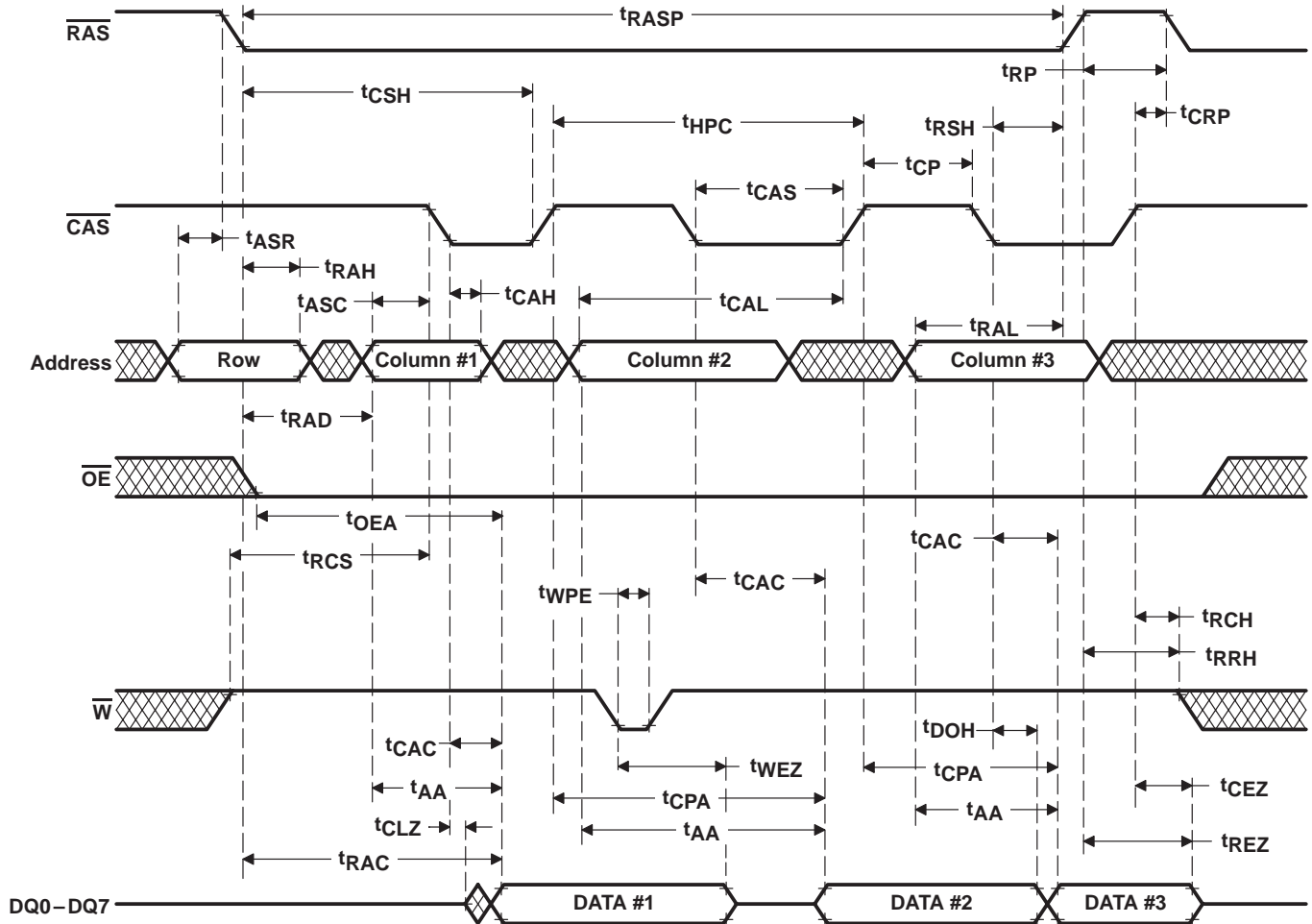
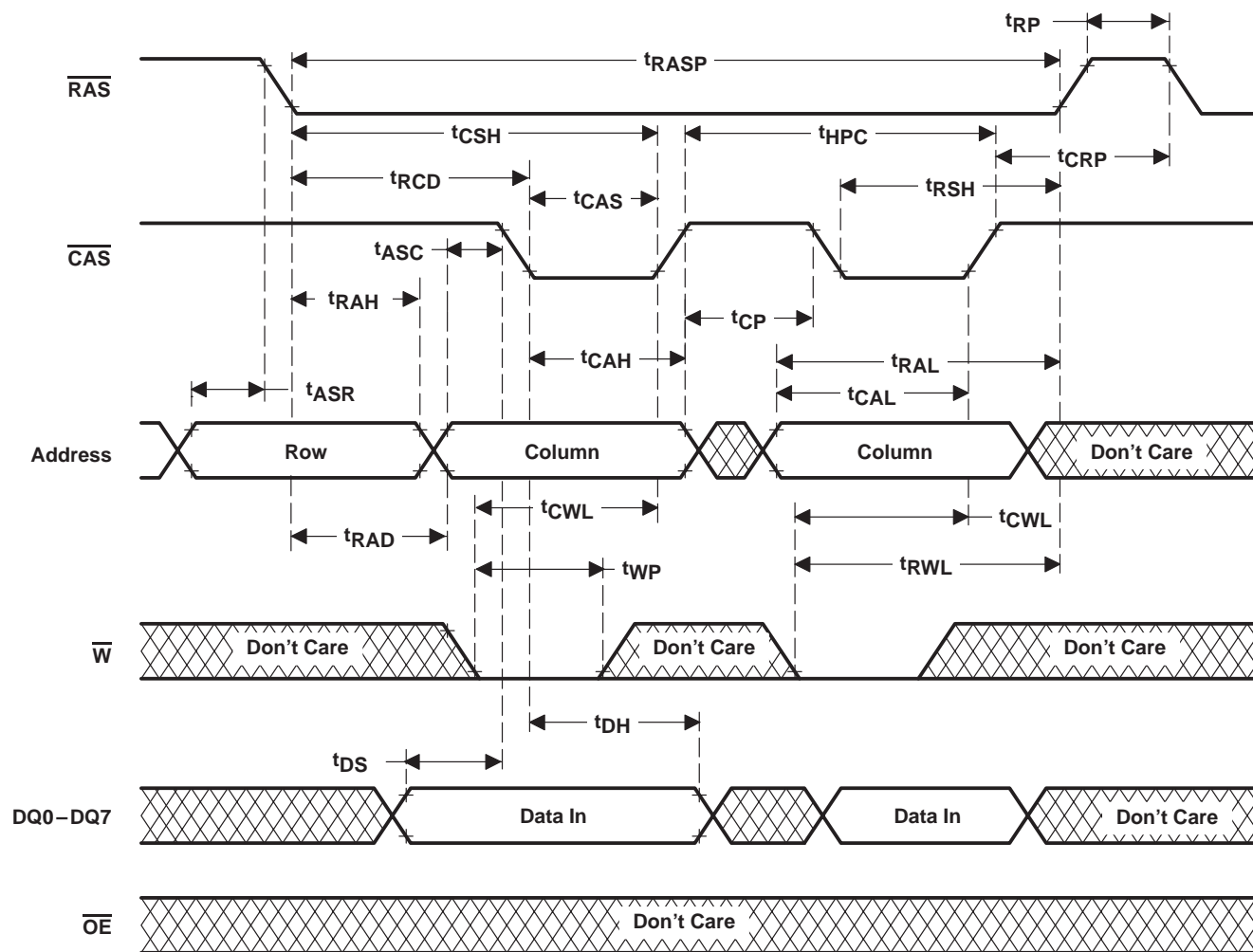


Figure 8. Extended-Data-Out Read-Cycle With \overline{W} Control

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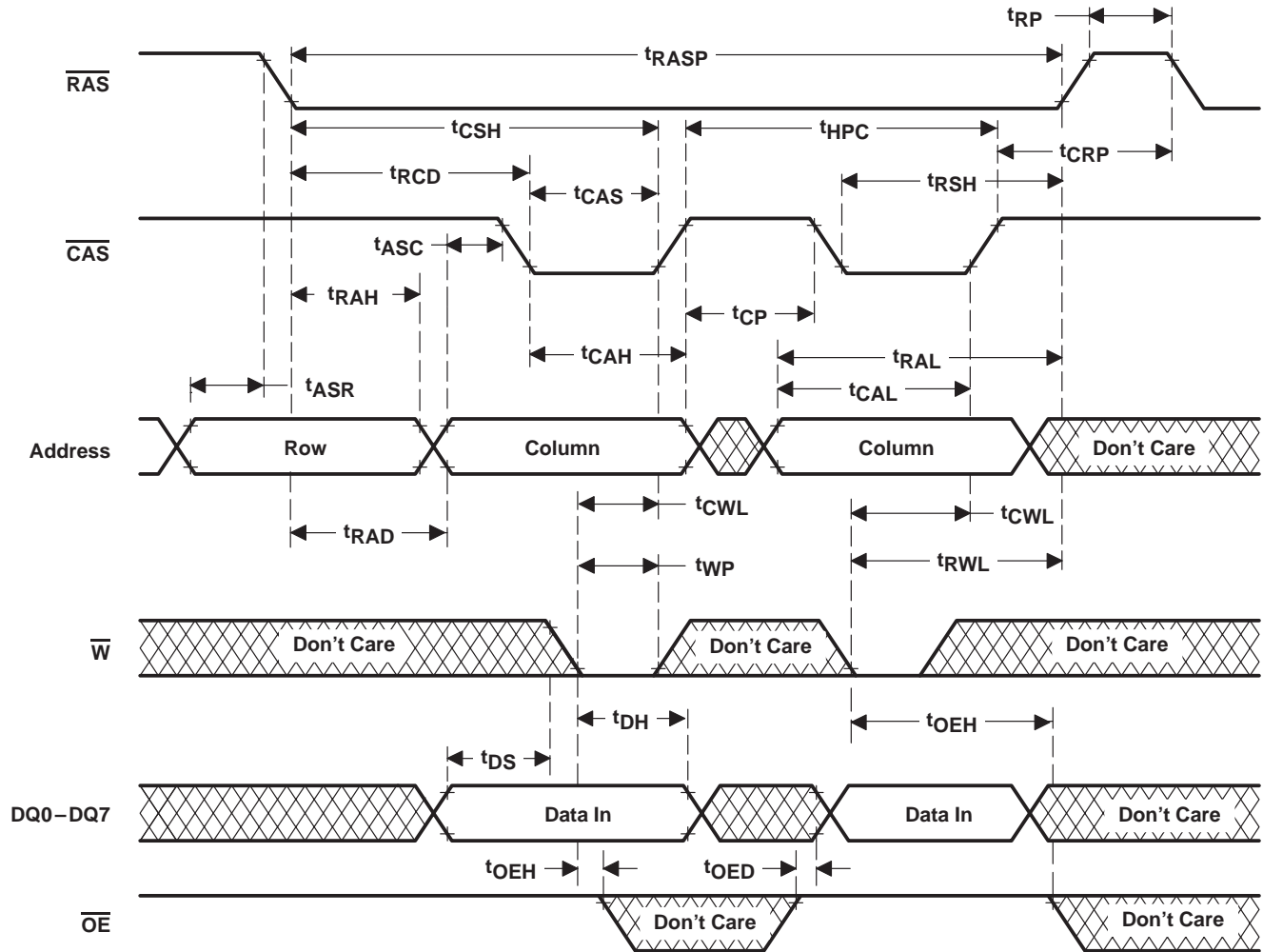
PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 9. EDO-Early-Write-Cycle Timing

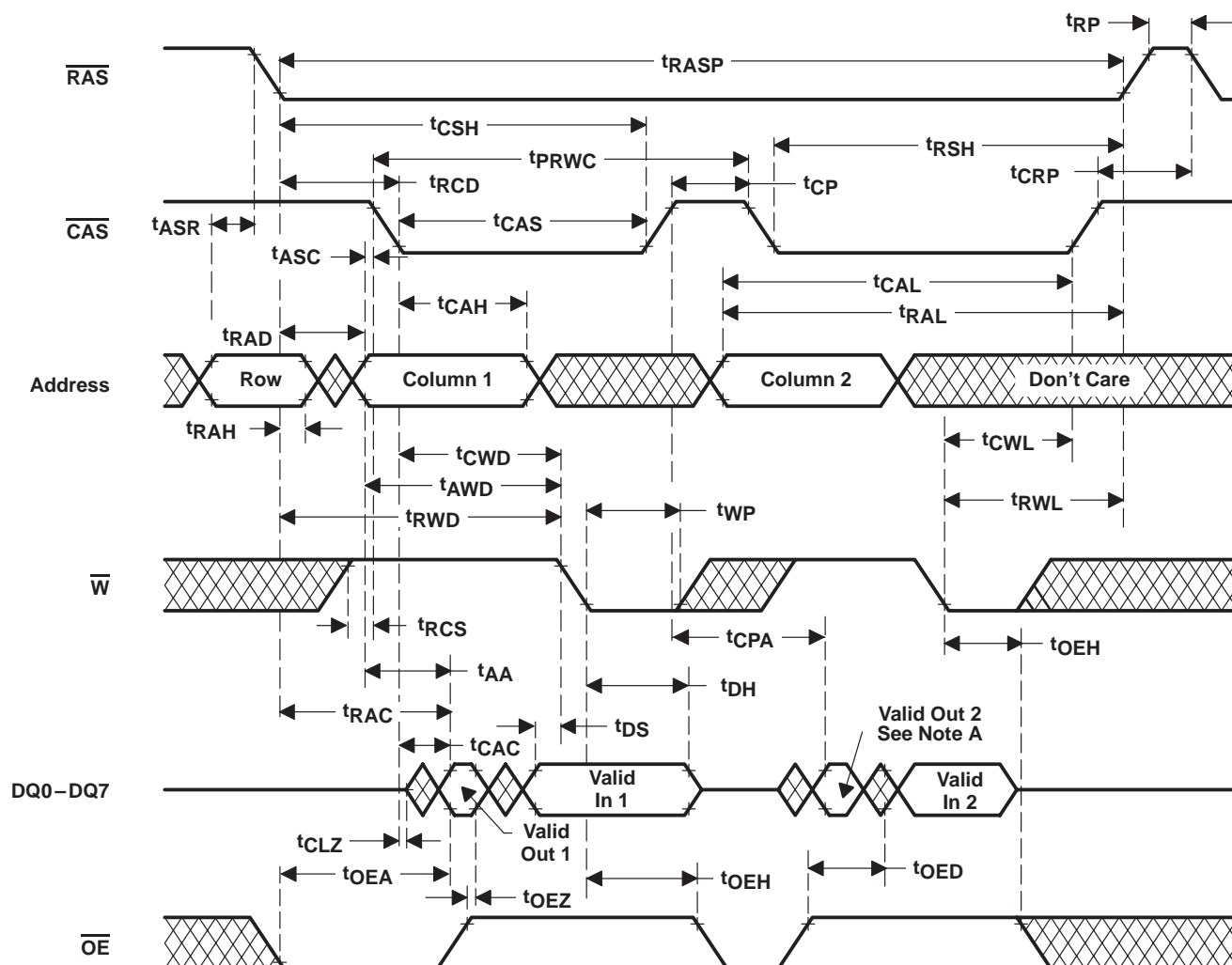
PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 10. EDO-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-write cycles as long as the read- and write-timing specifications are not violated.

Figure 11. EDO Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

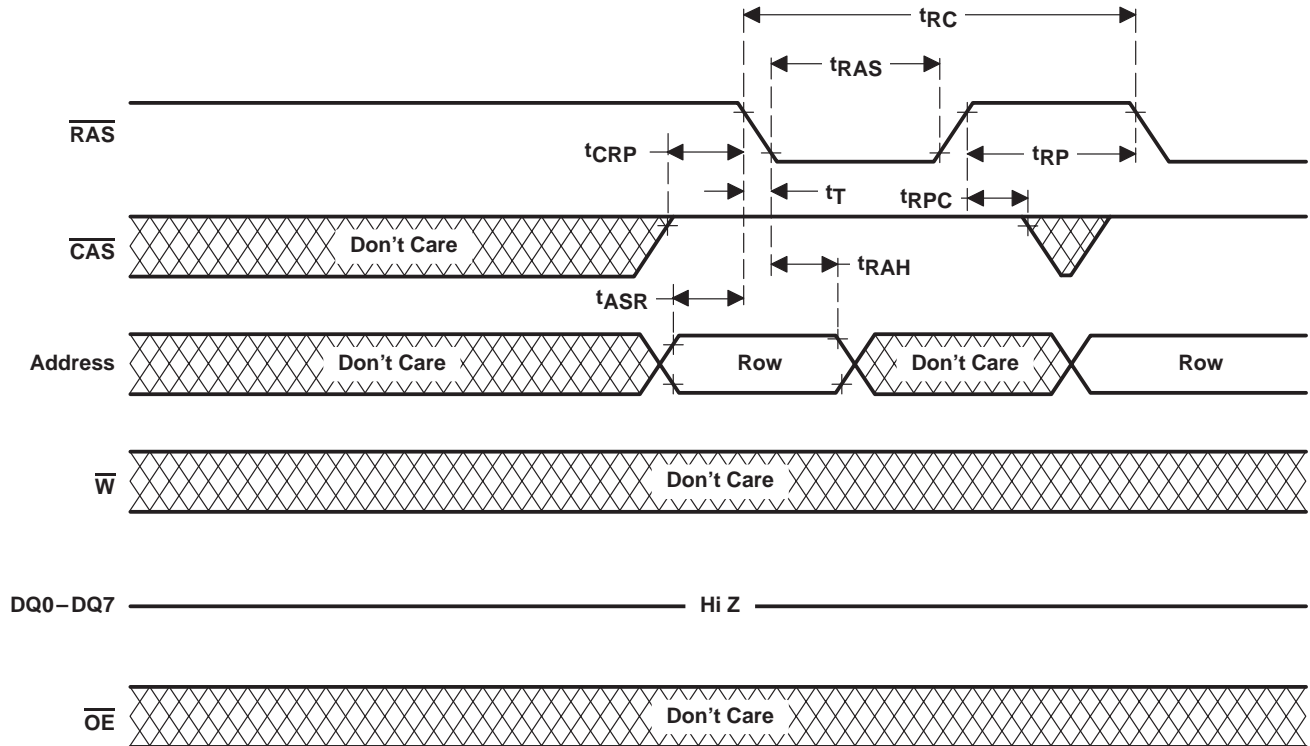


Figure 12. $\overline{\text{RAS}}$ -Only Refresh-Cycle Timing

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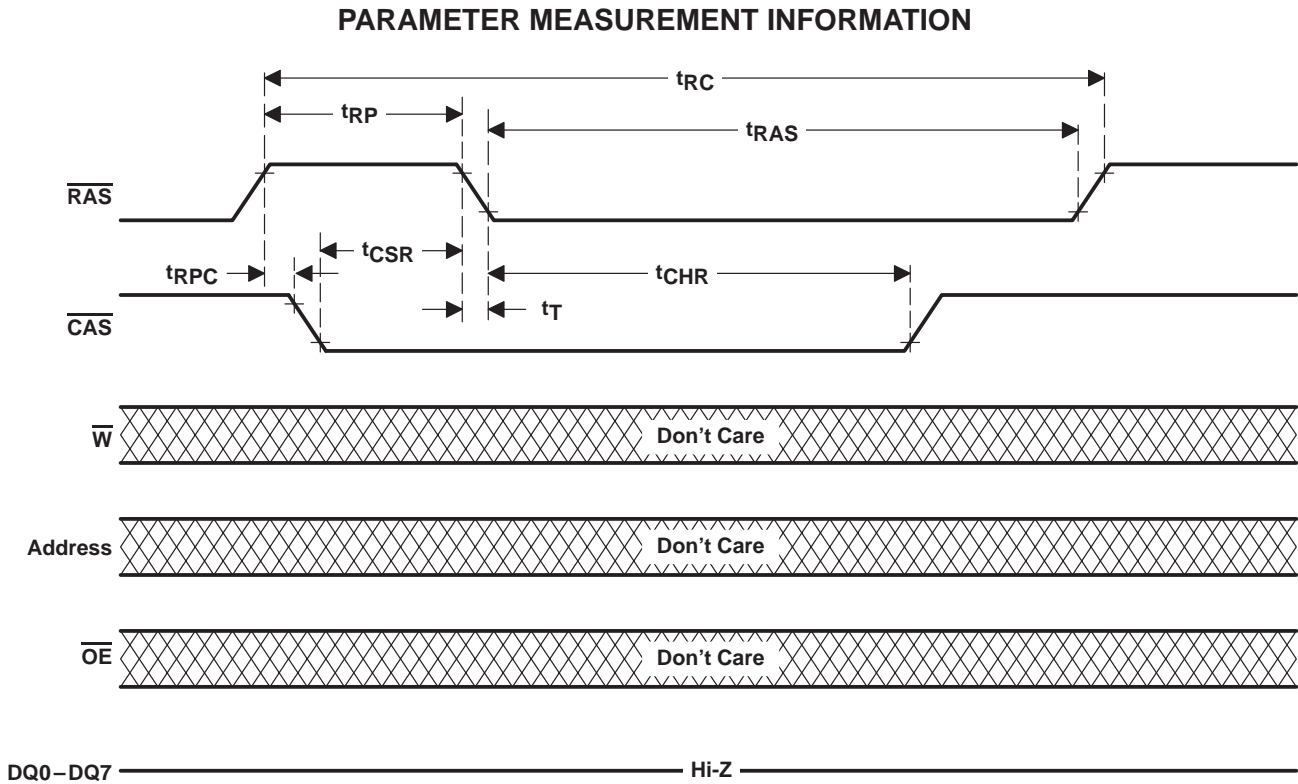


Figure 13. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

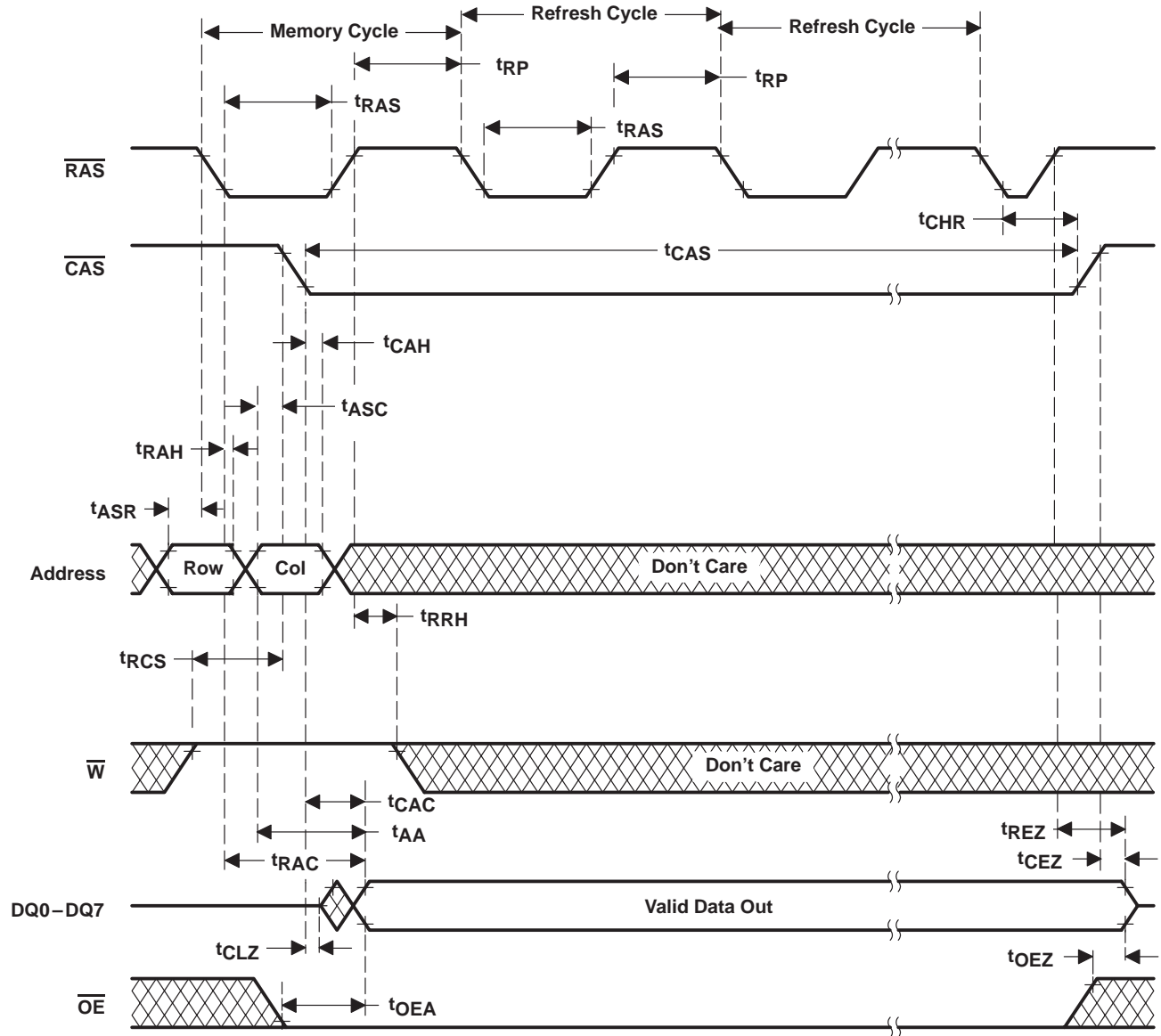


Figure 14. Hidden-Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION

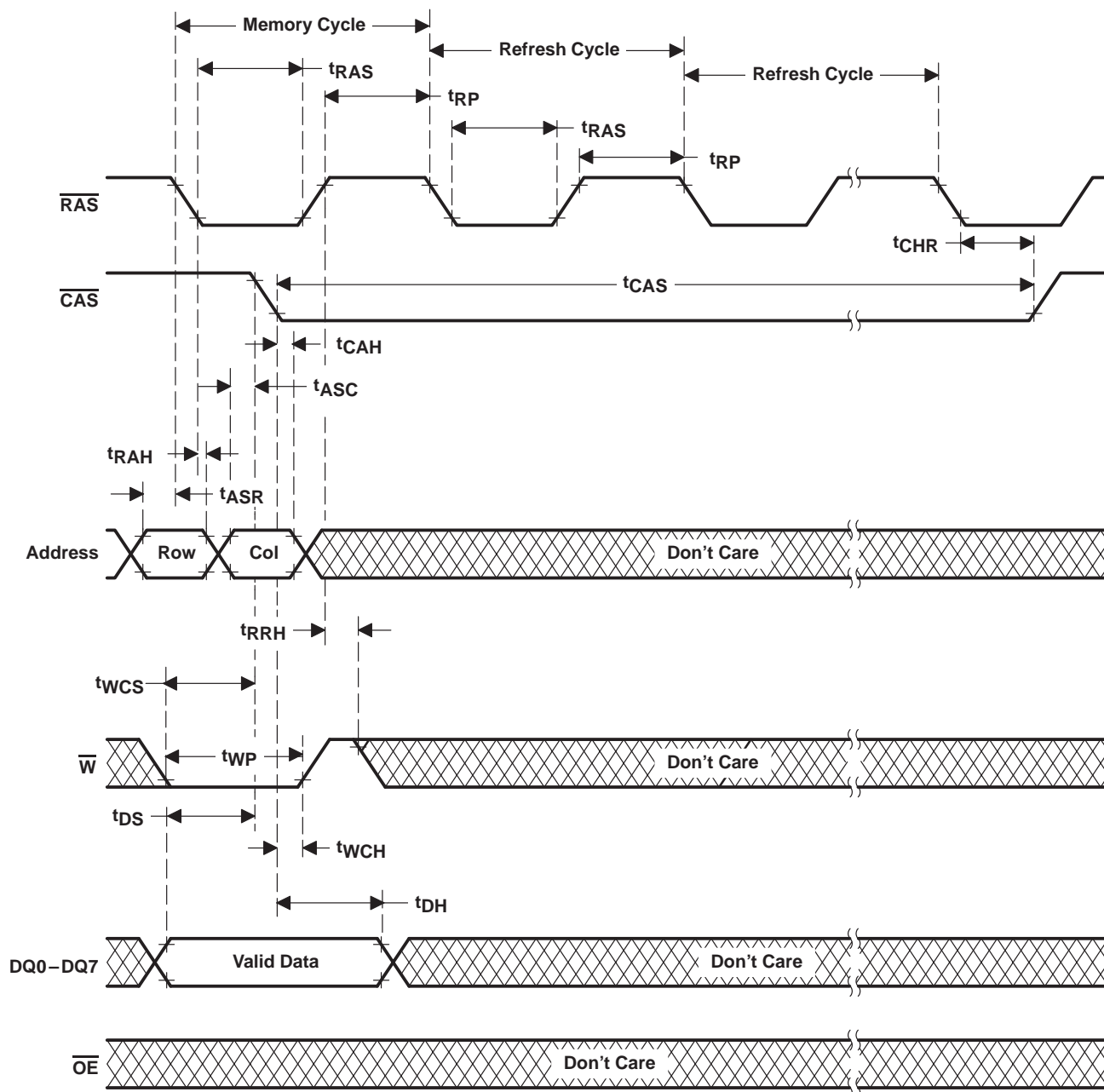
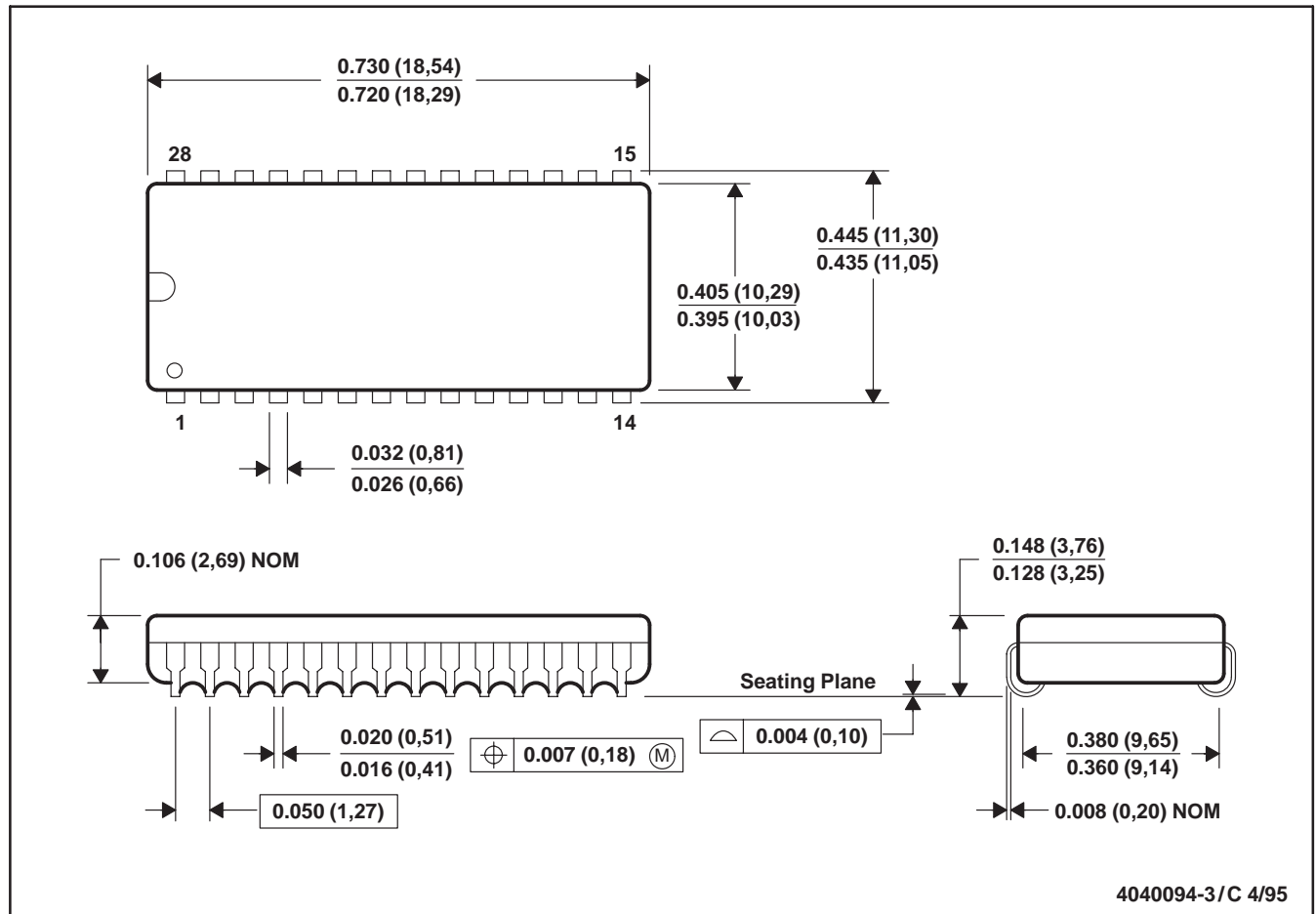


Figure 15. Hidden-Refresh Cycle (Write) Timing

MECHANICAL DATA

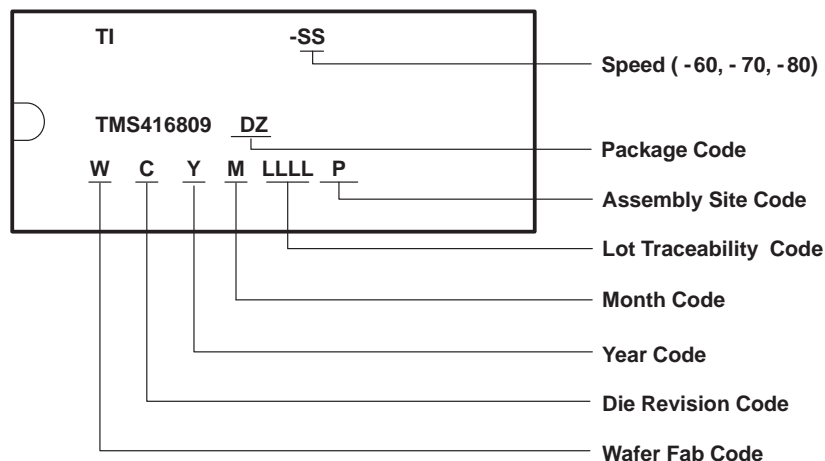
DZ (R-PDSO-J28)

PLASTIC SMALL-OUTLINE J-LEAD PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

device symbolization (TMS416809 illustrated)



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