

NT511740C5J

NT 511740C5J Data Sheet

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1. DESCRIPTION

The NT511740C5J is a 4,194,304-word x 4-bit dynamic RAM fabricated in NTC's CMOS silicon gate technology. The NT511740C5J achieves high integration , high-speed operation , and low-power consumption due to quadruple polysilicon double metal CMOS. The NT511740C5J is available in a 26/24-pin plastic SOJ.

2. FEATURES

- 4,194,304-word x 4-bit configuration
- Single 5V power supply, $\pm 10\%$ tolerance
- Input :TTL compatible , low input capacitance
- Output :TTL compatible , 3-state
- Refresh :2048 cycles/32 ms
- Fast page mode with EDO, read modify write capability
- CAS before RAS refresh, hidden refresh, RAS-only refresh capability
- Multi-bit test mode capability
- Package options:

26/24-Pin 300 mil plastic SOJ (SOJ26/24-P300) (Product:NT511740C5J-XX)

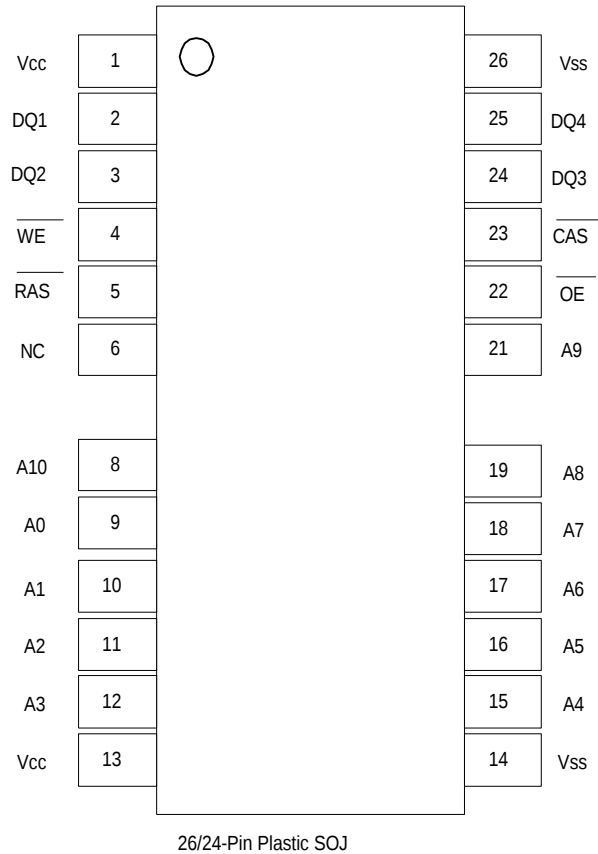
XX indicates speed rank.

3. PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operation(Max.)	Standby(Max.)
NT511740C5J-50	50ns	25ns	13ns	13ns	84ns	660mW	5.5 mW
NT511740C5J-60	60 ns	30 ns	15 ns	15 ns	104 ns	605mW	
NT511740C5J-70	70 ns	35 ns	20 ns	20 ns	124 ns	550 mW	

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4. PIN CONFIGURATION (TOPVIEW)

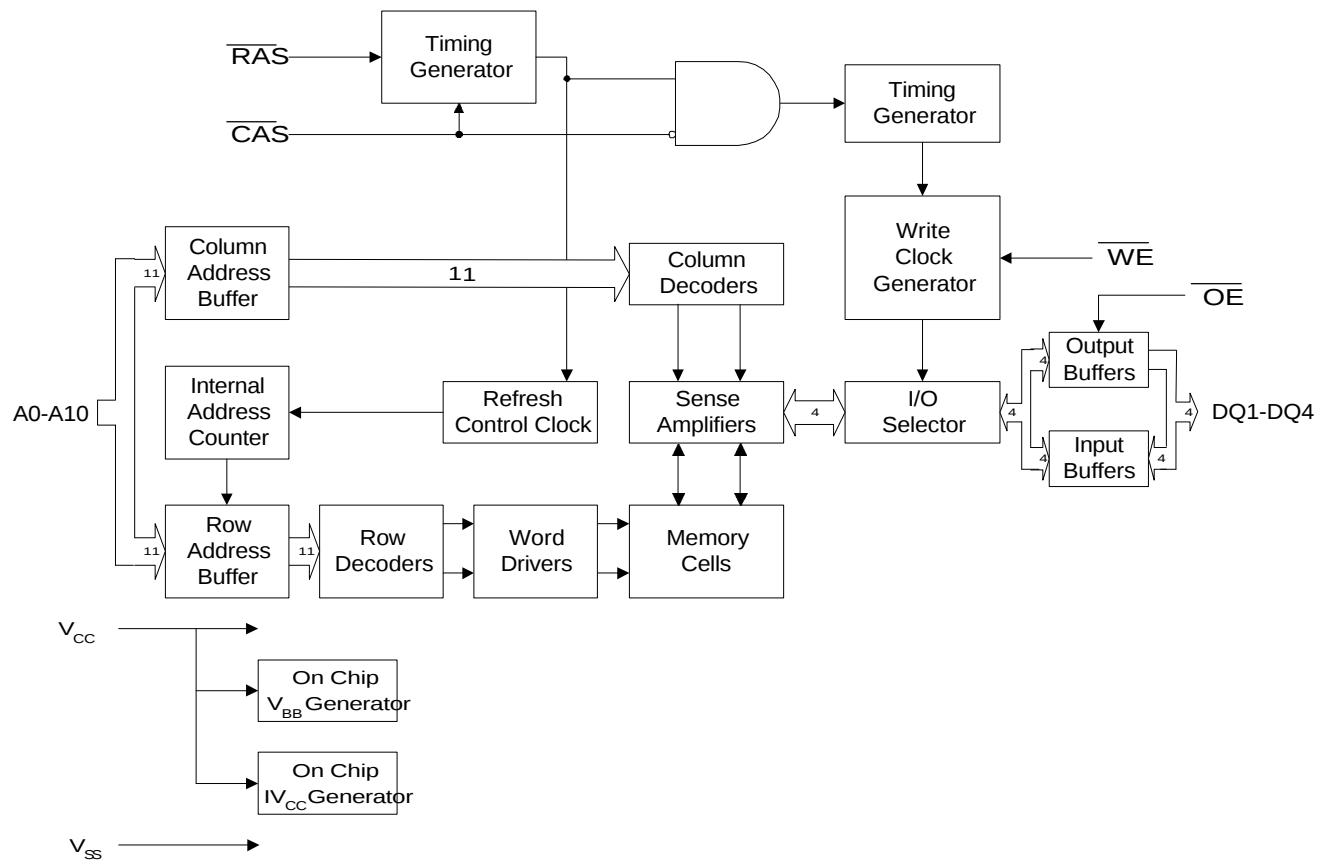


Pin Name	Function
A0-A10	Adress input
$\overline{\text{RAS}}$	Row Adress Strobe
$\overline{\text{CAS}}$	Column Adress Strobe
DQ1-DQ4	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
Vcc	Power Supply (5v)
Vss	Ground(0V)
NC	No Connection

Note:The same power supply voltage must be provided to every Vcc pin , and the same GND voltage level must be provided to every Vss pin.

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5. BLOCK DIAGRAM



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6. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.3 to V _{CC} +0.3	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-0.5 to 7	V
Short Circuit Output Current	I _{OS}	50	mA
Power Dissipation	P _D *	1	W
Operation Temperature	T _{opr}	0 to 70	
Storage Temperature	T _{stg}	-55 to 150	

*:Ta = 25

Recommended Operating Conditions

(Ta=0 to 70)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL}	-0.3	-	0.8	V

Capacitance

(V_{CC} = 5V±10%, Ta=25 , f=1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0-A10)	C _{IN1}	-	5	pF
Input Capacitance (RAS,CAS,WE,OE)	C _{IN2}	-	7	pF
Output Capacitance (DQ1-DQ4)	C _{I/O}	-	7	pF

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7. DC Characteristics

(V_{CC}=5V±10% , Ta=0 to

70 °C)

Parameter	Symbol	Condition	NT511740C 5J-50		NT511740C 5J-60		NT511740C 5J-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V _{OH}	I _{OH} = -5.0 mA	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	
Output LOW Voltage	V _{OL}	I _{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0V V _I 6.5V; All other pins not under test = 0V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0V V _O 5.5V	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = Min.	-	120	-	110	-	100	mA	1,2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = V _{IH}	-	2	-	2	-	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ V _{CC} = 0.2V	-	1	-	1	-	1		
Average Power Supply Current (RAS-only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V _{IH} , t _{RC} = Min.	-	120	-	110	-	110	mA	1,2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}}$ = V _{IH} , $\overline{\text{CAS}}$ = V _{IL} , DQ = enable	-	5	-	5	-	5	mA	1
Average Power Supply Current (CAS before RAS Refresh)	I _{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	-	110	-	100	-	90	mA	1,2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}}$ = V _{IL} , $\overline{\text{CAS}}$ cycling t _{PC} = Min.	-	110	-	100	-	90	mA	1,3

Notes

1. ICC Max. is specified as I_{CC} for output open condition.2. Address can be changed once or less while RAS = V_{IL}.2. ~~3.~~ Address can be changed once or less while CAS = V_{IH}.

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8. AC Characteristics (1/3)

(V_{cc}=5V±10% , T_a=0 to 70) Note:1,2,3,12,13

Parameter	Symbol	NT511740C5J-50		NT511740C5J-60		NT511740C5J-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	84	-	104	-	124	-	ns	
Read Modify Write Cycle Time	t _{RWC}	110	-	135	-	160	-	ns	
Fast Page Mode Cycle Time	t _{HPC}	20	-	25	-	30	-	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	58	-	68	-	78	-	ns	
Access Time form $\overline{\text{RAS}}$	t _{RAC}	-	50	-	60	-	70	ns	4,5,6
Access Time form $\overline{\text{CAS}}$	t _{CAC}	-	13	-	15	-	20	ns	4,5
Access Time form Column Address	t _{AA}	-	25	-	30	-	35	ns	4,6
Access Time form $\overline{\text{CAS}}$ Precharge	t _{CPA}	-	30	-	35	-	40	ns	4
Access Time form $\overline{\text{OE}}$	t _{OEA}	-	13	-	15	-	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	-	0	-	0	-	ns	4
Data Output Hold After $\overline{\text{CAS}}$ Low	t _{DOH}	5	-	5	-	5	-	ns	
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{CEZ}	0	13	0	15	0	20	ns	7,8
$\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time	t _{REZ}	0	13	0	15	0	20	ns	7,8
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	13	0	15	0	20	ns	7
$\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time	t _{WEZ}	0	13	0	15	0	20	ns	7
Transition Time	t _T	1	50	1	50	1	50	ns	3
Refresh Period	t _{REF}	-	32	-	32	-	32	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30	-	40	-	50	-	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)	t _{RASP}	50	100,000	60	100,000	70	100,000	ns	

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AC Characteristics (2/3)

Parameter	Symbol	NT10511740C5J-		NT511740C5J-		NT511740C5J-		Unit	Note
		50		60		70			
		Min.	Max.	Min.	Max.	Min.	Max.		
RAS Hold Time	t _{RSH}	7	-	10	-	13	-	ns	
RAS Hold Time referenced to OE	t _{ROH}	7	-	10	-	13	-	ns	
CAS Precharge Time (Fast Page Mode with EDO)	t _{CP}	7	-	10	-	13	-	ns	
CAS Pulse Width	t _{CAS}	7	10,000	10	10,000	13	10,000	ns	
CAS Hold Time	t _{CSH}	35	-	40	-	45	-	ns	
CAS to RAS Precharge Time	t _{CRP}	5	-	5	-	5	-	ns	
RAS Hold Time from CAS Precharge Time	t _{RHCP}	30	-	35	-	40	-	ns	
OE Hold Time from CAS (DQ Disable)	t _{CHO}	5	-	5	-	5	-	ns	
RAS to CAS Delay Time	t _{RCD}	11	37	14	45	14	50	ns	5
RAS to Column Address Delay Time	t _{RAD}	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t _{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t _{RAH}	7	-	10	-	13	-	ns	
Column Address Set-up Time	t _{ASC}	0	-	0	-	0	-	ns	
Column Address Hold Time	t _{CAH}	7	-	10	-	13	-	ns	
Column Address to RAS Lead Time	t _{RAL}	25	-	30	-	35	-	ns	
Read Command Set-up Time	t _{RCS}	0	-	0	-	0	-	ns	
Read Command Hold Time	t _{RCH}	0	-	0	-	0	-	ns	9
Read Command Hold Time referenced to RAS	t _{RRH}	0	-	0	-	0	-	ns	9
Write Command Set-up Time	t _{WCS}	0	-	0	-	0	-	ns	10

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AC Characteristics (3/3)

(V_{CC}=5V±10% ,T_a=0 to 70) Note 1,2,3,12,13

Parameter	Symbol	NT511740C5J-		NT511740C5J-		NT511740A5J-		Unit	Note
		50		60		70			
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Hold Time	t _{WCH}	7	-	10	-	13	-	ns	
Write Command Pulse Width	t _{WP}	7	-	10	-	10	-	ns	
WE Pulse Width (DQ Disable)	t _{WPE}	7	-	10	-	10	-	ns	
OE Command Hold Time	t _{OEH}	7	-	10	-	13	-	ns	
OE Precharge Time	t _{OEP}	7	-	10	-	10	-	ns	
OE Command Hold Time	t _{OCH}	7	-	10	-	10	-	ns	
Write Command to RAS Lead Time	t _{RWL}	7	-	10	-	13	-	ns	
Write Command to CAS Lead Time	t _{CWL}	7	-	10	-	13	-	ns	
Data-in Set-up Time	t _{DS}	0	-	0	-	0	-	ns	11
Data-in Hold Time	t _{DH}	7	-	10	-	13	-	ns	11
OE to Data-in Delay Time	t _{OED}	13	-	15	-	20	-	ns	
CAS to WE Delay Time	t _{CWD}	30	-	34	-	44	-	ns	10
Column Address to WE Delay Time	t _{AWD}	42	-	49	-	59	-	ns	10
RAS to WE Delay Time	t _{RWD}	67	-	79	-	94	-	ns	10
CAS Precharge WE Delay Time	t _{CPWD}	47	-	54	-	64	-	ns	10
CAS Active Delay Time from RAS Precharge	t _{RPC}	5	-	5	-	5	-	ns	
RAS to CAS Set-up Time (CAS before RAS)	t _{CSR}	5	-	5	-	5	-	ns	
RAS to CAS Hold Time (CAS before RAS)	t _{CHR}	10	-	10	-	10	-	ns	
WE to RAS Precharge Time (CAS before RAS)	t _{WRP}	10	-	10	-	10	-	ns	
WE Hold Time RAS (CAS before RAS)	t _{WRH}	10	-	10	-	10	-	ns	
RAS to WE Set-up Time (Test Mode)	t _{WTS}	10	-	10	-	10	-	ns	
RAS to WE Hold Time (Test Mode)	t _{WTH}	10	-	10	-	10	-	ns	

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Notes:

1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
2. The AC characteristics assume $t_T=2$ ns.
3. $V_{IH}(\text{Min.})$ and $V_{IL}(\text{Max.})$ are reference levels for measuring input timing signals. Transition time (t_T) are measured between V_{IH} and V_{IL} .
4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
5. Operation within the $t_{RCD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met.
 $t_{RCD}(\text{Max.})$ is specified as a reference point only . If t_{RCD} is greater than the specified $t_{RCD}(\text{Max.})$ limit, access time is controlled by t_{CAC} .
6. Operation within the $t_{RAD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met.
 $t_{RAD}(\text{Max.})$ is specified as a reference point only . If t_{RAD} is greater than the specified $t_{RAD}(\text{Max.})$ limit, access time is controlled by t_{AA} .
7. $t_{CEZ}(\text{Max.})$, $t_{REZ}(\text{Max.})$, $t_{WEZ}(\text{Max.})$ and $t_{OEZ}(\text{Max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
- ~~2.~~ 8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition .
- ~~3.~~ 9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- ~~4.~~ 10. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} , and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only . If $t_{WCS} t_{WCS}(\text{Min.})$, the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} t_{CWD}(\text{Min.})$, $t_{RWD} t_{RWD}(\text{Min.})$, $t_{AWD} t_{AWD}(\text{Min.})$ and $t_{CPWD} t_{CPWD}(\text{Min.})$, the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- ~~5.~~ 11. These parameters are referenced to CAS leading edge in an early write cycle, and to WE leading edge in an OE control write cycle or a read modify write cycle .
- ~~6.~~ 12. The test mode is initiated by performing a WE and CAS before RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test mode CA0 and CA1 are not used and each DQ pin now accesses 8-bit locations .Since all 4 DQ pins are used, a total of 32 data bits can be written in parallel into the memory array. In a read cycle, if 8 data bits are equal the DQ pin will indicate a high level. If the 8 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a RAS-only refresh cycle or a CAS before RAS refresh cycle.
- ~~7.~~ 13. In a test mode read cycle , the value of access time parameters is delayed for 5 ns for the specified value . These parameters should be specified in test mode cycle by adding the above value

4,194,304-word x 4-bit

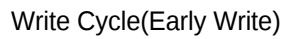
Dynamic RAM : Fast Page Mode with EDO

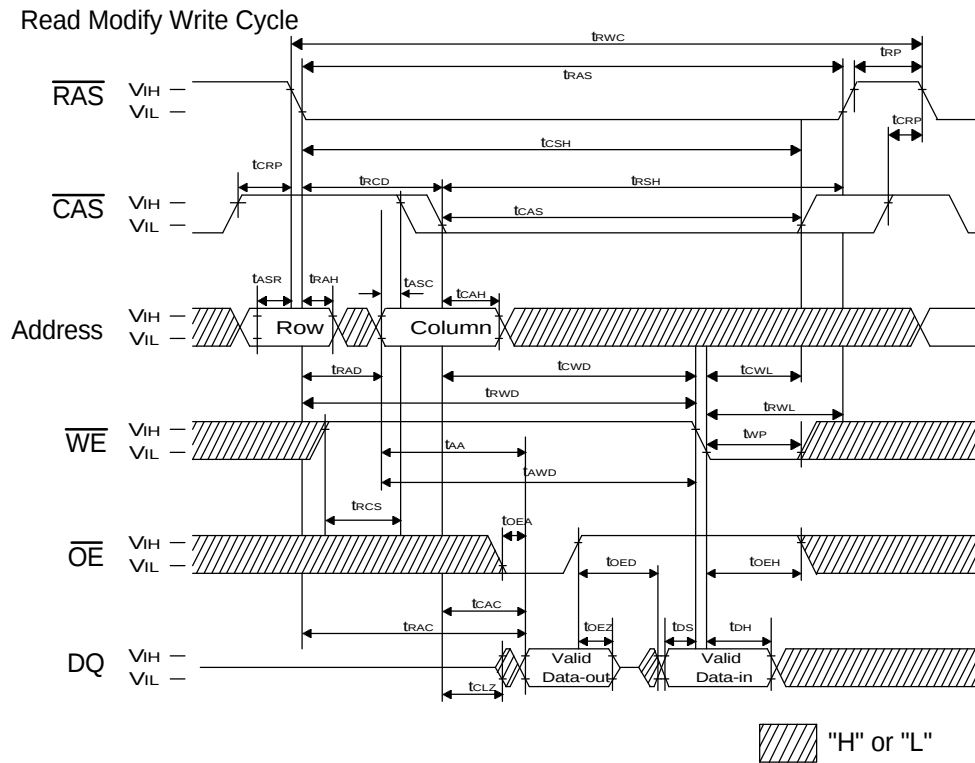


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to the specified value in this data sheet.

Read Cycle





Timing diagram for Fast Page Mode Read Cycle (Part 1). The diagram shows the relationship between RAS, CAS, Address, WE, OE, and DQ signals. Key timing parameters include:

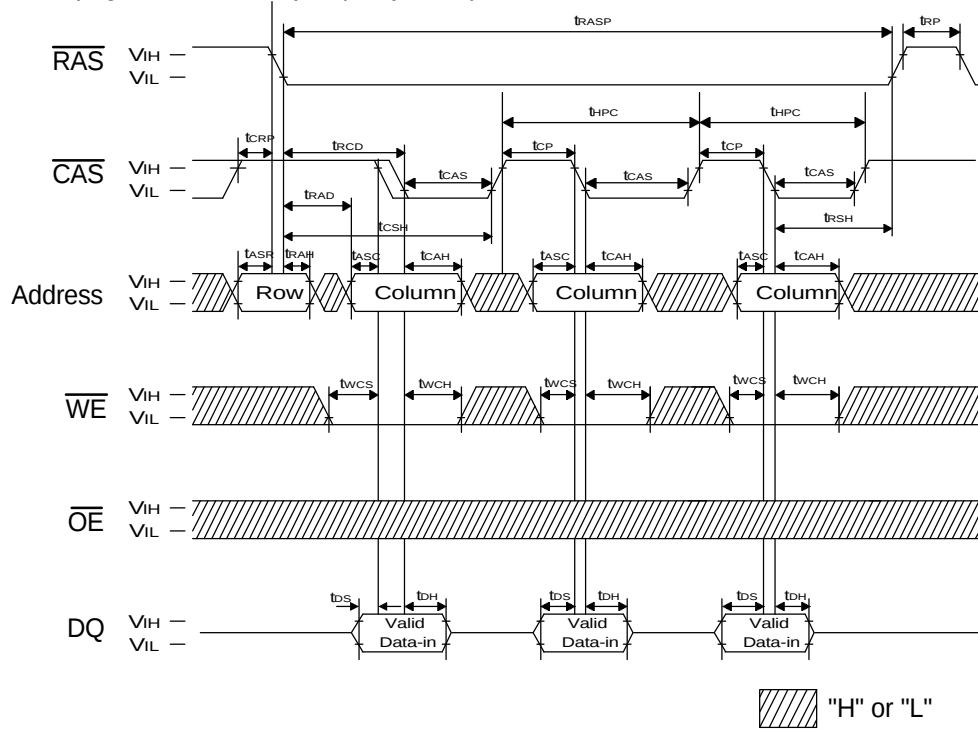
- t_{RAS} : RAS pulse width
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{RCP} : RAS to CAS setup time
- t_{AD} : Address to Data delay
- t_{CSH} : CAS to Address setup time
- t_{ASC} : Address to Column Address delay
- t_{CAH} : Column Address to Data delay
- t_{RCS} : RAS to Column Address delay
- t_{RAC} : RAS to Address delay
- t_{AA} : Address to Address delay
- t_{OEA} : OE to Address delay
- t_{CPA} : Column Address to Address delay
- t_{CAC} : Column Address to Address delay
- t_{DOH} : Data Output Hold time
- t_{OEP} : OE to Data Output delay
- t_{OEZ} : OE to Data Output delay
- t_{OEA} : OE to Address delay
- t_{REZ} : Data Output to Address delay
- t_{CLV} : Data Output to Address delay
- t_{RRH} : RAS to Address delay

Legend: Hatched area indicates "H" or "L" level.

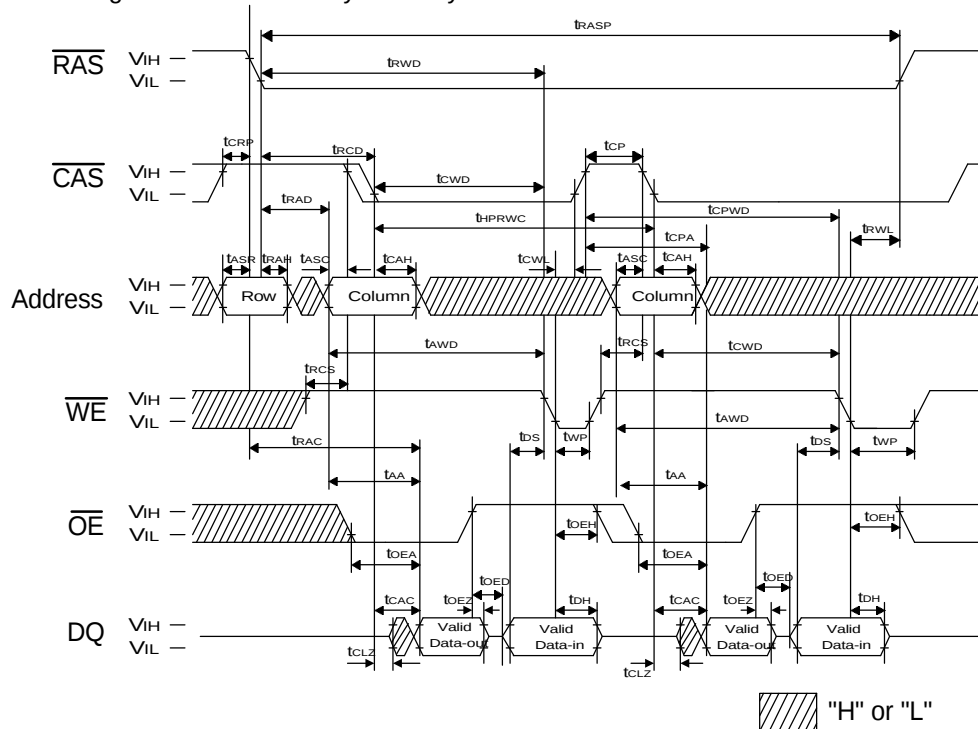
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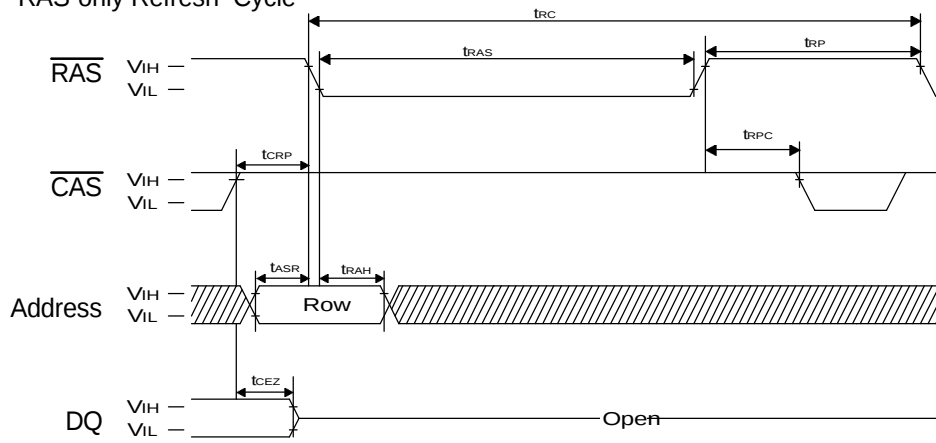
Fast page Mode Write Cycle(Early Write)



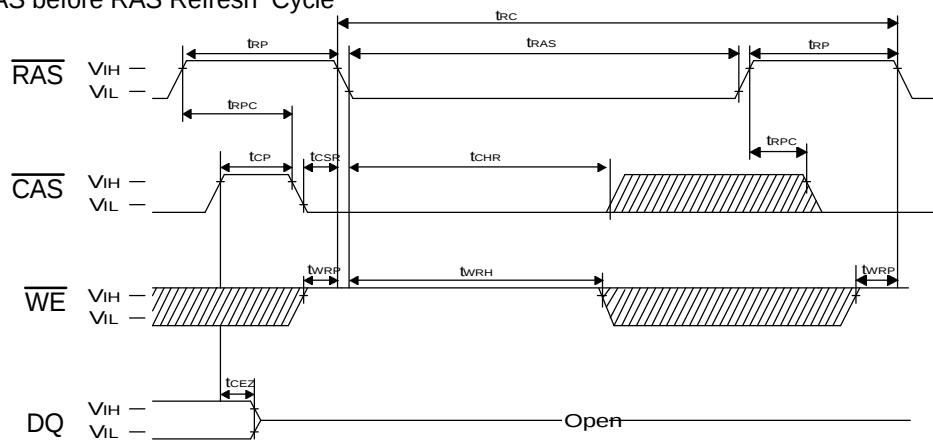
Fast Page Mode Read Modify Write Cycle



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 $\overline{\text{RAS}}$ -only Refresh CycleNote: $\overline{\text{WE}}, \overline{\text{OE}} = \text{"H" or "L"}$

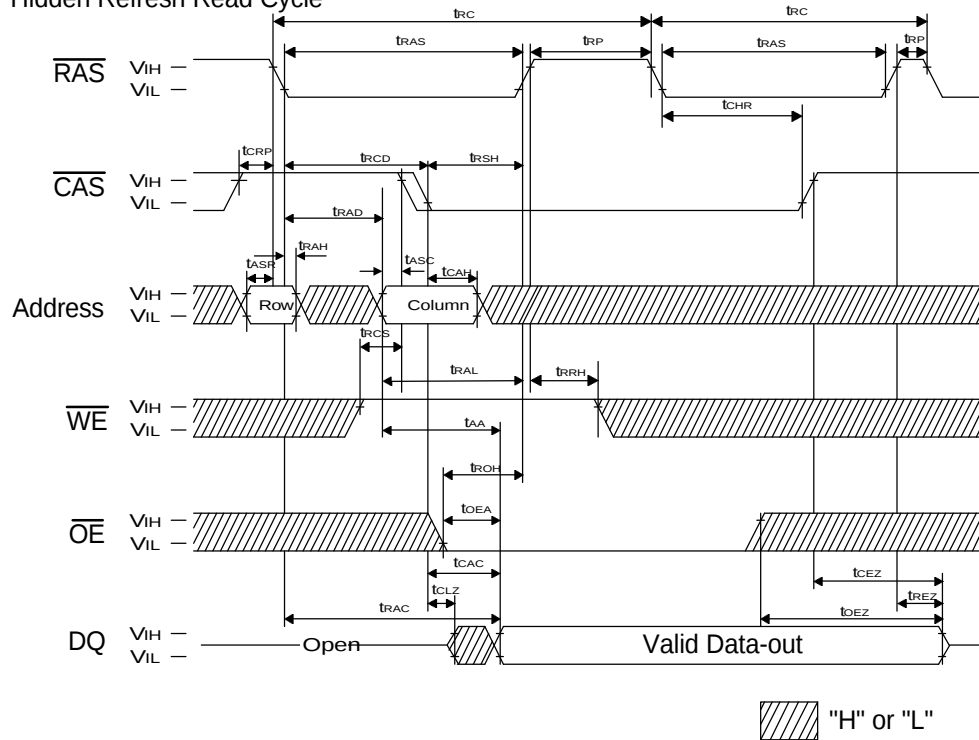
"H" or "L"

 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh CycleNote: $\overline{\text{OE}}, \text{Address} = \text{"H" or "L"}$

"H" or "L"

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Hidden Refresh Read Cycle



Hidden Refresh Write Cycle

