MIC4608

600V Half Bridge MOSFET or IGBT Driver

General Description

The MIC4608 is a 600V Half Bridge IGBT or MOSFET driver. The MIC4608 features a 450ns propagation delay including a 200ns input filtering time to prevent unwanted pulses. The low-side and high-side gate drivers are independently controlled (with shoot thru protection) or controlled with a single PWM signal. The MIC4608 has TTL input thresholds.

The robust operation of the MIC4608 ensures that the outputs are not affected by supply glitches, HS ringing below ground, or HS slewing with high-speed voltage transitions. Undervoltage protection is provided on both the low-side and high-side drivers.

The MIC4608 is available in a 14-pin SOIC package. The MIC4608 has an operating junction temperature range of –40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

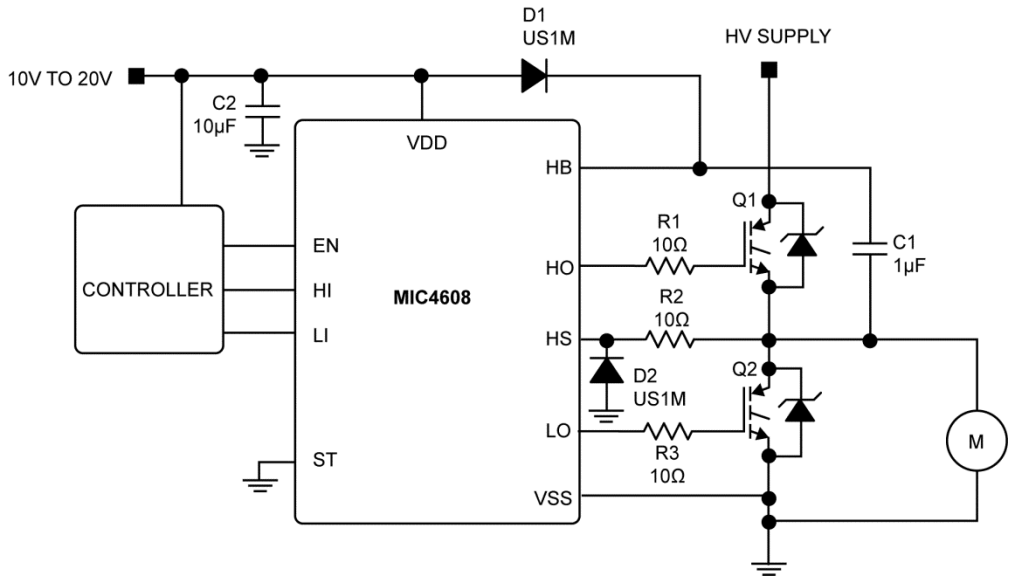
Features

- Gate drive supply voltage up to 20V
- Drives high-side and low-side N-Channel MOSFETs or IGBTs with independent inputs or with a single PWM signal
- ±50V/ns dV/dt immunity
- TTL input thresholds
- 200ns input filtering time
- Shoot thru protection
- Low power consumption
- Supply undervoltage protection
- –40°C to +125°C junction temperature range

Applications

- Full- and half-bridge motor drive
- Industrial controls
- White goods

Typical Application

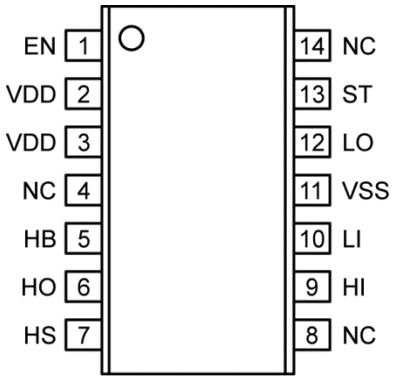


Half–Bridge Motor Driver

Ordering Information

Part Number	Input	Junction Temperature Range	Package
MIC4608YM	TTL	–40°C to +125°C	14-Pin SOIC

Pin Configuration



14-Pin SOIC (M)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	EN	A high level on this pin enables the driver. A low level disables the drivers and places the part in a low quiescent current state. This pin has an internal 300kΩ pull-down resistor to V_{SS}.
2	VDD	Input supply for gate drivers. Decouple this pin to VSS with a >2.2µF capacitor. Bootstrap diode connected to HB.
3	VDD	Input supply for gate drivers. Connect directly to pin 2.
4	NC	No connection.
5	HB	High-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and HS. An external bootstrap diode is connected to this pin as well.
6	HO	High-side drive output. Connect to gate of the external low-side power MOSFET or IGBT.
7	HS	High-side drive reference connection. Connect to source/emitter of the external high-side power MOSFET or IGBT. Decouple this pin with the bootstrap capacitor to HB.
8	NC	No connection
9	HI	High-side drive input and PWM input for single signal drive. This pin has an internal 300kΩ pull-down resistor to VSS.
10	LI	Low-side drive input. This pin has an internal 300kΩ pull-down resistor to VSS.
11	VSS	Driver Reference supply input. Generally connected to power ground of external circuitry.
12	LO	Low-side drive output. Connect to gate of the external low-side power MOSFET or IGBT.
13	ST	State pin. PWM or Independent drive. Logic low allows for independent operation and logic high allows for single input PWM drive operation. This pin has an internal 300kΩ pull-down resistor to VSS.
14	NC	No connection.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}, V_{HB} – V_{HS}) ..... –0.3V to 25V
Input Voltages (V_{LI}, V_{HI}, V_{ST}, V_{EN})..... –0.3V to V_{DD} +0.3V
Voltage on LO (V_{LO}) ..... –0.3V to V_{DD} + 0.3V
Voltage on HO (V_{HO}) ..... V_{HS} –0.3V to V_{HB} + 0.3V
Voltage on HS (continuous) ..... –25V to +630V
Voltage on HB ..... +655V
HS Slew Rate 50V/ns
Storage Temperature (T_S) ..... –60°C to +150°C
ESD Rating[3]
HBM 1.5kV
MM 150V

Operating Ratings[2]

Supply Voltage (V_{DD}) ..... 10V to 20V
Input Voltages (V_{LI}, V_{HI}, V_{ST}, V_{EN}) ..... 0V to V_{DD}
Voltage on HS (repetitive transient) .....5V–V_{DD} to 600V
Voltage on HB ..... V_{HS} +10V to V_{HS} +20V
and/or..... V_{DD} –1V to V_{DD} +600V
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
14-Pin SOIC (θ_{JA}) ..... 105°C/W

Electrical Characteristics[3][4]

V_{DD} = V_{HB} = 20V; V_{SS} = V_{HS} = 0V; V_{ST} = 0V; No load on LO or HO; T_A = 25°C, unless noted. **Bold** values indicate –40°C≤ T_J ≤ +125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current						
I_{DD}	V_{DD} Quiescent Current	V_{HI} = V_{LI} = 0V		42	**100**	µA
I_{DDSH}	V_{DD} Shutdown Current	V_{EN} = 0V, HS = floating		0.1	**1**	µA
		V_{EN} = 0V, V_{HS} = 0V		0.1	**1**	
I_{DDO}	V_{DD} Operating Current	f = 20kHz		150	**350**	µA
I_{HB}	Total HB Quiescent Current	V_{LI} = V_{HI} = 0V or V_{LI} = 0V and V_{HI} = 10V		35	**100**	µA
I_{HBO}	Total HB Operating Current	f = 20kHz		210	**400**	µA
Input (TTL: LI and HI)						
V_{IL}	Low-Level Input Voltage				**0.8**	V
V_{IH}	High-Level Input Voltage		**2.2**			V
V_{HYS}	Input Voltage Hysteresis			0.2		V
I_{HI_LI}	Input Current	V_{LI} = V_{HI} = 20V		57		µA
R_I	Input Pull-Down Resistance			300		kΩ
Input (TTL: EN and ST)						
V_{IL}	Low-Level Input Voltage				**0.8**	V
V_{IH}	High-Level Input Voltage		**2.2**			V
V_{HYS}	Input Voltage Hysteresis			0.2		V
I_{HI_LI}	Pin Current	V_{LI} = V_{HI} = 20V		57		µA
R_I	Input Pull-Down Resistance			300		kΩ

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
4. Specification for packaged product only.

Electrical Characteristics[3][4] (Continued)

V_{DD} = V_{HB} = 20V; V_{SS} = V_{HS} = 0V; V_{ST} = 0V; No load on LO or HO; T_A = 25°C, unless noted. **Bold** values indicate –40°C≤ T_J ≤ +125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Undervoltage Protection						
V_{DDR}	V_{DD} Falling Threshold		**7.0**	8.5	**9.6**	V
	V_{DD} Rising Threshold			**9.0**		V
V_{DDH}	V_{DD} Threshold Hysteresis			0.5		V
V_{HBR}	HB Falling Threshold		**7.0**	8.0	**9.0**	V
	HB Rising Threshold			**8.5**		V
V_{HBH}	HB Threshold Hysteresis			0.5		V
LO Gate Driver						
V_{OLL}	Low-Level Output Voltage	I_{LO} = 50mA		0.46	**0.9**	V
V_{OHL}	High-Level Output Voltage	I_{LO} = –50mA, V_{OHL} = V_{DD} - V_{LO}		0.46	**0.9**	V
I_{OHL}	Peak Sink Current	V_{LO} = 0V		1		A
I_{OLL}	Peak Source Current			1		A
HO Gate Driver						
V_{OLH}	Low-Level Output Voltage	I_{HO} = 50mA		0.4	**0.9**	V
V_{OHH}	High-Level Output Voltage	I_{HO} = –50mA, V_{OHH} = V_{HB} – V_{HO}		0.4	**0.9**	V
I_{OHH}	Peak Sink Current	V_{HO} = 0V		1		A
I_{OLH}	Peak Source Current			1		A
Switching Specifications ($V_{LI/HI}$ high level=10V; C_{LOAD} on HO/LO = 1.15nF)						
fs	Switching Frequency Range			25		kHz
$t_{HI_LI_OL}$	Overlap Timing Between LI/HI			20		ns
t_{ON}	Turn-On Propagation Delay	V_{ST} = 0V; LI to LO or HI to HO	300	450	600	ns
t_{OFF}	Turn-Off Propagation Delay	V_{ST} = 0V; LI to LO or HI to HO	300	450	600	ns
t_{ON}	HO Turn-On Propagation Delay	V_{ST} = 20V; HI Rising to HO Rising	520	850	1020	ns
t_{ON}	LO Turn-On Propagation Delay	V_{ST} = 20V; HI Falling to LO Rising	520	750	1020	ns
t_{OFF}	HO Turn-Off Propagation Delay	V_{ST} = 20V; HI Falling to HO Falling	300	450	600	ns
t_{OFF}	LO Turn-Off Propagation Delay	V_{ST} = 20V; HI Rising to LO Falling	400	615	1020	ns
t_{EN_RISE}	Enable Turn-On Prop Delay	EN to HO or LO		2800		ns
t_{EN_FALL}	Enable Turn-Off Prop Delay	EN to HO or LO		600		ns
t_R	Turn-On Rise Time			31	60	ns
t_F	Turn-Off Fall Time			31	60	ns
t_{FLTR}	Input Filtering Time	LI, HI, EN, ST pins	160	200	320	ns
t_D	Dead Time		220	300	420	ns
t_{PW}	Minimum Input Pulse Width that Changes the Output	Note 5		350		ns

Note:

5. Guaranteed by design. Not production tested.

Timing Diagram

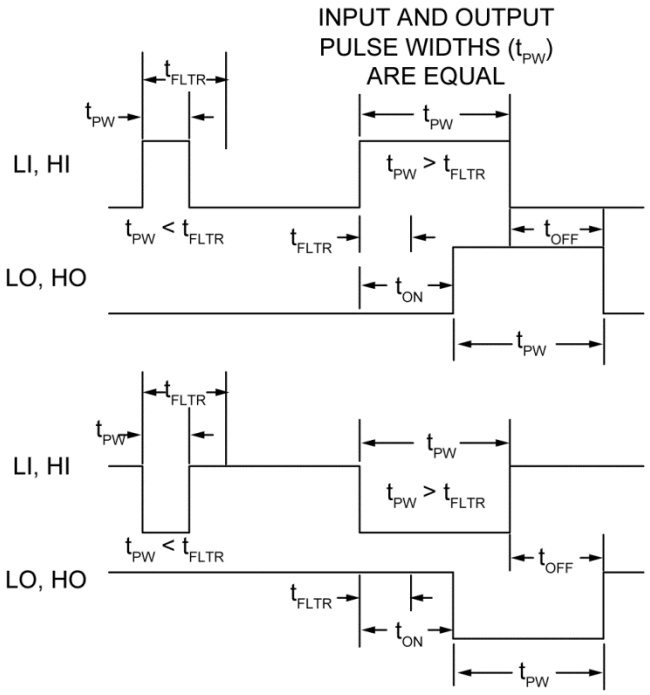


Figure 1. Minimum Pulse Width diagram

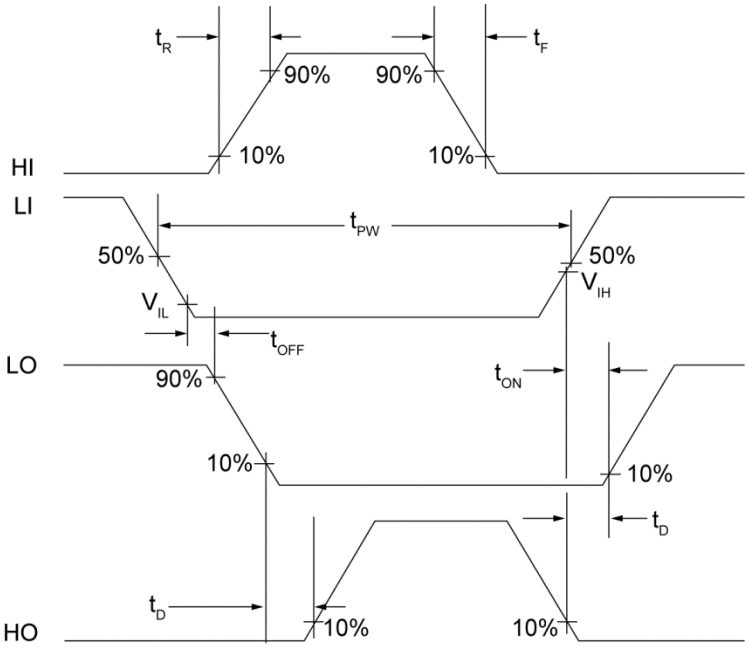
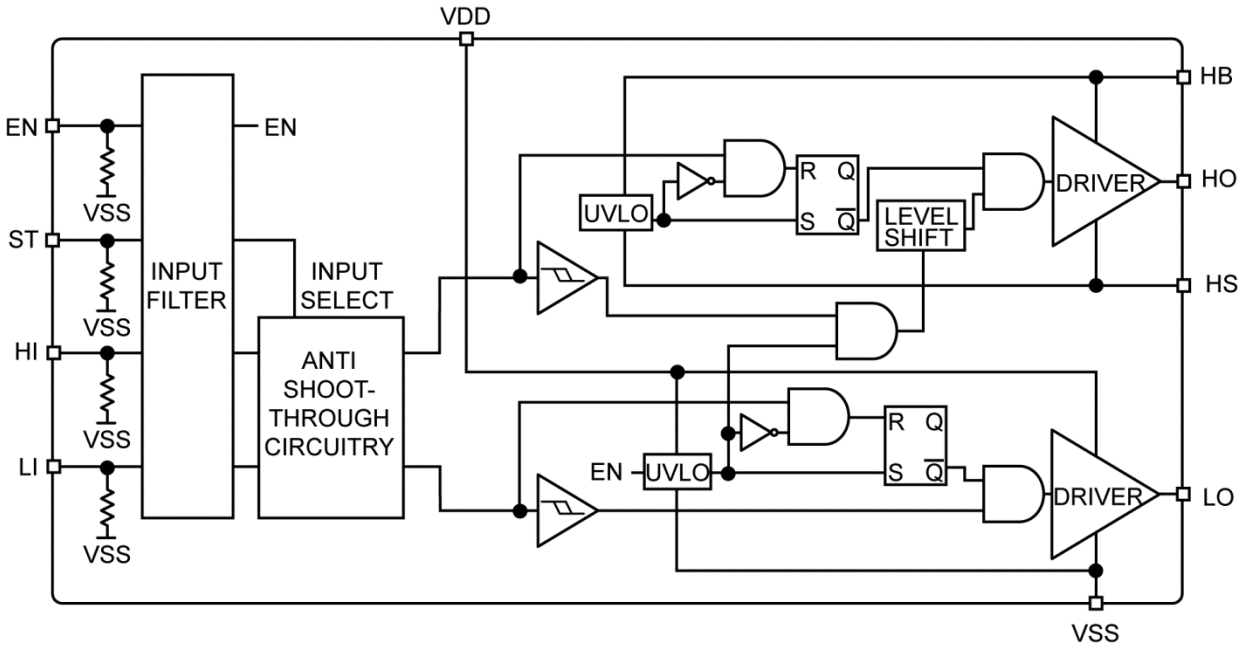


Figure 2. Dead Time, Propagation Delay and Rise/Fall Time Diagram

Functional Diagram



Operational Truth Table

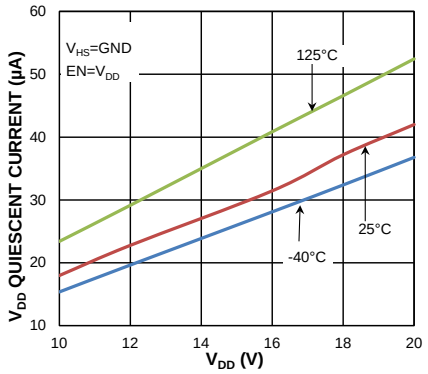
	Inputs				ULVO[6, 7]		Outputs[8, 9]	
Condition	**ST**	**HI**	**LI**	**EN**	**HB UVLO**	**VDD UVLO**	**HO**	**LO**
Disabled	X	X	X	L	X	X	L	L
VDD UVLO	X	X	X	X	X	L	L	L
VHB UVLO	L	X	L or H	H	L	H	L	L or H
VHB UVLO	H	H or L	X	H	L	H	L	L or H
Switching	L	H	H	⌐¬	H	H	L	L
	L	H	H	H	⌐¬	⌐¬	L	L
	L	L	H	H	H	H	L	H
	L	H	L	H	H	H	H	L
	L	H	⌐¬	H	H	H	H	L[10]
	L	⌐¬	H	H	H	H	L	H
	H	H	X	⌐¬	H	H	H[10]	L
	H	H	X	H	⌐¬	⌐¬	H	L
	H	L	X	H	H	H	L	H
	H	H	X	H	H	H	H	L

Note:

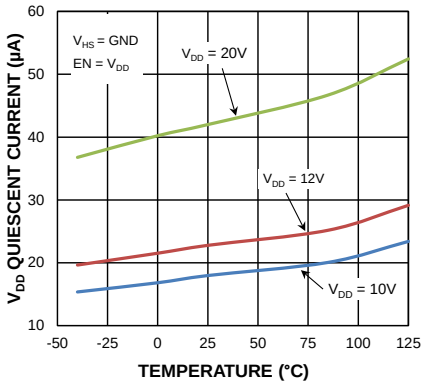
6. UVLO = H when VDD > UVLO Threshold.
7. UVLO = L when VDD < UVLO Threshold.
8. HO and LO remain low if both HI and LI are High when VDD rises above the UVLO threshold or when the EN pin is asserted high. Normal switching operation begins when one of the inputs changes state from H to L.
9. Anti-shoot-through circuit prevents a high on both outputs simultaneously.
10. Output remains low until the other output transitions from high to low, then the output goes high.

Typical Characteristics

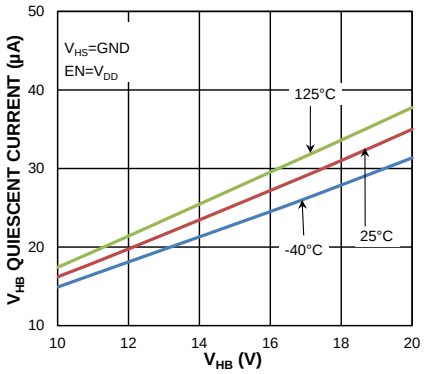
V_{DD} Quiescent Current vs. V_{DD} Voltage



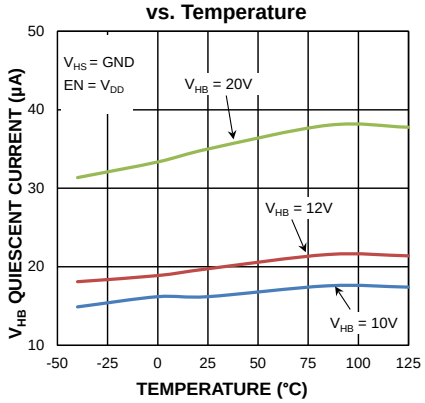
V_{DD} Quiescent Current vs. Temperature



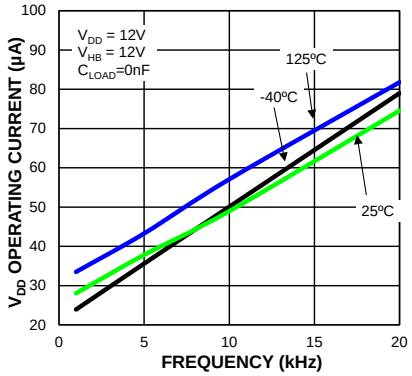
V_{HB} Quiescent Current vs. V_{HB} Voltage



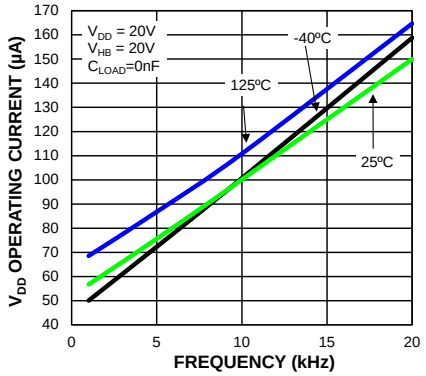
V_{HB} Quiescent Current vs. Temperature



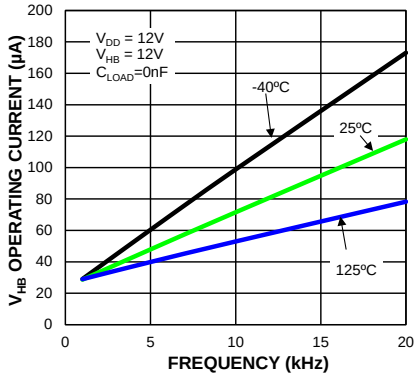
V_{DD} Operating Current vs. Frequency



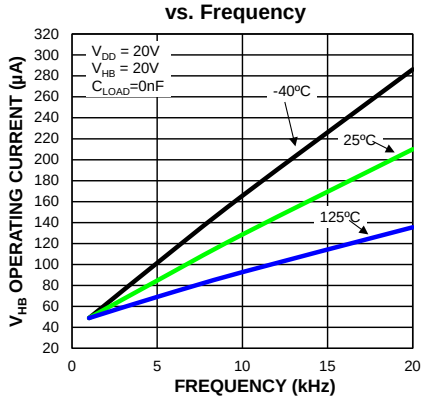
V_{DD} Operating Current vs. Frequency



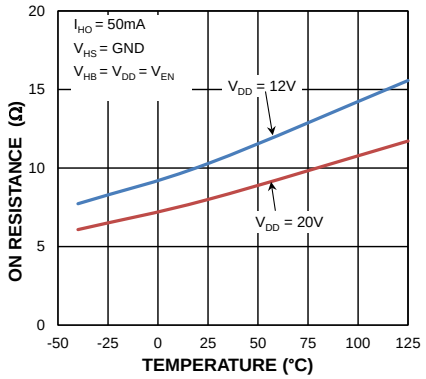
V_{HB} Operating Current vs. Frequency



V_{HB} Operating Current vs. Frequency

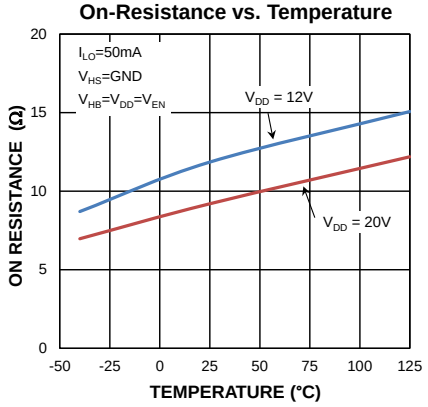


HO Output Sink/Source On-Resistance vs. Temperature

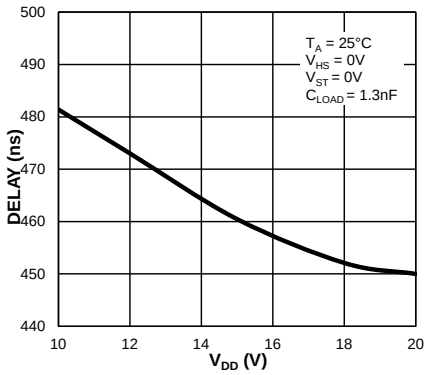


Typical Characteristics (Continued)

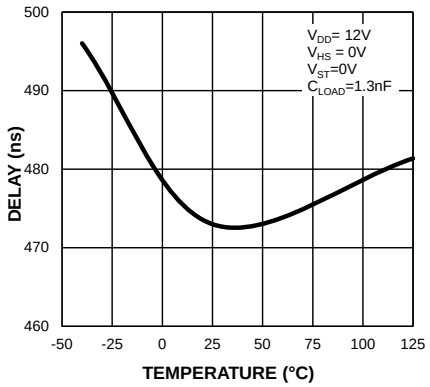
LO Output Sink/Source On-Resistance vs. Temperature



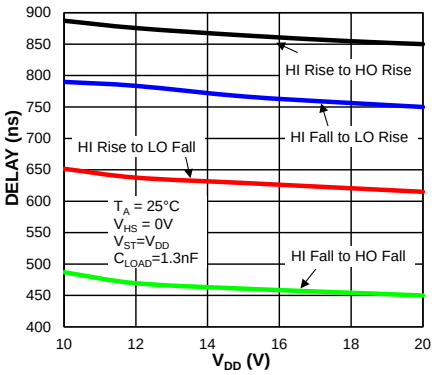
Input to Output Propagation Delay (ST = Low) vs. V_{DD} Voltage



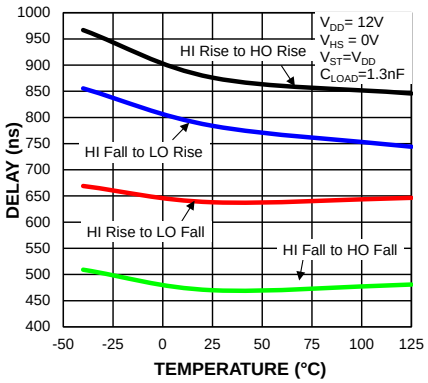
Input to Output Propagation Delay (ST=Low) vs. Temperature



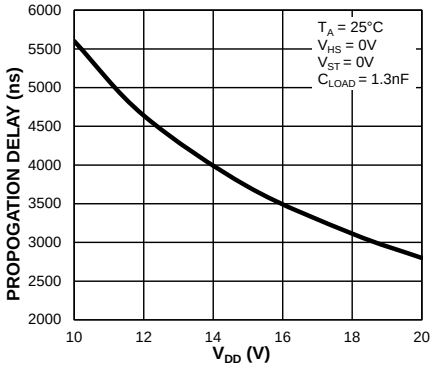
Input to Output Propagation Delay (ST=High) vs. V_{DD} Voltage



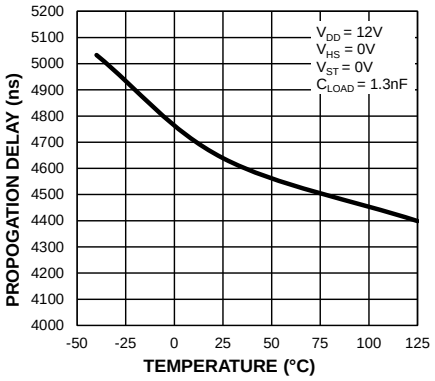
Input to Output Propagation Delay (ST=High) vs. Temperature



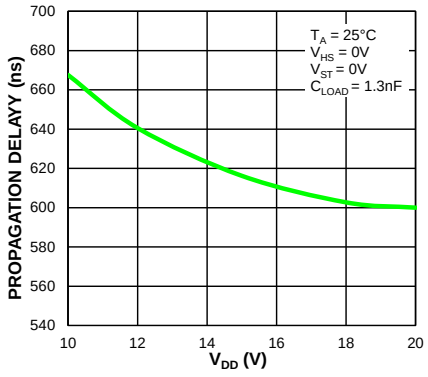
Enable Turn-On Propagation Delay vs. V_{DD}



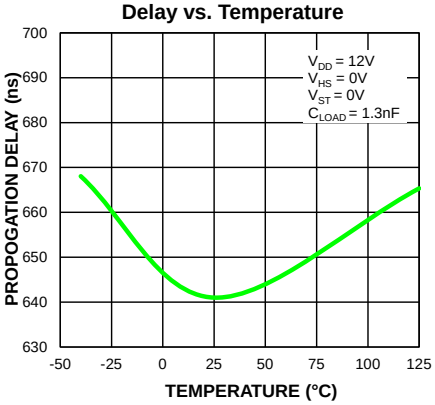
EN Turn-On Propagation Delay vs. Temperature



Enable Turn-Off Propagation Delay vs. V_{DD}

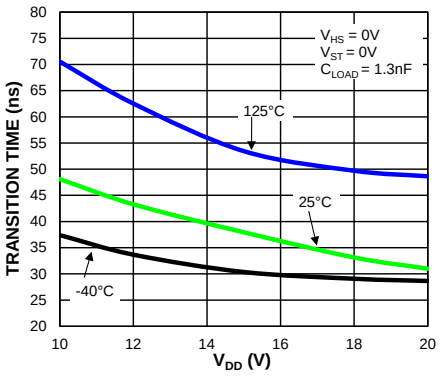


Enable Turn-Off Propagation Delay vs. Temperature

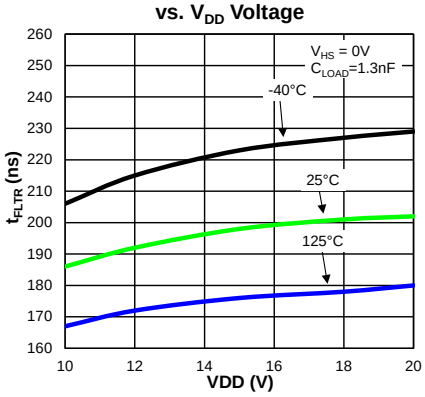


Typical Characteristics (Continued)

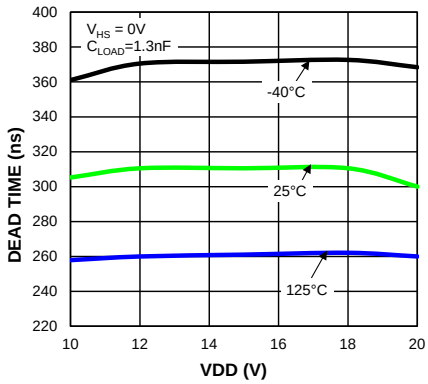
HO/LO Rise Time and Fall Time



Input Filter Time vs. V_{DD} Voltage



Dead Time vs. V_{DD} Voltage



Functional Description

The MIC4608 is a 600V half-bridge driver designed to drive both high-side and low-side IGBTs or MOSFETs. Minimum input pulse width filters and anti-shoot-through logic circuitry improve the driver's noise immunity. A STATE pin allows either a single input or two independent inputs to control both FETs.

Startup and UVLO Circuitry

The VDD pins supply power directly to the low-side gate driver and to the high-side driver through an external bootstrap diode. VDD also supplies power to the internal logic and control circuitry.

The high-side and low-side drivers each have a separate UVLO circuit that force the driver output low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuit monitors the voltage between the HB and HS pins. Hysteresis in the UVLO circuits prevents noise and finite circuit impedance from causing chatter during turn-on.

State Pin (ST)

The state pin configures the driver for single (PWM) input or independent (HI/LI) input operation. Setting the ST pin low allows the HO and LO outputs to be independently controlled by the HI and LI pins, respectively. Setting the ST pin high will disable the LI input. The HO and LO pins are controlled by the HI pin. The dead time is automatically added between the HO and LO outputs in this mode.

In either mode, the internal anti-shoot-through circuitry prevents overlap of the HO and LO signals. An internal pull-down resistor is connected from the ST pin to VSS.

Enable Pin (EN)

Setting the EN pin low puts the device into a low I_Q state and turns off both the LO and HO outputs. A high level on the EN pin turns on the internal bias in the driver and allows the driver to operate normally. An internal pull-down resistor is connected from the EN pin to VSS.

Input Stage

The HI and LI pins are referenced to the VSS pin and have a CMOS/TTL compatible input range. The input threshold voltage is independent of the V_{DD} supply. The input voltage must not exceed the VDD pin voltage. The voltage state of the input signal(s) does not change the quiescent current draw of the driver.

The input stage block diagram is shown in Figure 3.

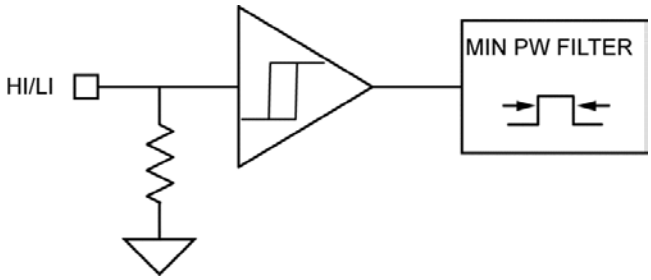


Figure 3. Input Stage

An internal pull-down resistor is connected to the HI and LI pins. This keeps the driver output pins low if the inputs are disconnected or left floating. A small amount of hysteresis is programmed into the input to prevent false triggering of the output. In addition, there is a minimum pulse width filter on the HI and LI inputs for additional noise immunity protection. The input pulse width must exceed the T_{FLTR} time before the outputs will change state. Refer to the Electrical Characteristics table and Figure 1 for additional information.

Low-Side Driver

The low-side driver is designed to drive a ground (VSS pin) referenced N-channel MOSFET or IGBT. Low driver impedances allow the external IGBT to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low R_{DSON} from the external power device. Refer to the low-side driver block diagram in the Functional Diagram section for further details.

When driving the external IGBT on, the driver's P-channel MOSFFET is turned on and V_{DD} is applied to the external IGBT's gate. To turn off the external IGBT, the driver's N-channel FET is turned on, which will discharge the external IGBT's gate to ground.

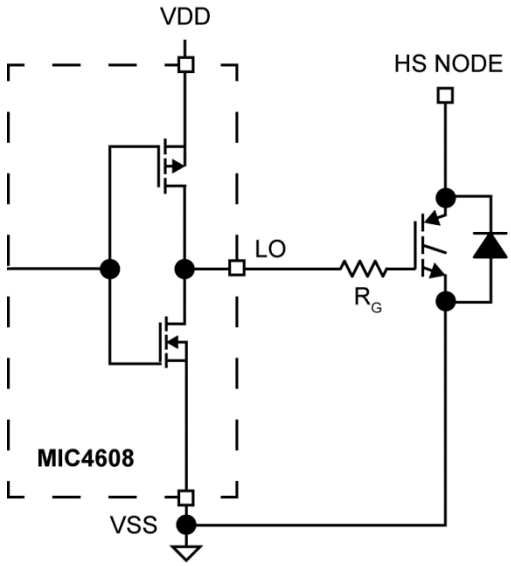


Figure 4. Low-Side Block Diagram

High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in Figure 5. This driver is designed to drive a floating N-channel FET or IGBT, whose source/emitter terminal is referenced to the HS pin.

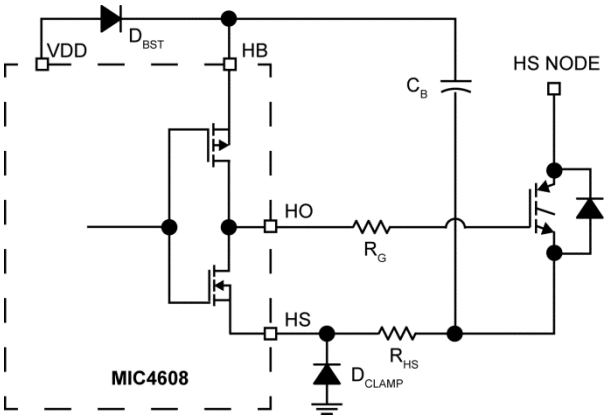


Figure 5. High-Side Driver and Bootstrap Circuit Block Diagram

A low-power, high-speed, level-shifting circuit isolates the low side (VSS pin) referenced circuitry from the high-side (HS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap circuit while the voltage level of the HS pin is shifted high.

The bootstrap circuit consists of an external diode and capacitor, C_B. In a typical application, such as the motor drive circuit shown in Figure 6, the HS pin is at ground potential while the low-side IGBT is on. The diode allows capacitor C_B to charge up to V_{DD}-V_F during this time (where V_F is the diode's forward voltage drop). When the high-side IGBT is ready to turn on, the voltage across capacitor C_B is applied to the IGBT's gate. As the upper IGBT turns on, voltage on the HS pin rises with the emitter of the high-side IGBT until it reaches V_{IN}. As the HS and HB pins rise, the internal diode is reverse biased preventing capacitor C_B from discharging.

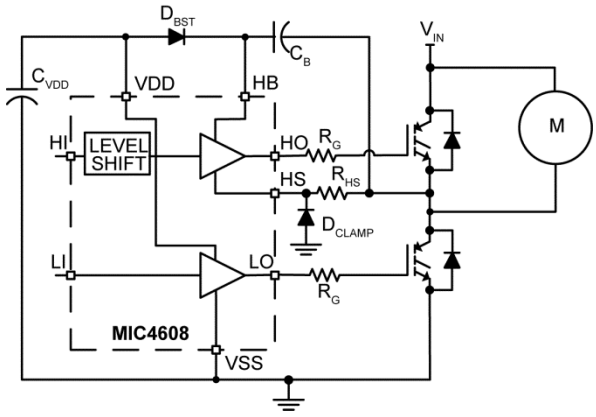


Figure 6. MIC4608 Driving a Motor

Application Information

Bootstrap Circuit

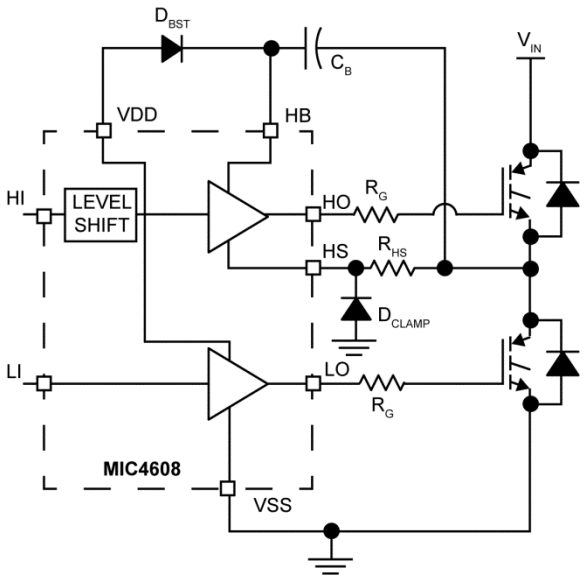


Figure 7. Bootstrap Circuit

Figure 7 shows the bootstrap circuit, where the capacitor voltage drops each time it delivers charge to turn on the IGBT. The voltage drop depends on the gate charge required by the IGBT. Most IGBT and MOSFET specifications contain a gate charge versus V_{GE} or V_{GS} voltage information or graphs. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

$$C_B \geq \frac{Q_{gate}}{\Delta V_{HB}} \qquad \text{Eq. 1}$$

Where:
Q_{gate} = total gate charge at V_{HB}
ΔV_{HB} = voltage drop at the HB pin

The decoupling capacitor for the VDD input may be calculated in with the same formula; however, the two capacitors are usually equal in value.

HS Node Clamp

A resistor/diode clamp between the switching node and the HS pin is recommended to minimize large negative glitches or pulses on the HS pin.

Figure 8 shows the high-side and low-side IGBTs in on and off mode, which regulate the speed of the motor. There is a brief period of time (dead time) between switching to prevent both IGBTs from being on at the same time. When the high-side IGBT is conducting during the on-time state, current flows into the motor. After the high-side IGBT turns off, but before the low-side IGBT turns on, current from the motor flows through the diode in parallel with the low-side IGBT. Depending upon the turn-on time of the diode, the motor current, and circuit parasitics, the initial negative voltage on the switch node can be several volts or more. The forward voltage drop of the diode can be several volts, depending on the diode and motor current.

Even though the HS pin is rated for negative voltage, it is good practice to clamp the negative voltage on the HS pin with a resistor and diode to prevent excessive negative voltage from damaging the driver. Depending upon the application and amount of negative voltage on the switch node, a 1A fast recovery diode and minimum 10 ohm resistor are recommended. The diode reverse voltage must be greater than the high-voltage input supply (V_{IN}). Larger values of resistance can be used if necessary.

Adding a series resistor in the switch node limits the peak high-side driver current during turn-off, which affects the switching speed of the high-side driver. The resistor in series with the HO pin may be reduced to help compensate for the extra HS pin resistance.

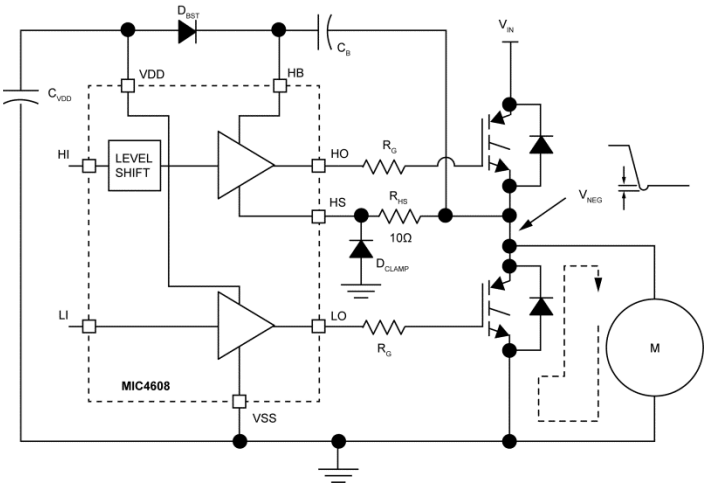


Figure 8. Negative HS Pin Voltage

Power Dissipation Considerations

Power dissipation in the driver can be separated into two areas:

- Gate driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to emitter and gate to collector capacitance of the external IGBT. Figure 9 shows a simplified equivalent circuit of the MIC4608 driving an external high-side IGBT.

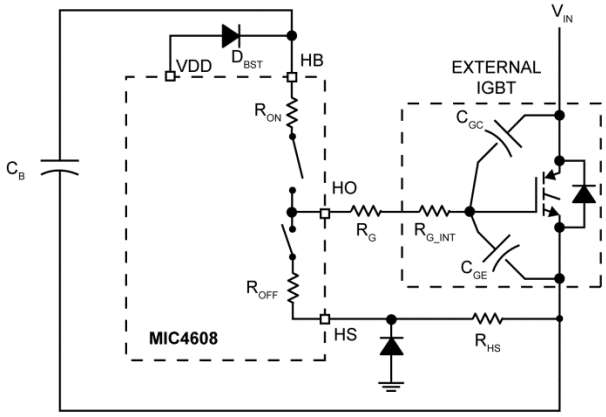


Figure 9. MIC4608 High-Side Driving and External IGBT

Dissipation during External IGBT/MOSFET Turn-On

Energy from capacitor C_B is used to charge up the input capacitance of the IGBT (C_{GE} and C_{GC}). The energy delivered to the gate is dissipated in the three resistive components, R_{ON}, R_G and R_{G_INT}. R_G is the series resistor (if any) between the driver IC and the IGBT. R_{G_INT} is the gate resistance of the IGBT. R_{G_INT} is usually listed in the IGBT or MOSFET specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_INT}.

The effective capacitances of C_{GE} and C_{GC} are difficult to calculate because they vary non-linearly with I_C, V_{GE}, and V_{CE}. Fortunately, most power IGBT and MOSFET specifications include a graph of total gate charge versus V_{GE}. Figure 10 shows a typical gate charge curve for an arbitrary IGBT. This chart shows that for a gate voltage of 12V, the IGBT requires 12nC of charge. The power dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

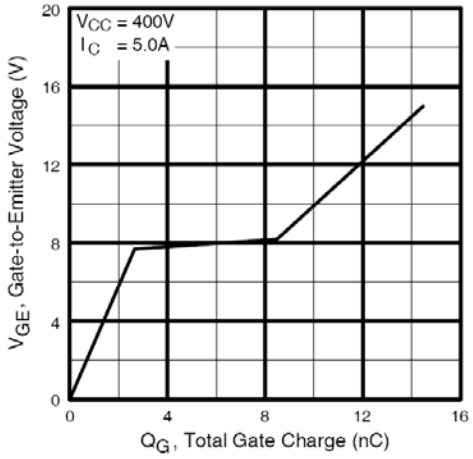


Figure 10. Typical Gate Charge vs. V_{GE}

$$P_{DRIVER} = Q_G \times V_{GE} \times f_S \qquad \text{Eq. 2}$$

Where:

P_{DRIVER} = Average drive circuit power due to switching

Q_G = Total gate charge at V_{GE}

V_{GE} = Gate to emitter voltage on the IGBT

f_S = Switching frequency of the gate drive circuit

The power dissipated by each of the internal gate drivers (high-side or low-side) is equal to the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_INT}. Letting $R_{ON} = R_{OFF}$, the power dissipated in either the high or low driver in the MIC4608 due to driving the external IGBT is:

$$Pdiss_{HS(LS)} = P_{DRIVER} \frac{R_{ON}}{R_{ON} + R_G + R_{G_INT}} \qquad \text{Eq. 3}$$

The total power dissipated is equal to the sum of the high-side and low-side driver dissipations.

Supply Current Power Dissipation

Power is dissipated in the MIC4608 even if nothing is being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The supply current is proportional to operating frequency and the V_{DD} and V_{HB} voltages. The Typical Characteristics graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4608 due to supply current is:

$$Pdiss_{SUPPLY} = V_{DD} \times I_{DD} + V_{HB} \times I_{HB} \qquad \text{Eq. 4}$$

Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4608 is equal to the power dissipation caused by driving the external IGBTs and the supply current.

$$Pdiss_{TOTAL} = Pdiss_{SUPPLY} + Pdiss_{DRIVE(HS)} + Pdiss_{DRIVE(LS)}$$

Eq. 5

The die temperature can be calculated after the total power dissipation is known.

$$T_J = T_A + Pdiss_{TOTAL} \times \theta_{JA}$$

Eq. 6

Where:
T_A = maximum ambient temperature
T_J = junction temperature (°C)
$Pdiss_{TOTAL}$ = power dissipation of the MIC4608
θ_{JA} = thermal resistance from junction to ambient air

Other Timing Considerations

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low side (VDD) and high side (HB) supply pins. These capacitors supply the charge necessary to drive the external IGBTs and MOSFETs and also minimize the voltage ripple on these pins. The capacitor from HB to HS has two functions: it provides decoupling for the high-side circuitry and also provides current to the high-side circuit while the high-side external IGBT/MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1µF is required for each of the capacitors, regardless of the IGBT/MOSFETs being driven. Larger IGBT/MOSFETs and low switching frequencies may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the VDD and VSS pins. The bypass capacitor (C_B) for the HB supply pin must be located as close as possible between the HB and HS pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the section "Grounding, Component Placement and Circuit Layout" for more information.

Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4608 driver requires proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

Figure 11 shows the critical current paths when the driver outputs go high and turn on the external IGBTs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the IGBT gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the IGBT gate, and out the emitter. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the emitter of the IGBT. This voltage works against the gate drive voltage and can either slow down or turn off the IGBT during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the HB pin and out the HO pin, into the gate of the high side IGBT. The return path for the current is from the emitter of the IGBT and back to capacitor C_B. The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the IGBT emitter and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the IGBT.

It is important to note that capacitor C_B must be placed close to the HB and HS pins. This capacitor not only provides all the energy for turn-on but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.

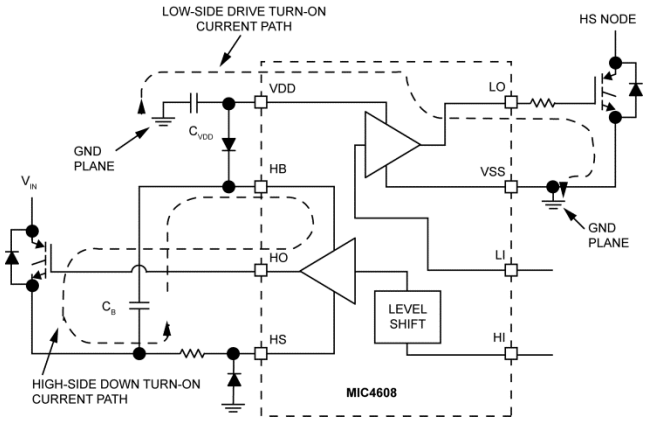


Figure 11. Turn-On Current Paths

Figure 12 shows the critical current paths when the driver outputs go low and turn off the external IGBTs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, CB.

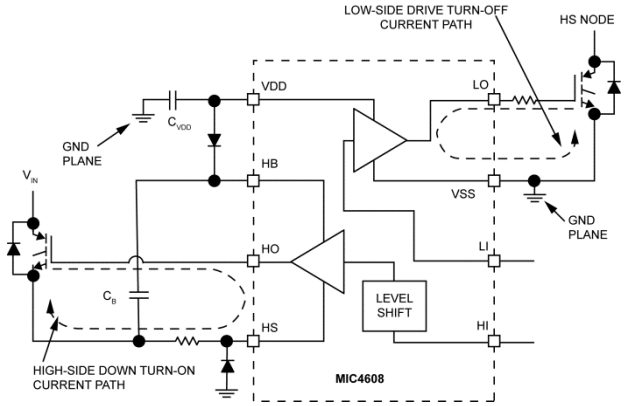
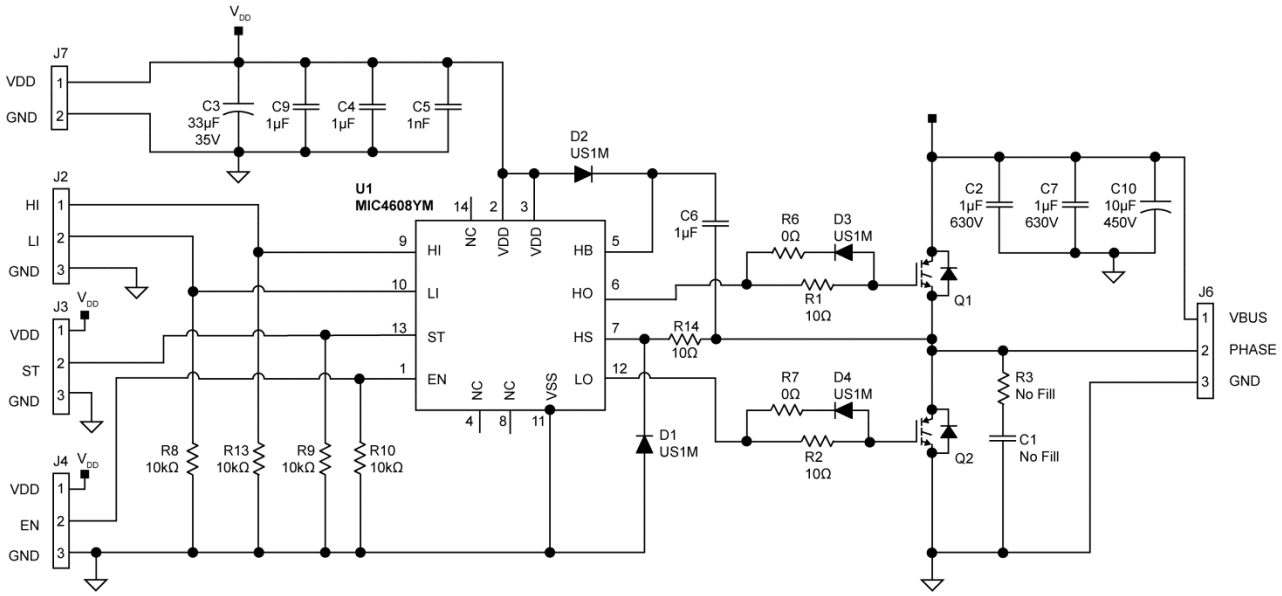


Figure 12. Turn-Off Current Paths

Use the following layout guidelines for optimum circuit performance:

Use a ground plane to minimize parasitic inductance and impedance of the return paths. The MIC4608 is capable of greater than 1A peak currents and any impedance between the MIC4608, the decoupling capacitors, and the external IGBT/MOSFET will degrade the performance of the driver.

Typical Application Schematic



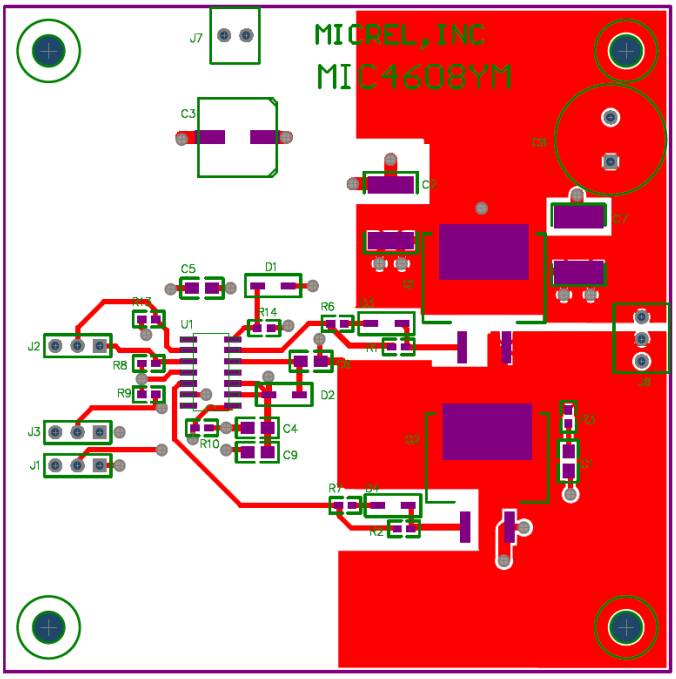
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	No Fill			0
C2, C7	CKG57NX7T2J105M500JH	TDK[11]	1µF, 630V, X7T, Ceramic Capacitor	2
C10	SK100M450ST	Cornell Dubilier[12]	10µF, 450V, Aluminum Electrolytic	1
C3	EEE-FK1V330P	Panasonic[13]	33µF, 35V, Aluminum Electroltyic	1
C4, C6, C9	C2012X7S2A105K125AE	TDK	1µF, 100V, X7S, 0805	3
C5	C2012X7R2A102M085AA	TDK	1nF, 100V, X7R, 0805	1
D1, D2, D3, D4	US1M-E3	Vishay[14]	1A, 1kV, Fast Recovery Diode	4
Q1, Q2	IRG4RC10UDTRLP	IR[15]	IGBT, 600V, 8.5A, DPAK	2
R1, R2, R14	CRCW060310R0FRT1	Vishay Dale	10Ω (0603 size), 1%	4
R3	No Fill			0
R6, R7	CRCW0600000FRT1	Vishay Dale	0Ω (0603 size)	2
R8, R9, R10, R13	CRCW06031002FRT1	Vishay Dale	10kΩ (0603 size), 1%	4
U1	**MIC4608YM**	**Micrel[16]**	**600V Half Bridge MOSFET or IGBT Driver**	**1**

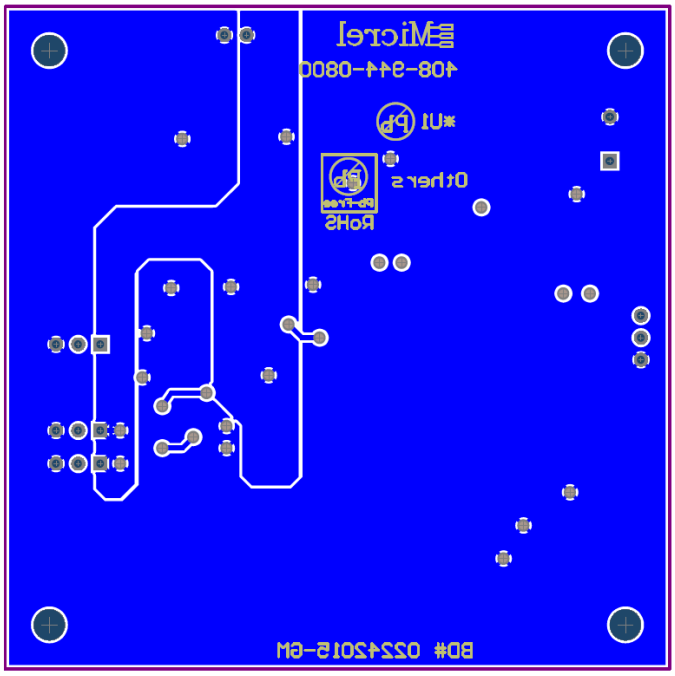
Notes:

11. TDK: www.tdk.com.
12. Cornell Dubilier: www.cde.com.
13. Panasonic: www.panasonic.com.
14. Vishay: www.vishay.com.
15. IR: www.IRF.com.
16. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations



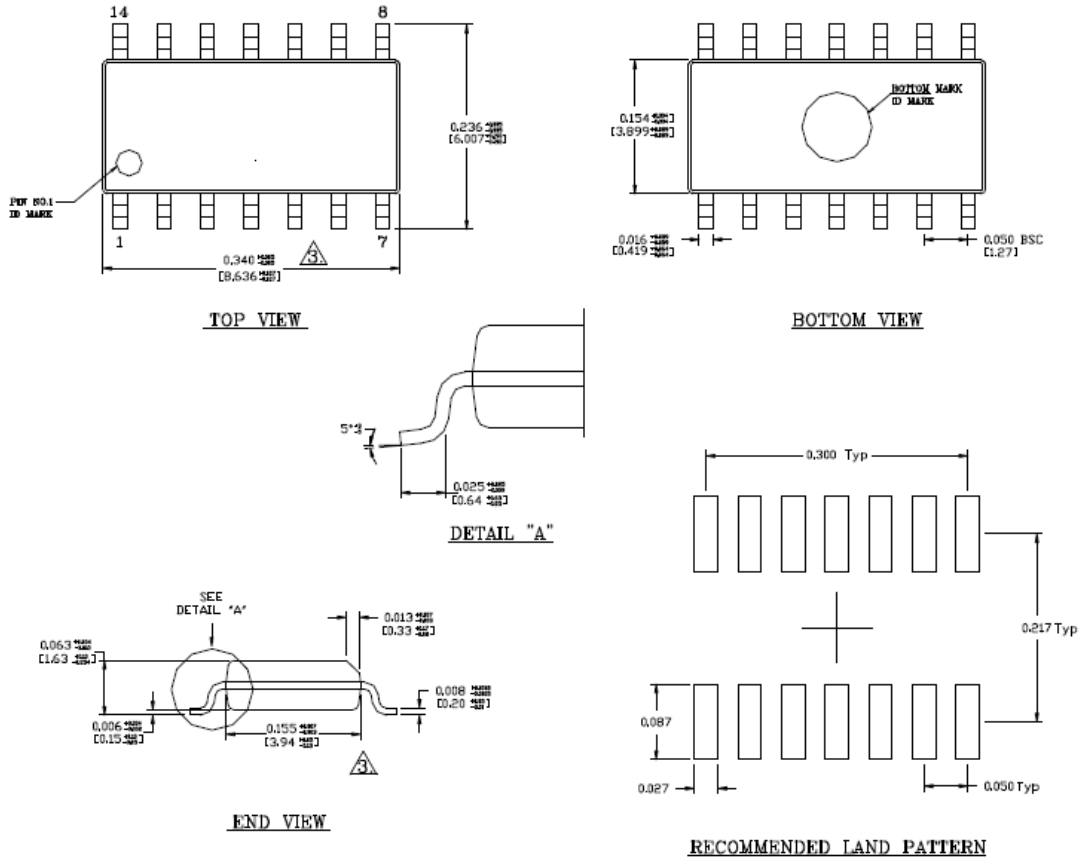
Top Layer



Bottom Layer

Package Information and Recommended Landing Pattern[17]

DRAWING #	SOICN-14LD-PL-1	UNIT	INCH [MM]
Lead Frame	Copper	Lead Finish	Matte Tin



NOTES:
1. DIMENSIONS ARE IN INCHES [MILLIMETER].
2. CONTTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010 [0.25] PER SIDE.

14-Pin SOIC (M)

Note:

17. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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