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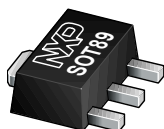
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Kind regards,

Team Nexperia



BSS192

240 V, P-channel vertical D-MOS transistor

12 December 2014

Product data sheet

1. General description

P-channel enhancement mode vertical Double-Diffused Field-Effect Transistor (D-MOSFET) in a SOT89 (SC-62) medium power and flat lead Surface Mounted Device (SMD) plastic package.

2. Features and benefits

- Direct interface to Complementary (C-MOS) transistor and Transistor-Transistor Logic (TTL) devices
- Very fast switching
- No secondary breakdown

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-	-240	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	-200	mA
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -200\text{ mA}; T_j = 25\text{ }^{\circ}\text{C}$		-	10	12	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .

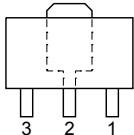
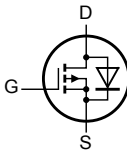


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 SOT89	 017aaa257
2	D	drain		
3	G	gate		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BSS192	SOT89	plastic surface-mounted package; die pad for good heat transfer; 3 leads	SOT89

7. Marking

Table 4. Marking codes

Type number	Marking code
BSS192	KB

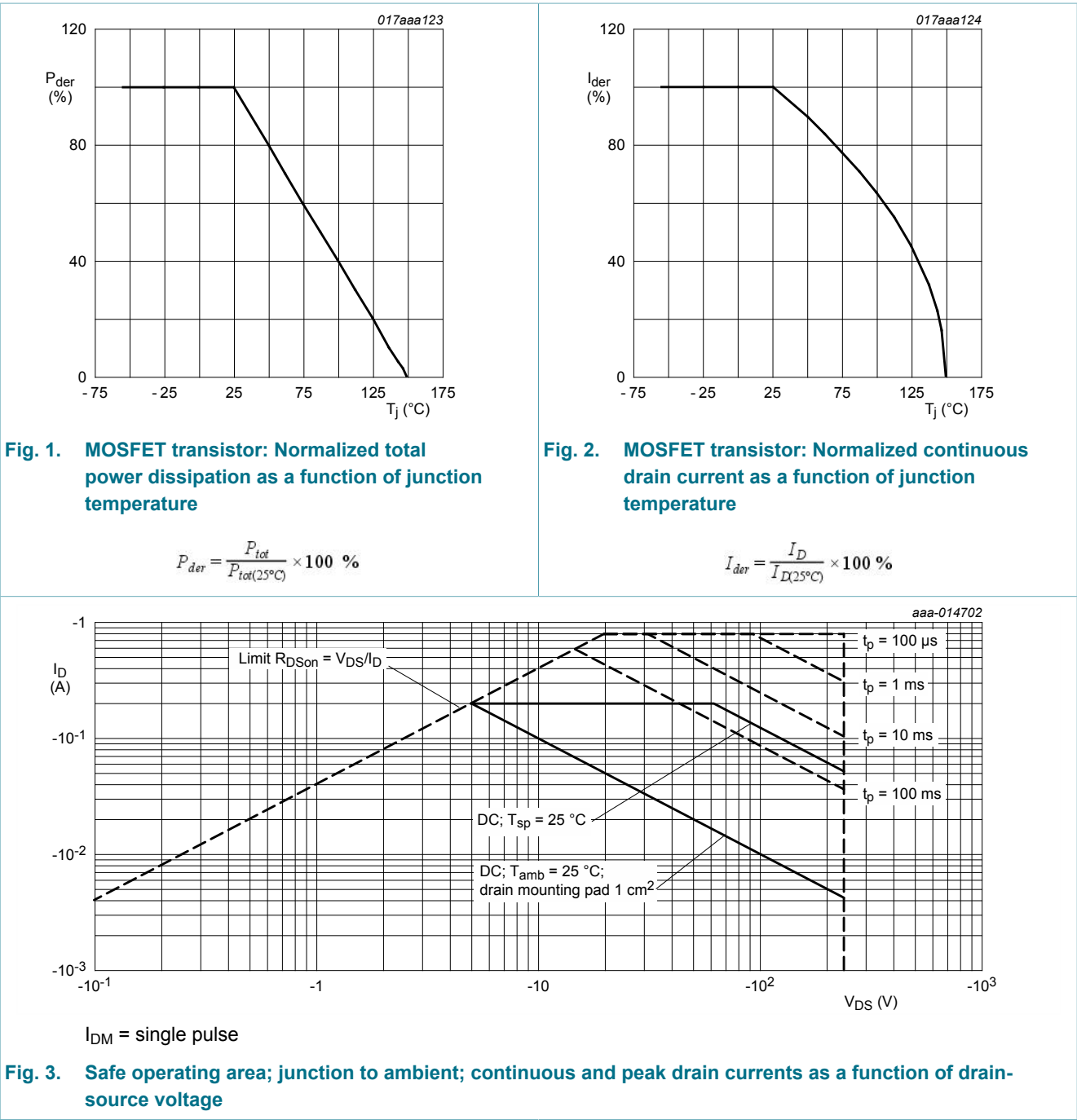
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-240	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	-340	mA
		$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-200	mA
		$V_{GS} = -10\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	-120	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	-800	mA
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	560	mW
			[1]	-	1	W
		$T_{sp} = 25\text{ }^{\circ}\text{C}$		-	12.5	W
T_j	junction temperature			-55	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature			-55	150	$^{\circ}\text{C}$
T_{stg}	storage temperature			-65	150	$^{\circ}\text{C}$
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-200	mA

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	194	225	K/W
			[2]	-	108	125	K/W
		t ≤ 5 s	[2]	-	37	42	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	4	10	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

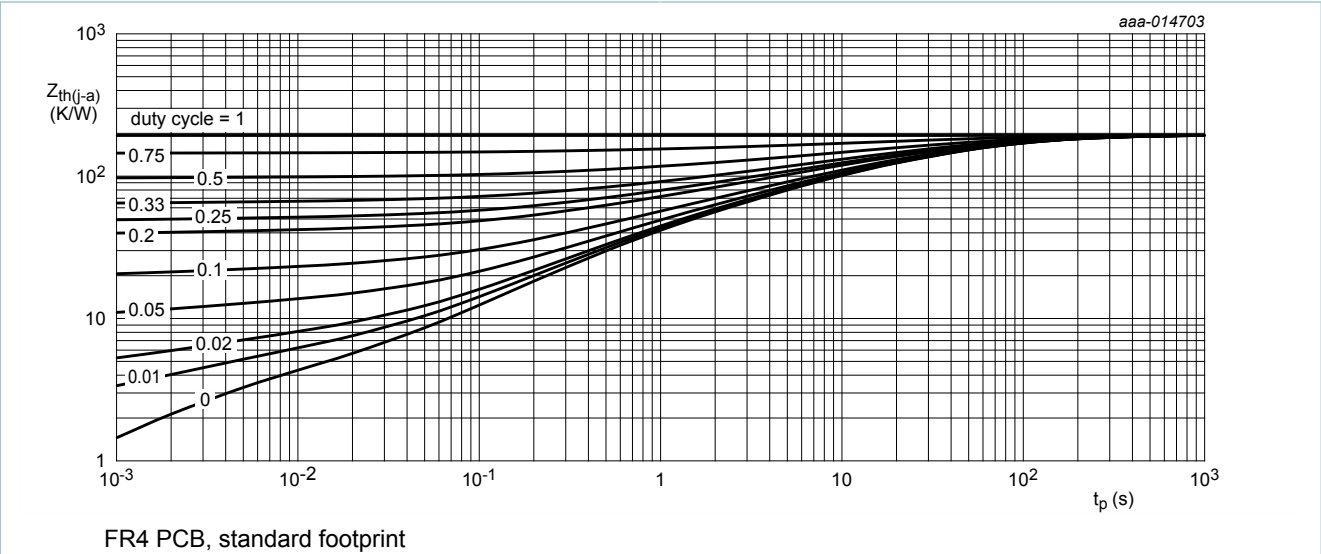


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

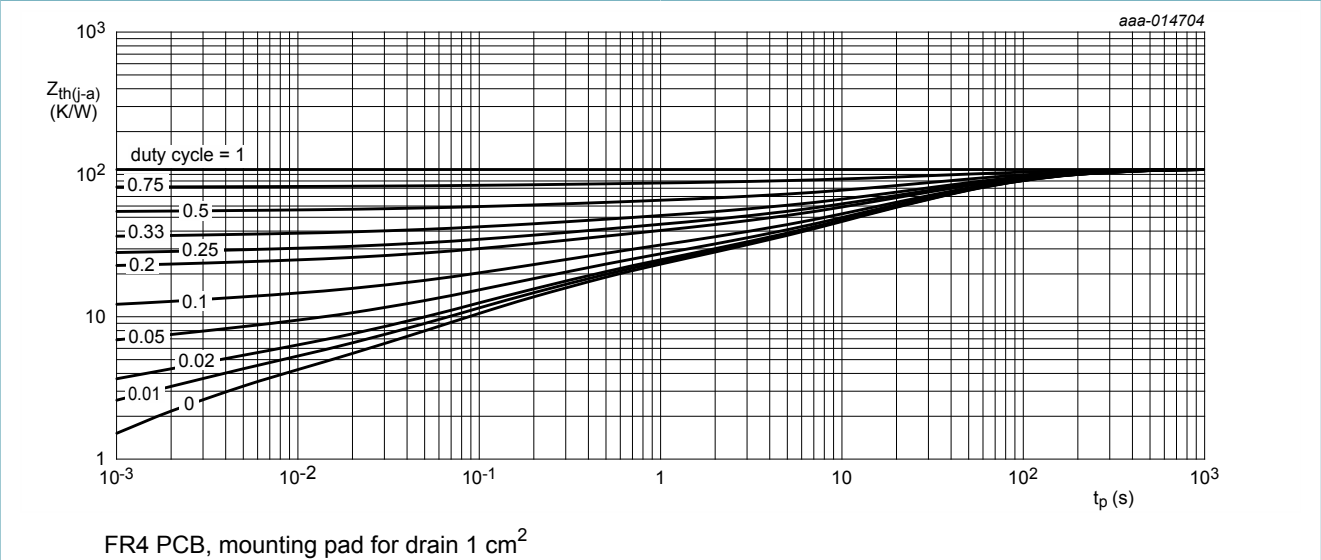


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -10 μA; V _{GS} = 0 V; T _j = 25 °C		-240	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -1 mA; V _{DS} = V _{GS} ; T _j = 25 °C		-0.8	-	-2.8	V
I _{DSS}	drain leakage current	V _{DS} = -200 V; V _{GS} = 0.2 V; T _j = 25 °C		-	-0.1	-60	μA
		V _{DS} = -60 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-200	nA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -200 mA; T _j = 25 °C		-	10	12	Ω
		V _{GS} = -10 V; I _D = -200 mA; T _j = 150 °C		-	21	25	Ω
		V _{GS} = -4.5 V; I _D = -100 mA; T _j = 25 °C		-	13	18	Ω
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -200 mA; T _j = 25 °C		-	200	-	mS
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -50 V; I _D = -250 mA; V _{GS} = -10 V; T _j = 25 °C		-	1.9	5	nC
Q _{GS}	gate-source charge			-	0.3	-	nC
Q _{GD}	gate-drain charge			-	0.6	-	nC
C _{iss}	input capacitance	V _{DS} = -25 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	55	90	pF
C _{oss}	output capacitance			-	20	30	pF
C _{rss}	reverse transfer capacitance			-	5	15	pF
t _{d(on)}	turn-on delay time	V _{DS} = -50 V; I _D = -250 mA; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	3.2	6	ns
t _r	rise time			-	4.6	6	ns
t _{d(off)}	turn-off delay time			-	11.7	20	ns
t _f	fall time			-	7	12	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -200 mA; V _{GS} = 0 V; T _j = 25 °C		-	0.86	1.2	V

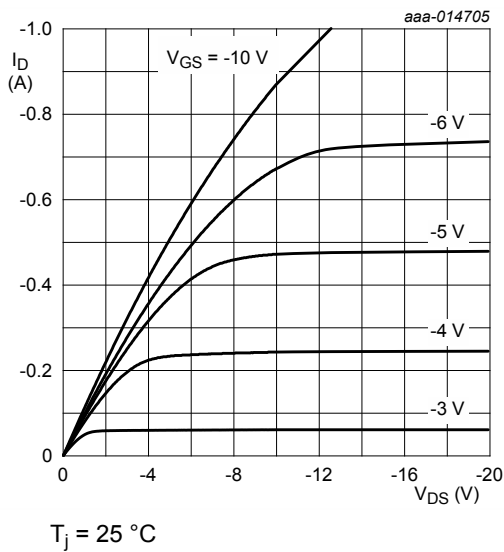


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

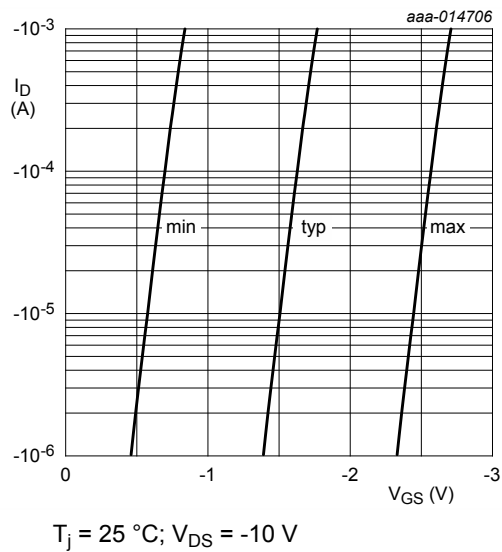


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

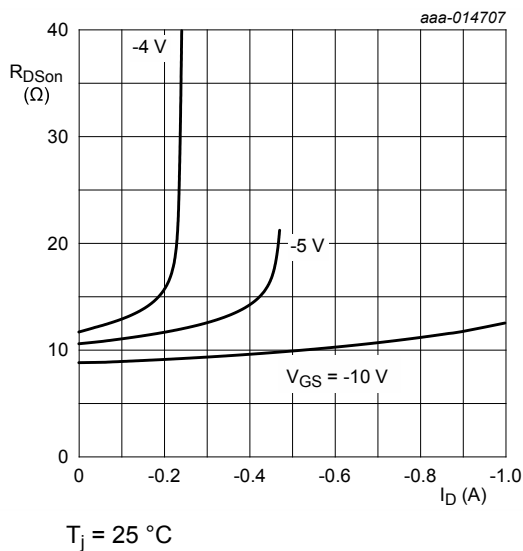


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

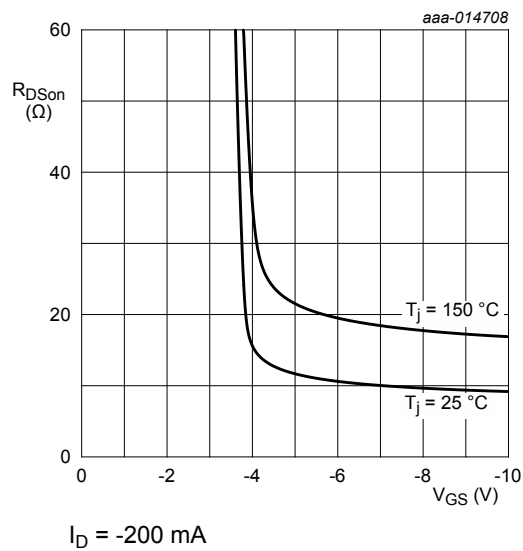


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

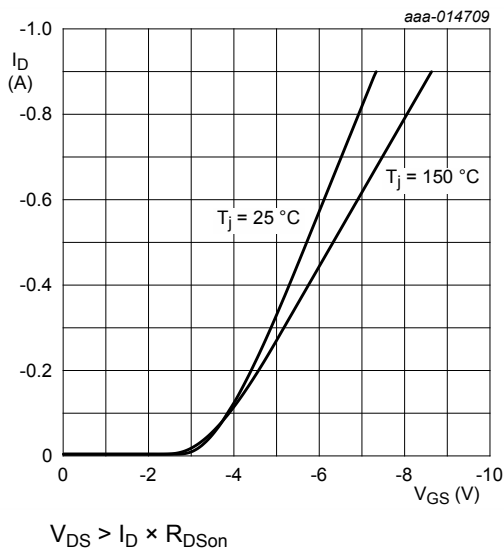


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

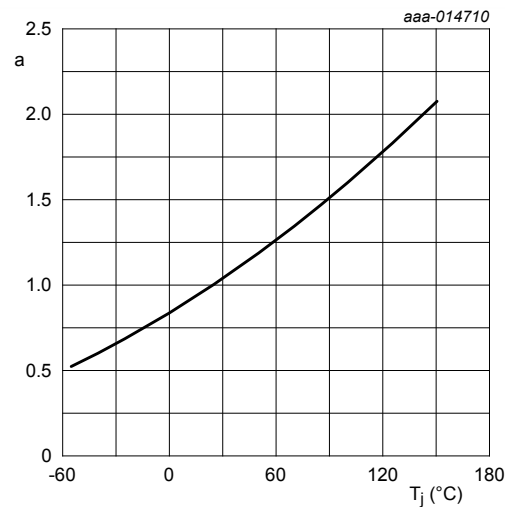


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)25\text{ °C}}}$$

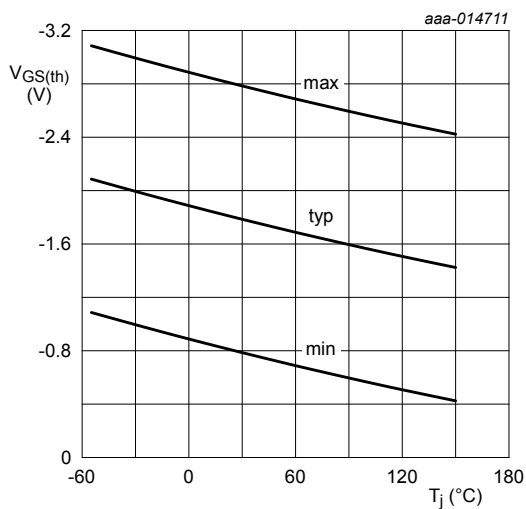


Fig. 12. Gate-source threshold voltage as a function of junction temperature

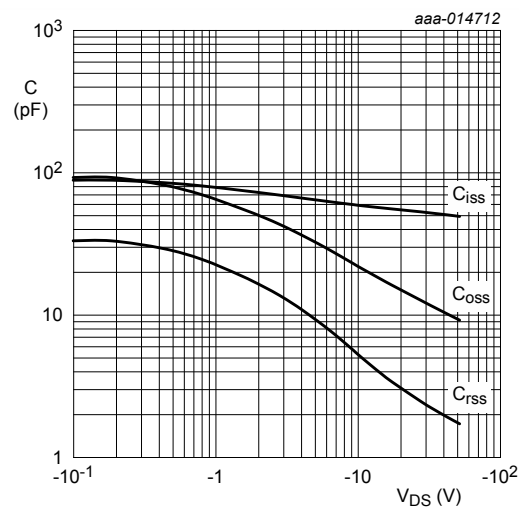


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

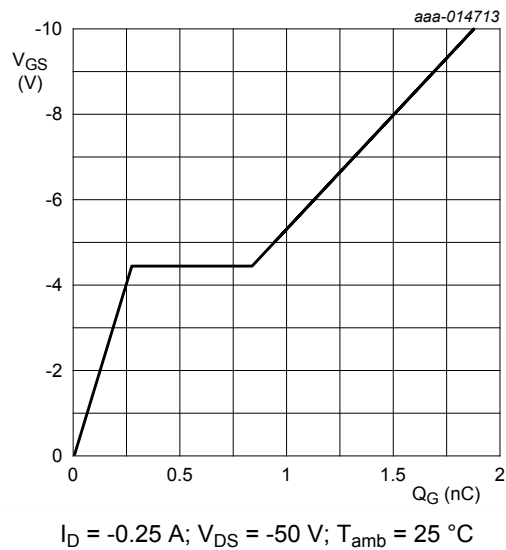


Fig. 14. Gate-source voltage as a function of gate charge; typical values

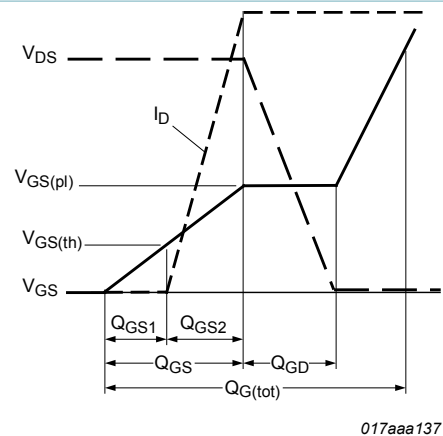


Fig. 15. MOSFET transistor: Gate charge waveform definitions

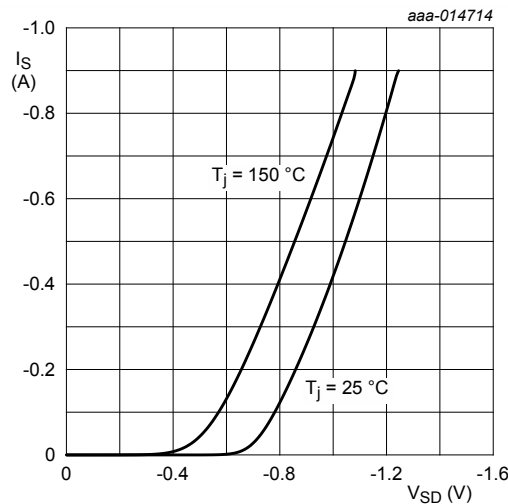


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

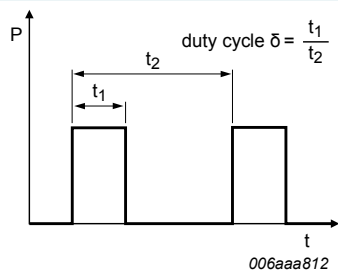


Fig. 17. Duty cycle definition

12. Package outline

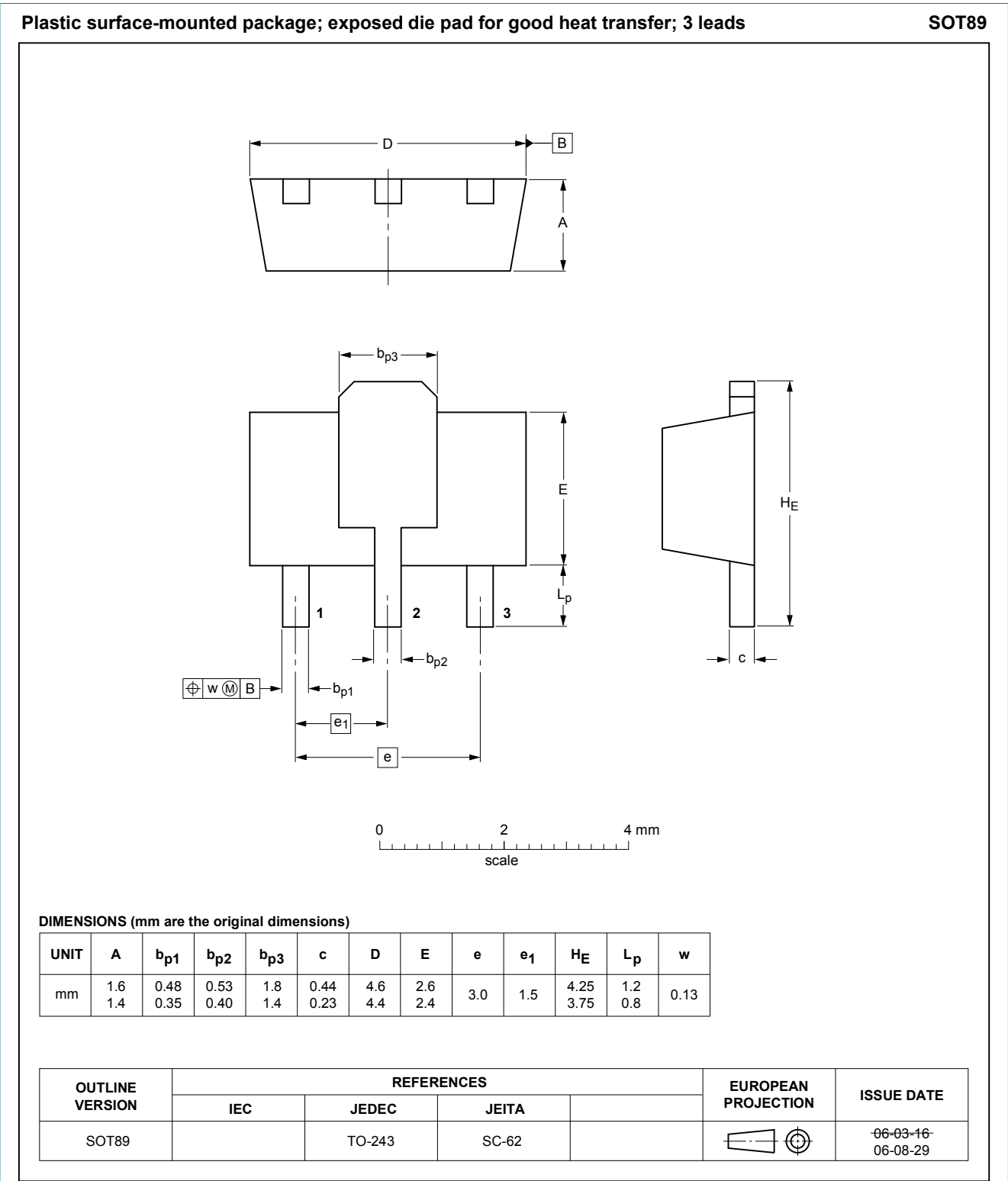


Fig. 18. Package outline SOT89

13. Soldering

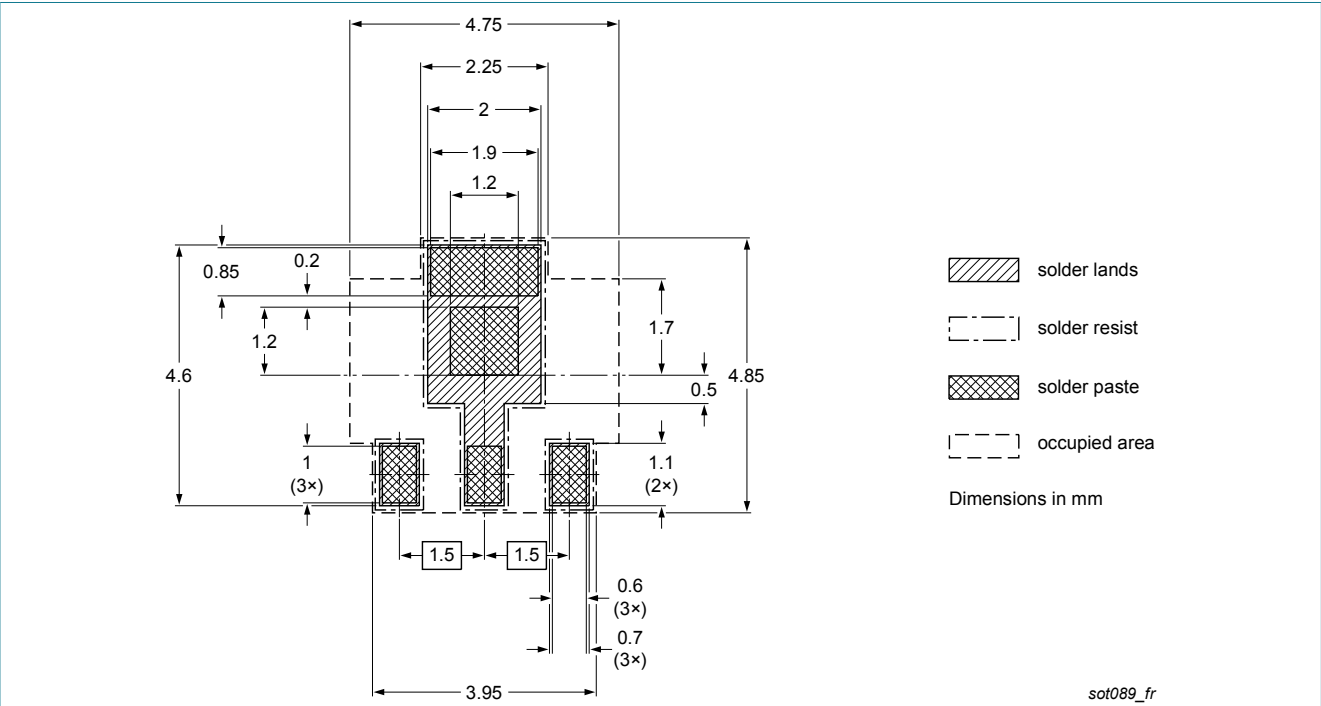


Fig. 19. Reflow soldering footprint for SOT89

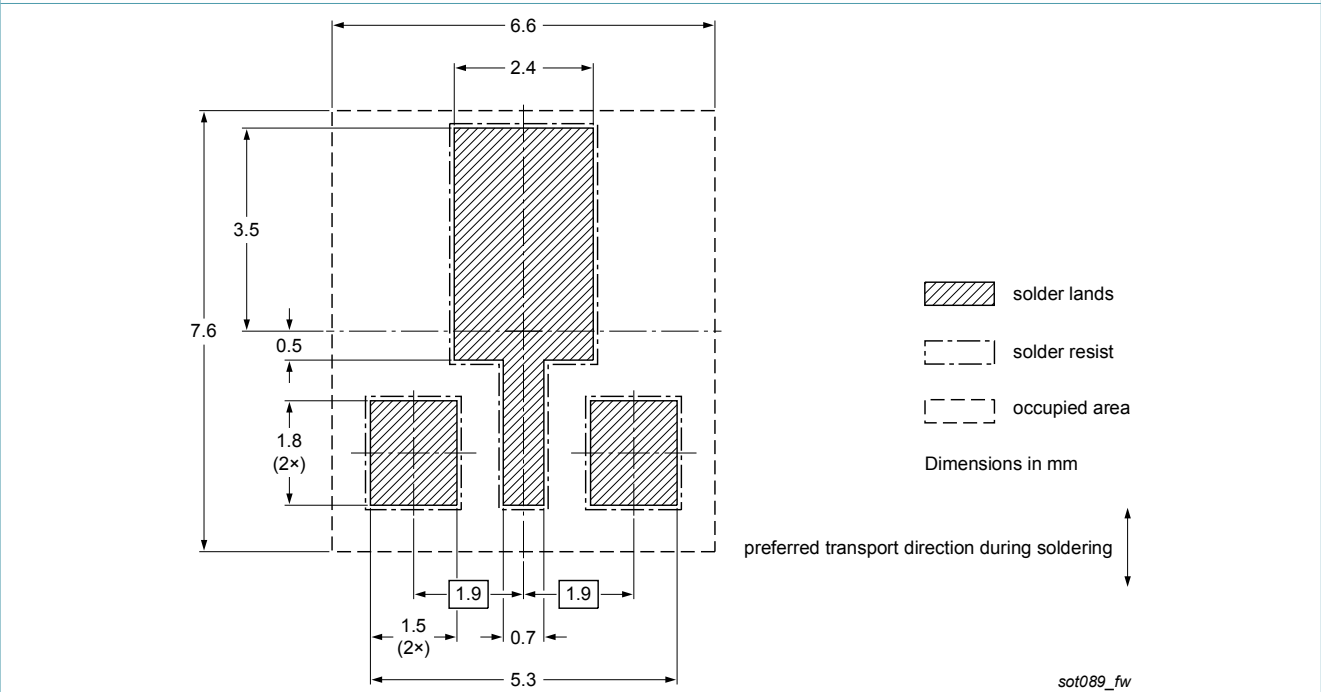


Fig. 20. Wave soldering footprint for SOT89

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BSS192 v.4	20141212	Product data sheet	-	BSS192 v.3
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors - Legal texts have been adapted to the new company name where appropriate			
BSS192 v.3	20021120		-	BSS192 v.2
BSS192 v.2	20020522		-	BSS192 v.1
BSS192 v.1	19970620			-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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