



16-Bit Registers

Features

- Low power, pin-compatible replacement for LCX, LPT, LVC, LVCH & LVT families
- 5V tolerant inputs and outputs*
- 6 mA & 24 mA balanced drive outputs
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for reduced noise
- FCT-C speed at 5.2 ns
- Latch-up performance exceeds JEDEC standard no. 17
- Typical output skew < 250 ps
- Industrial temperature range of -40°C to +85°C
- TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)
- Typical V_{Olp} (ground bounce) performance exceeds Mil Std 883D
- $V_{CC} = 2.7V$ to $3.6V$
- ESD (HBM) > 2000V

CY74FCT163H374

- Bus hold on data inputs
- Eliminates the need for external pull-up or pull-down resistors
- *Devices with bus hold are not recommended for translating rail-to-rail CMOS signals to 3.3V logic levels

CY74FCT163LD374

- Lite Drive™ option for low noise applications
- 6 mA balanced drive outputs
- FCT-A speed at 6.5 ns
- $V_{CC} = 3.0V$ to $3.6V$
- ESD (HBM) > 1100V

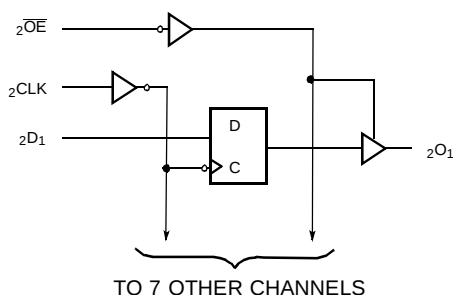
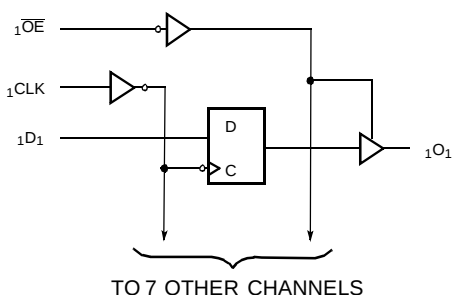
Functional Description

These devices are 16-bit D-type registers designed for use as buffered registers in high-speed, low power bus applications. These devices can be used as two independent 8-bit registers or as a single 16-bit register by connecting the output Enable ($\overline{OE}$) and Clock (CLK) inputs. The outputs are 24-mA balanced output drivers with current limiting resistors to reduce the need for external terminating resistors, and provide for minimal undershoot and reduced ground bounce. Flow-through pinout and small shrink packaging aid in simplifying board layout.

The CY74FCT163H374 and CY74FCT163LDH374 have "bus hold" on the data inputs, which retain the input's last state whenever the source driving the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

The CY74FCT163374 and the CY74FCT16LD374 are designed with inputs and outputs capable of being driven by 5.0V buses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power off disable feature enabling them to be used in applications requiring live insertion.

Logic Block Diagrams CY74FCT163374, CY74FCT163H374, CY74FCT163LD374, CY74FCT163LDH374



Pin Configuration SSOP/TSSOP Top View

$\overline{1OE}$	1	48	$1CLK$
$1O_1$	2	47	$1D_1$
$1O_2$	3	46	$1D_2$
GND	4	45	GND
$1O_3$	5	44	$1D_3$
$1O_4$	6	43	$1D_4$
V_{CC}	7	42	V_{CC}
$1O_5$	8	41	$1D_5$
$1O_6$	9	40	$1D_6$
GND	10	39	GND
$1O_7$	11	38	$1D_7$
$1O_8$	12	37	$1D_8$
$2O_1$	13	36	$2D_1$
$2O_2$	14	35	$2D_2$
GND	15	34	GND
$2O_3$	16	33	$2D_3$
$2O_4$	17	32	$2D_4$
V_{CC}	18	31	V_{CC}
$2O_5$	19	30	$2D_5$
$2O_6$	20	29	$2D_6$
GND	21	28	GND
$2O_7$	22	27	$2D_7$
$2O_8$	23	26	$2D_8$
$2OE$	24	25	$2CLK$

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Function Table^[1]

Inputs			Outputs	Function
D	CLK	OE	O	
X	L	H	Z	High-Z
X	H	H	Z	
L	$\downarrow$	L	L	Load Register
H	$\downarrow$	L	H	
L	$\downarrow$	H	Z	
H	$\downarrow$	H	Z	

Pin Description

Name	Description
D	Data Inputs ^[2]
CLK	Clock Inputs
OE	Three-State Output Enable Inputs (Active LOW)
O	Three-State Outputs

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage Range 0.5V to +4.6V

DC Input Voltage -0.5V to +7.0V

DC Output Voltage -0.5V to +7.0V

DC Output Current

(Maximum Sink Current/Pin) -60 to +120 mA

Power Dissipation 1.0W

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	2.7V to 3.6V

Electrical Characteristics for Non Bus Hold Devices Over the Operating Range V_{CC}=2.7V to 3.6V

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{IH}	Input HIGH Voltage	All Inputs	2.0		5.5	V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[6]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =5.5			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	μA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =5.5V			±1	μA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =GND			±1	μA
I _{OS}	Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =GND	-60	-135	-240	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V			±100	μA
I _{CC}	Quiescent Power Supply Current	V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V, V _{CC} =Max.		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{IN} =V _{CC} -0.6V ^[8] , V _{CC} =Max.		2.0	30	μA

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. $\downarrow$ = LOW-to-HIGH Transition.
- On the CY74FCT163H374 & CY74FCT163LDH374 these pins have "bus hold."
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- Typical values are at V_{CC}=3.3V, T_A = +25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Per TTL driven input; all other inputs at V_{CC} or GND.



Electrical Characteristics For Bus Hold Devices Over the Operating Range $V_{CC}=2.7V$ to $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V_{IH}	Input HIGH Voltage	All Inputs	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis ^[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	$V_{CC}=\text{Min.}$, $I_{IN}=-18\text{ mA}$		-0.7	-1.2	V
I_{IH}	Input HIGH Current	$V_{CC}=\text{Max.}$, $V_I=V_{CC}$			± 100	μA
I_{IL}	Input LOW Current				± 100	μA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input ^[9]	$V_{CC}=\text{Min.}$ $V_I=2.0V$	-50			μA
		$V_I=0.8V$	+50			μA
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input ^[9]	$V_{CC}=\text{Max.}$, $V_I=1.5V$			± 500	μA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}$, $V_{OUT}=V_{CC}$			± 1	μA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}$, $V_{OUT}=\text{GND}$			± 1	μA
I_{OS}	Short Circuit Current ^[7]	$V_{CC}=\text{Max.}$, $V_{OUT}=\text{GND}$	-60	-135	-240	mA
I_{OFF}	Power-Off Disable	$V_{CC}=0V$, $V_{OUT}\leq 4.5V$			± 100	μA
I_{CC}	Quiescent Power Supply Current	$V_{IN}\leq 0.2V$, $V_{CC}=\text{Max.}$			+40	μA
ΔI_{CC}	Quiescent Power supply Current (TTL inputs HIGH)	$V_{IN}=V_{CC}-0.6V$ ^[8] , $V_{CC}=\text{Max.}$			+350	μA

Electrical Characteristics For Balanced Drive Devices Over the Operating Range $V_{CC}=2.7V$ to $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
I_{ODL}	Output LOW Dynamic Current ^[7]	$V_{CC}=3.3V$, $V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=1.5V$	45		110	mA
I_{ODH}	Output HIGH Dynamic Current ^[7]	$V_{CC}=3.3V$, $V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=1.5V$	-45		-110	mA
V_{OH}	Output HIGH Voltage	$V_{CC}=\text{Min.}$, $I_{OH}=-0.1\text{ mA}$	$V_{CC}-0.2$			V
		$V_{CC}=\text{Min.}$, $I_{OH}=-8\text{ mA}$	2.4 ^[10]	3.0		V
		$V_{CC}=3.0V$, $I_{OH}=-24\text{ mA}$	2.0	3.0		V
V_{OL}	Output LOW Voltage	$V_{CC}=\text{Min.}$, $I_{OL}=0.1\text{ mA}$			0.2	V
		$V_{CC}=\text{Min.}$, $I_{OL}=24\text{ mA}$		0.3	0.55	V

Electrical Characteristics For Lite Drive Devices Over the Operating Range $V_{CC}=3.0V$ to $3.6V$

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
I_{ODL}	Output LOW Dynamic Current ^[7]	$V_{CC}=3.3V$, $V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=1.5V$	15.0		45	mA
I_{ODH}	Output HIGH Dynamic Current ^[7]	$V_{CC}=3.3V$, $V_{IN}=V_{IH}$ or V_{IL} , $V_{OUT}=1.5V$	-15.0		-45	mA
V_{OH}	Output HIGH Voltage	$V_{CC}=3.0V$, $I_{OH}=-6\text{ mA}$	2.4	3.0		V
V_{OL}	Output LOW Voltage	$V_{CC}=3.0V$, $I_{OL}=6\text{ mA}$			0.55	V

Notes:

9. Pins with bus hold are described in Pin Description.
10. $V_{OH}=V_{CC}-0.6V$ at rated current.



Capacitance^[6] ($T_A = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	4.5	6.0	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ. ^[5]	Max.	Unit
I _{CCD}	Dynamic Power Supply Current ^[11]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ =GND	V _{IN} =V _{CC} or V _{IN} =GND	50	75	μA/MHz
I _C	Total Power Supply Current ^[12]	V _{CC} =Max., f ₁ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$ =GND	V _{IN} =V _{CC} or V _{IN} =GND	0.5	0.8	mA
			V _{IN} =V _{CC} −0.6V or V _{IN} =GND	0.5	0.8	mA
		V _{CC} =Max., f ₁ =2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$ =GND	V _{IN} =V _{CC} or V _{IN} =GND	2.0	3.0 ^[13]	mA
			V _{IN} =V _{CC} −0.6V or V _{IN} =GND	2.0	3.3 ^[13]	mA

Switching Characteristics Over the Operating Range $V_{CC} = 3.0\text{V}$ to 3.6V ^[14,15]

Parameter	Description	CY74FCT163374A CY74FCT163H374A		CY74FCT163374C CY74FCT163H374C		Unit	Fig. No. ^[16]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	1.5	6.5	1.5	5.2	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.5	1.5	5.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.5	1.5	5.0	ns	1, 7, 8
t_{SU}	Input Setup time	2.0		2.0		ns	1, 4
t_H	Input Hold time	1.5	-	1.5	-	ns	1, 4
$t_{SK(O)}$	Output Skew ^[17]		0.5		0.5	ns	—

Notes:

- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4\text{V}$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- For $V_{CC} = 2.7$, propagation delay, output enable and output disable times should be degraded by 20%.
- See "Parameter Measurement Information" in the General Information section.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.



Switching Characteristics Over the Operating Range $V_{CC}=3.0V$ to $3.6V$ ^[14,15]

Parameter	Description	CY74FCT163LD374 ^[18] CY74FCT163LDH374		CY74FCT163LD374A ^[18] CY74FCT163LDH374A		Unit	Fig. No. ^[16]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Q Output	1.5	10	1.5	6.5	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	12.5	1.5	6.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	5.5	ns	1, 7, 8
t_{SU}	Input Setup time	2.0		2.0		ns	1, 4
t_H	Input Hold time	1.5		1.5		ns	1, 4
$t_{SK(O)}$	Output Skew ^[17]		0.5		0.5	ns	—

Note:

18. For Lite Drive devices the load capacitance is 30 pF. For all others it is 50 pF.

Ordering Information CY74FCT163374

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT163374CPAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163374CPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT163374APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163374APVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT163H374

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.2	CY74FCT163H374CPAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163H374CPVC	O48	48-Lead (300-Mil) SSOP	
6.5	CY74FCT163H374APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163H374APVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT163LD374

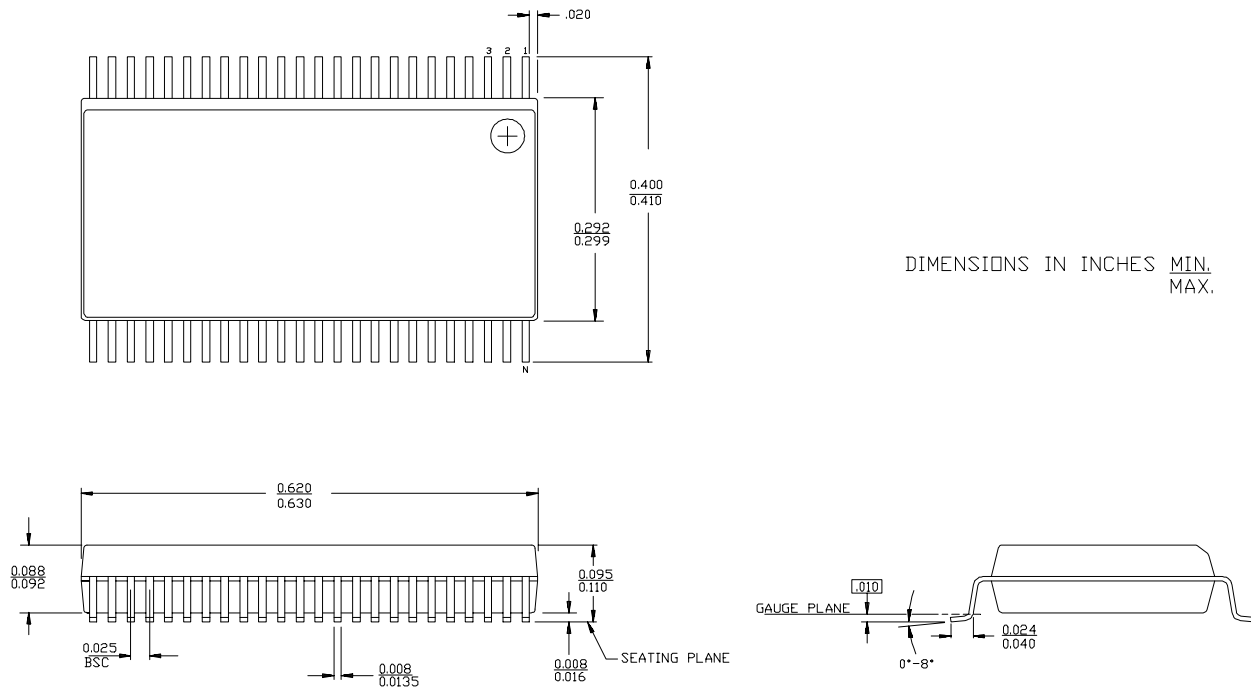
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5	CY74FCT163LD374APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LD374APVC	O48	48-Lead (300-Mil) SSOP	
10	CY74FCT163LD374PAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LD374PVC	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT163LDH374

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.5	CY74FCT163LDH374APAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LDH374APVC	O48	48-Lead (300-Mil) SSOP	
10	CY74FCT163LDH374PAC	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163LDH374PVC	O48	48-Lead (300-Mil) SSOP	

Package Diagrams

48-Lead Shrunk Small Outline Package O48



48-Lead Thin Shrunk Small Outline Package Z48

