

# TB2104F

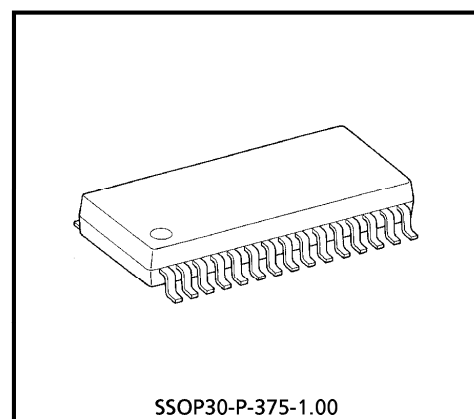
## VFD DRIVER

The TB2104F is a VFD (fluorescent display tube) driver IC implemented by the Bi-CMOS process.

The logic section is configured with CMOS transistors, and the high voltage tolerant output driver section is configured with bipolar transistors.

### FEATURES

- Incorporates a shift register, latch, and driver capable of handling 20 bits of data.
- The output driver comes with an active pull-down, so it can function as a VFD grid, anode driver.
- Three serial data lines are used to input display data.
- The data receiver section can also accept general-purpose serial data and T-BUS (Toshiba Semiconductor Bus).
- In serial data mode, multiple drivers can be cascaded to expand the handling capacity in 20bit increments.

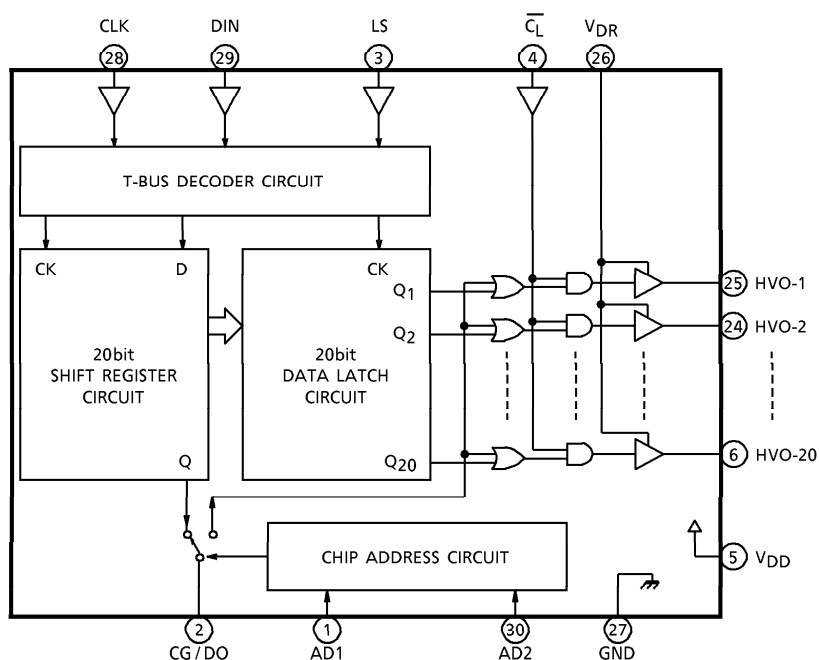


Weight : 0.7g (Typ.)

### PIN CONNECTION

AD1	1	30	AD2
CG/DO	2	29	DIN
LS	3	28	CLK
$\overline{C_L}$	4	27	GND
V <sub>DD</sub>	5	26	V <sub>DR</sub>
HVO-20	6	25	HVO-1
HVO-19	7	24	HVO-2
HVO-18	8	23	HVO-3
HVO-17	9	22	HVO-4
HVO-16	10	21	HVO-5
HVO-15	11	20	HVO-6
HVO-14	12	19	HVO-7
HVO-13	13	18	HVO-8
HVO-12	14	17	HVO-9
HVO-11	15	16	HVO-10

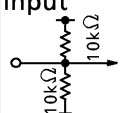
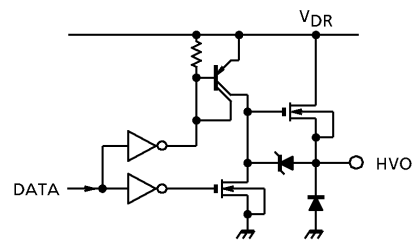
### BLOCK DIAGRAM



980508EBA2

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## PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	AD1	Address Setting Input	<ul style="list-style-type: none"> <li>Chip select/address setting inputs</li> <li>When using in Serial Mode, keep AD1 and AD2 "Open".</li> <li>In other settings than "Open", it becomes T-BUS Mode and addresses up to 8 kinds can be set.</li> </ul>	3-value input 
30	AD2			
3	LS	Strobe Input	<ul style="list-style-type: none"> <li>Serial data input terminals</li> <li>Inputs display data through the DIN terminal synchronizing with rise of CLK input.</li> <li>Display data are updated when inputting "H" level into LS terminal after completing data input.</li> <li>In T-BUS Mode, LS terminal becomes "PERIOD" input.</li> </ul>	CMOS Input
28	CLK	Clock Input		
29	DIN	Data Input		
2	CG/DO	Lamp Test Input and Data Output	<ul style="list-style-type: none"> <li>Lamp test input terminal and data output terminal</li> <li>In Serial Mode (AD1 = AD2 = Open), this terminal serves as the serial data output terminal and enables cascade connection of driver IC.</li> <li>In T-BUS Mode, this terminal serves as the lamp test input and is able to use all the driver outputs (HVO-1 ~ 20) at "H" level by inputting "H" level signal.</li> <li>During the normal operation in T-BUS Mode, use this terminal by fixing at "L" level.</li> </ul>	CMOS Input / CMOS Output built in pull-down resistor 20kΩ
4	$\overline{C_L}$	Clear Input	<ul style="list-style-type: none"> <li>Driver OFF (blanking) input terminal</li> <li>All the driver outputs are fixed at "L" level when "L" level signal is input.</li> <li>When "H" level signal is input, it becomes the normal mode.</li> </ul>	CMOS Input built in pull-up resistor 20kΩ
5	V <sub>DD</sub>	Logic Unit Power Supply	<ul style="list-style-type: none"> <li>Power supply and GND terminals</li> </ul>	—
26	V <sub>DR</sub>	Drive Unit Power Supply		
27	GND	Ground		
25 24 23 ⋮ ⋮ 8 7 6	HVO-1 HVO-2 HVO-3 ⋮ ⋮ HVO-18 HVO-19 HVO-20	Driver Output	<ul style="list-style-type: none"> <li>High-tension driver output terminal</li> <li>Equivalent circuit</li> </ul> 	—

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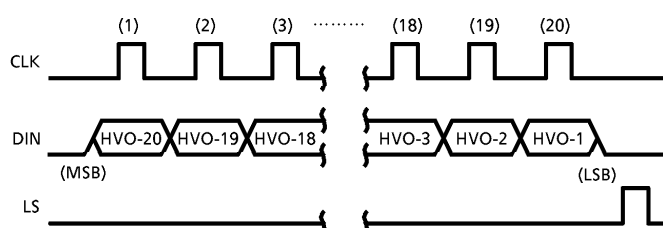
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## EXPLANATION OF OPERATION

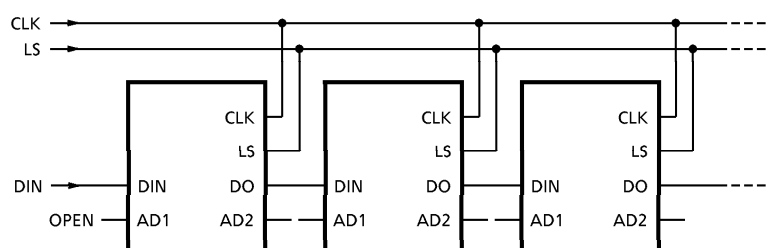
### 1. Serial data receiver circuit

- The serial data receiver circuit can be changed over to operate in the serial mode or the T-BUS Mode by switching, the AD1/AD2 terminals.
- In T-BUS Mode, the AD1/AD2 terminals become the chip select code inputs and it becomes possible to connect up to 8 drivers on the same bus line.

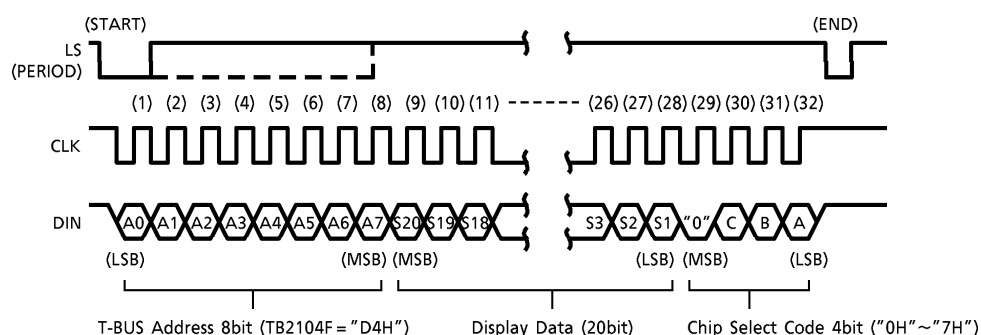
#### 1) Input data format in serial data mode (AD1 = AD2 = "Open")



- Display data are updated when data for 20 bits are input from MSB side (HVO-20), synchronizing with rise of CLK signal and LS input is set to "H" level after inputting data.
- When increasing driver ICs, connect them through cascade connection as shown below :



### 2. Input data format in T-BUS Mode



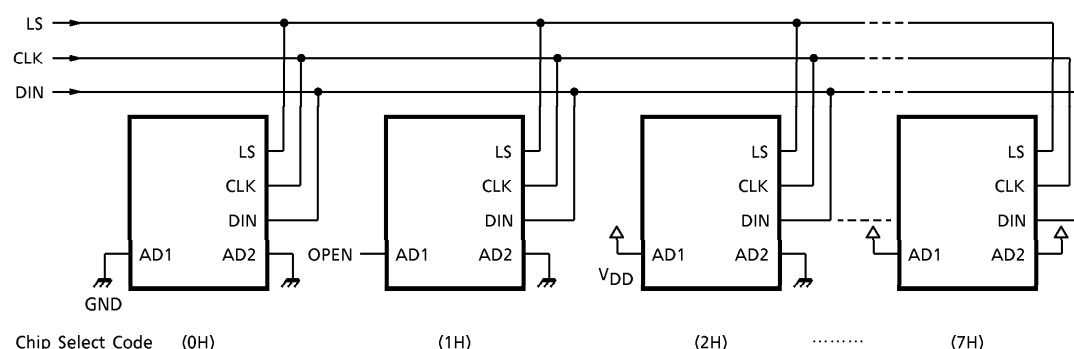
- In T-BUS Mode, start data transmission with the LS terminal (PERIOD) set at "L" level. Thereafter, send address data 8 bits, display data 20 bits, and chip select code 4 bits, synchronizing with rise of CLK signal.
- After sending data, set the LS terminal to "L" level again and terminate the data sending.
- On a driver IC when chip select code agrees with chip select code by AD1/AD2, display data are updated at fall of LS signal.
- When increasing driver ICs, it is possible to connect up to 8 ICs on the same bus line in combination with AD1/AD2.
- T-BUS address of the TB2104F is "D4H".
- When data are transferred using T-BUS address "00H", the data can be input to all the driver ICs on the bus line independently of chip select codes ("0H"~"7H"). (This function can be used for Power On reset.)

### 3. AD1/AD2 input and chip select codes

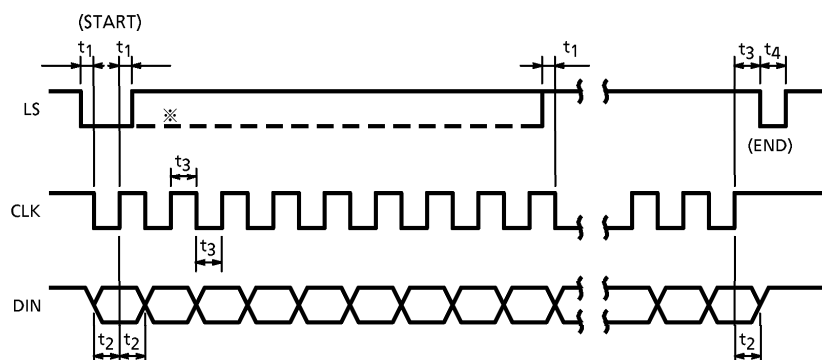
AD1/AD2 input are 3-value level inputs and 9 kinds (3×3) of codes can be set.

AD1	AD2	A	B	C	CHIP SELECT CODE	MODE
V <sub>IH</sub>	V <sub>IH</sub>	1	1	1	"7H"	T-BUS
V <sub>IM</sub>		0	1	1	"6H"	
V <sub>IL</sub>		1	0	1	"5H"	
V <sub>IH</sub>	V <sub>IM</sub>	0	0	1	"4H"	Serial
V <sub>IM</sub>		—	—	—	—	
V <sub>IL</sub>		1	1	0	"3H"	
V <sub>IH</sub>	V <sub>IL</sub>	0	1	0	"2H"	T-BUS
V <sub>IM</sub>		1	0	0	"1H"	
V <sub>IL</sub>		0	0	0	"0H"	

### 4. Example of extension of driver ICs in T-BUS Mode chip select code



## 5. T-BUS Mode timing chart



- $f_{CLK} \leq 500\text{kHz}$
- $t_1 \geq 0.2\mu\text{s}$ ,  $t_2 \geq 0.2\mu\text{s}$
- $t_3 \geq 1.0\mu\text{s}$ ,  $t_4 \geq 1.0\mu\text{s}$

## Cautions for use

- Therefore, multiple driver outputs may possibly become "H" level simultaneously after the power is turned ON.  
(In this case, the allowable power dissipation of a device using this IC may possible be exceeded, destroying the device.)
- In order to avoid this, while keeping the clear terminal ( $\overline{CL}$ ) at "L" level, rise the power supply for the logic unit ( $V_{DD}$ ) and then, that for the drivers ( $V_{DR}$ ), reset all the contents of the data latch ("L" level) by serial data, and initialize the driver outputs.

## MAXIMUM RATINGS (Ta = 25°C)

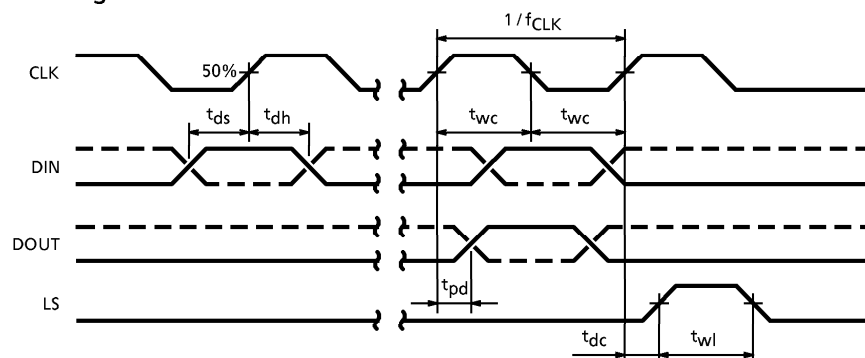
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	-0.3~7.0	V
Input Voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> +0.3	V
Driver Voltage	V <sub>DR</sub>	V <sub>DD</sub> ~60	V
Driver Current	I <sub>DR</sub>	50	mA
Power Dissipation	P <sub>D</sub> (Note)	800	mW
Operating Temperature	T <sub>opr</sub>	-40~85	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

(Note) In case it is used at more than Ta = 25°C, it is considered by reducing 6.4mW each 1°C.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V<sub>DD</sub> = 5V, V<sub>DR</sub> = 50V, Ta = 25°C)

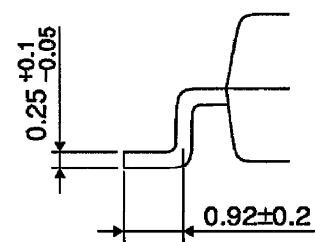
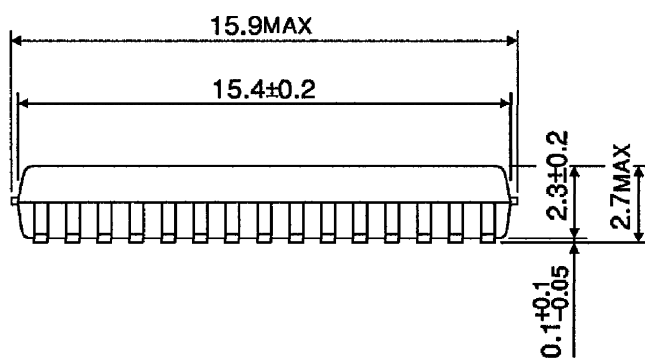
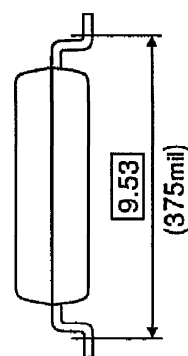
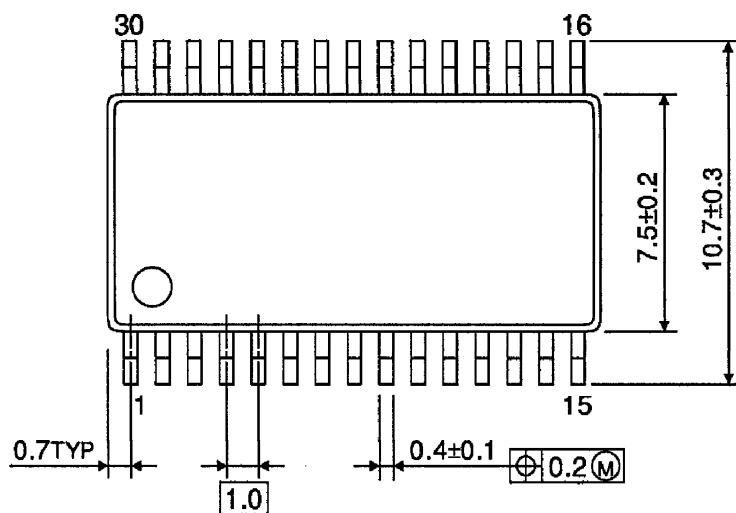
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage (1)		V <sub>DD</sub>	—	Logic unit		4.5	5.0	5.5	V
Operating Supply Voltage (2)		V <sub>DR</sub>	—	Driver unit		10	~	50	V
Operating Supply Current (1)		I <sub>DD</sub>	—	No load, No input		—	0.3	1.5	mA
Operating Supply Current (2)		I <sub>DR</sub>	—	No load, Output V <sub>OL</sub> level		—	2.3	3.5	mA
Input Voltage	“H” Level	V <sub>IH</sub> (1)	—	CMOS input terminal DIN, CLK, LS, CG, $\overline{\text{CL}}$		V <sub>DD</sub> × 0.7	~	V <sub>DD</sub>	V
	“L” Level	V <sub>IL</sub> (1)				GND	~	V <sub>DD</sub> × 0.3	
Input Voltage	“H” Level	V <sub>IH</sub> (2)	—	3-value input terminal AD1, AD2		V <sub>DD</sub> − 0.5	~	V <sub>DD</sub>	V
	Open	V <sub>IM</sub>				—	V <sub>DD</sub> × 0.5	—	
	“L” Level	V <sub>IL</sub> (2)				GND	~	GND + 0.5	
Input Current	“H” Level	I <sub>IH</sub>	—	CMOS input terminal	V <sub>IH</sub> = 5V	− 1.0	~	1.0	μA
	“L” Level	I <sub>IL</sub>			V <sub>IL</sub> = 0V	− 1.0	~	1.0	
Input Resistance		R <sub>IN</sub>	—	3-value input terminal		80	100	120	kΩ
Output Current	“H” Level	I <sub>OH</sub> (1)	—	HVO-1~ − 20 Output terminal	V <sub>OH</sub> = 45V	—	− 8.4	− 5	mA
	“L” Level	I <sub>OL</sub> (1)			V <sub>OL</sub> = 3V	2.0	2.7	—	
Output Current	“H” Level	I <sub>OH</sub> (2)	—	DO output terminal	V <sub>OH</sub> = 4V	—	− 0.3	− 0.1	mA
	“L” Level	I <sub>OL</sub> (2)			V <sub>OL</sub> = 1V	0.1	0.3	—	
Clock Frequency		f <sub>CLK</sub>	Fig.1	CLK max. operating		—	5.0	4.0	MHz
Clock Pulse Width		t <sub>wc</sub>		CLK min. operating		75	60	—	ns
Data Setup Time		t <sub>ds</sub>		DIN min. operating pulse width		50	40	—	ns
Data Hold Time		t <sub>dh</sub>				50	40	—	ns
LS Pulse Width		t <sub>wl</sub>		LS min. operating		80	60	—	ns
CLK-LS Delay Time		t <sub>dc</sub>		CLK→LS delay time		50	40	—	ns
CLK-DOUT Delay Time		t <sub>pd</sub>		CLK→DOUT delay time CL = 30pF		—	120	160	ns

Fig.1 : Serial data timing chart



**OUTLINE DRAWING**  
SSOP30-P-375-1.00

Unit : mm



Weight : 0.7g (Typ.)