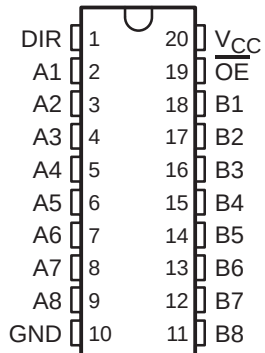


SN54HCT645, SN74HCT645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

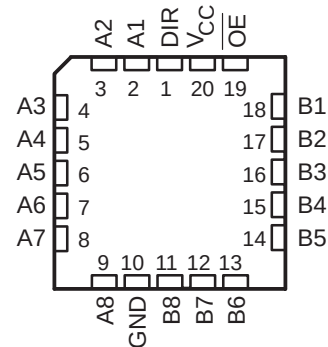
SCLS019D – MARCH 1984 – REVISED AUGUST 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- True Logic

SN54HCT645 . . . J OR W PACKAGE
SN74HCT645 . . . DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT645 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 20	SN74HCT645N	SN74HCT645N
	SOIC – DW	Tube of 25	SN74HCT645DW	HCT645
		Reel of 2000	SN74HCT645DWR	
	SOP – NS	Reel of 2000	SN74HCT645NSR	HCT645
	TSSOP – PW	Tube of 70	SN74HCT645PW	HT645
		Reel of 2000	SN74HCT645PWR	
		Reel of 250	SN74HCT645PWT	
-55°C to 125°C	CDIP – J	Tube of 20	SNJ54HCT645J	SNJ54HCT645J
	CFP – W	Tube of 85	SNJ54HCT645W	SNJ54HCT645W
	LCCC – FK	Tube of 55	SNJ54HCT645FK	SNJ54HCT645FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN54HCT645, SN74HCT645

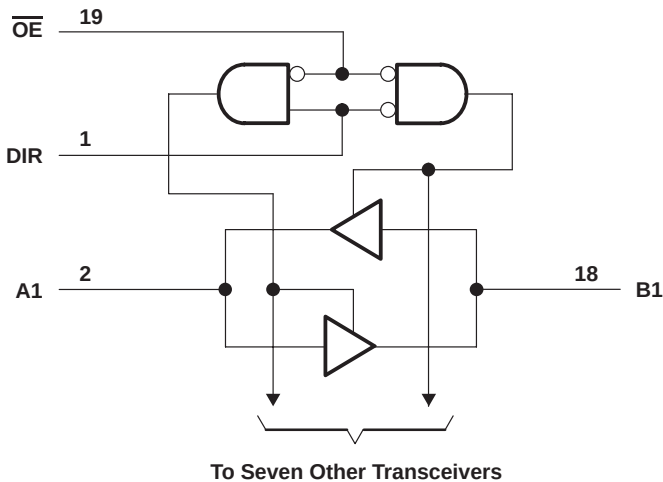
OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCLS019D – MARCH 1984 – REVISED AUGUST 2003

FUNCTION TABLE		
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HCT645, SN74HCT645 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

			SN54HCT645			SN74HCT645			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V	2			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise/fall time				500			500	ns
T _A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCT645		SN74HCT645		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}		V _I = V _{IH} or V _{IL}	I _{OH} = –20 μA	4.5 V	4.4	4.499		4.4		4.4		V
			I _{OH} = –6 mA		3.98	4.3		3.7		3.84		
V _{OL}		V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
			I _{OL} = 6 mA			0.17	0.26		0.4		0.33	
I _I	DIR or $\overline{\text{OE}}$	V _I = V _{CC} or 0		5.5 V	±0.1	±100		±1000		±1000		nA
I _{OZ}	A or B	V _O = V _{CC} or 0		5.5 V	±0.01	±0.5		±10		±5		μA
I _{CC}		V _I = V _{CC} or 0, I _O = 0		5.5 V			8	160		80		μA
ΔI _{CC} [†]		One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}		5.5 V		1.4	2.4	3		2.9		mA
C _i	DIR or $\overline{\text{OE}}$			4.5 V to 5.5 V		3	10	10		10		pF

[†] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT645		SN74HCT645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	4.5 V		16	22		33		28	ns
			5.5 V		14	20		30		25	
t _{en}	$\overline{\text{OE}}$	A or B	4.5 V		25	46		69		58	ns
			5.5 V		22	41		62		52	
t _{dis}	$\overline{\text{OE}}$	A or B	4.5 V		26	40		60		50	ns
			5.5 V		23	36		54		45	
t _t		A or B	4.5 V		9	12		18		15	ns
			5.5 V		8	11		16		14	

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SN54HCT645, SN74HCT645

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT645		SN74HCT645		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	4.5 V		20	30		45		38	ns
			5.5 V		18	27		41		34	
t_{en}	$\overline{OE}$	A or B	4.5 V		36	59		89		74	ns
			5.5 V		30	53		80		67	
t_t		A or B	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, $T_A = 25^\circ\text{C}$

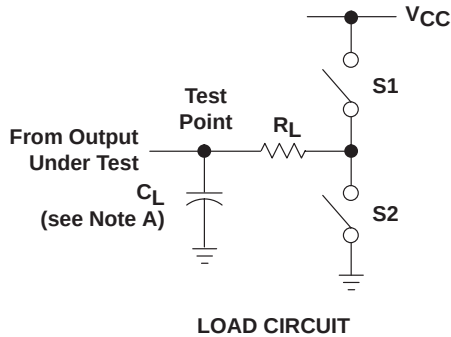
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	No load	40	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

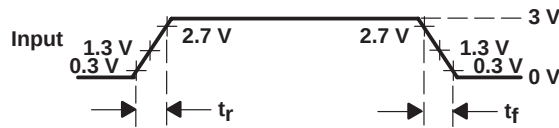


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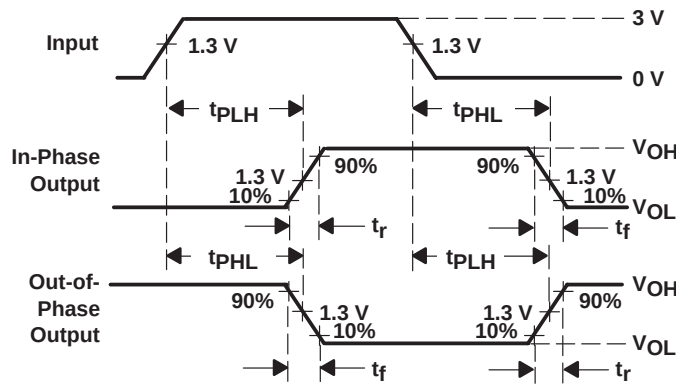
PARAMETER MEASUREMENT INFORMATION



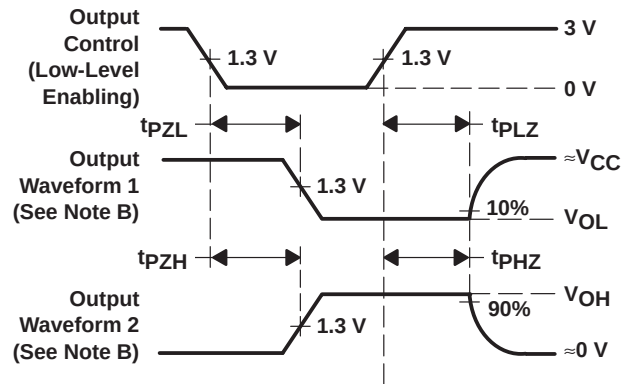
PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	--	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT645DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT645	Samples
SN74HCT645DWE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		Samples
SN74HCT645DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT645	Samples
SN74HCT645DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT645	Samples
SN74HCT645DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT645	Samples
SN74HCT645DWRG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		Samples
SN74HCT645N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT645N	Samples
SN74HCT645N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	-40 to 85		
SN74HCT645NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT645N	Samples
SN74HCT645PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT645	Samples
SN74HCT645PWE4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		Samples
SN74HCT645PWG4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		Samples
SN74HCT645PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT645	Samples
SN74HCT645PWTE4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		Samples
SN74HCT645PWTG4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

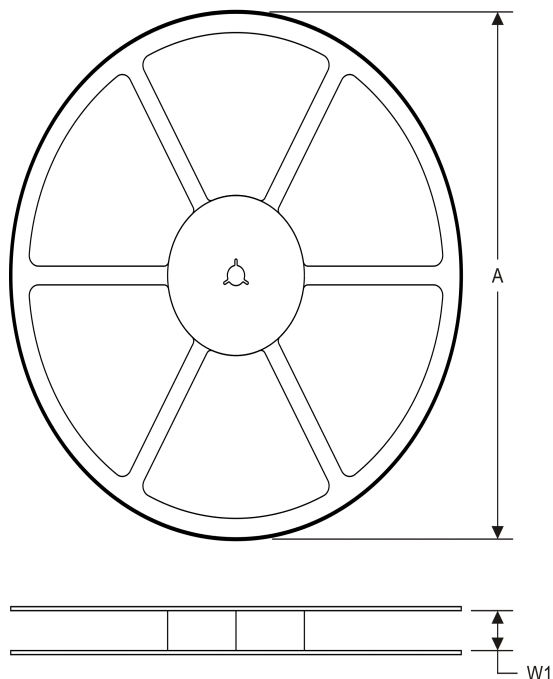
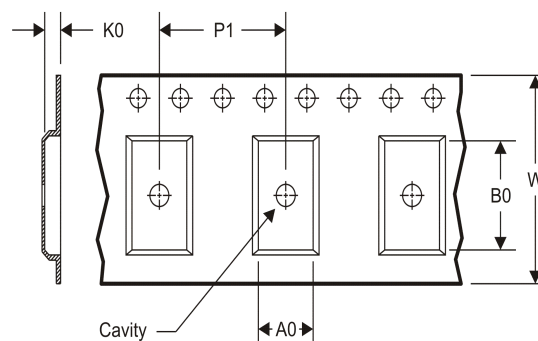
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


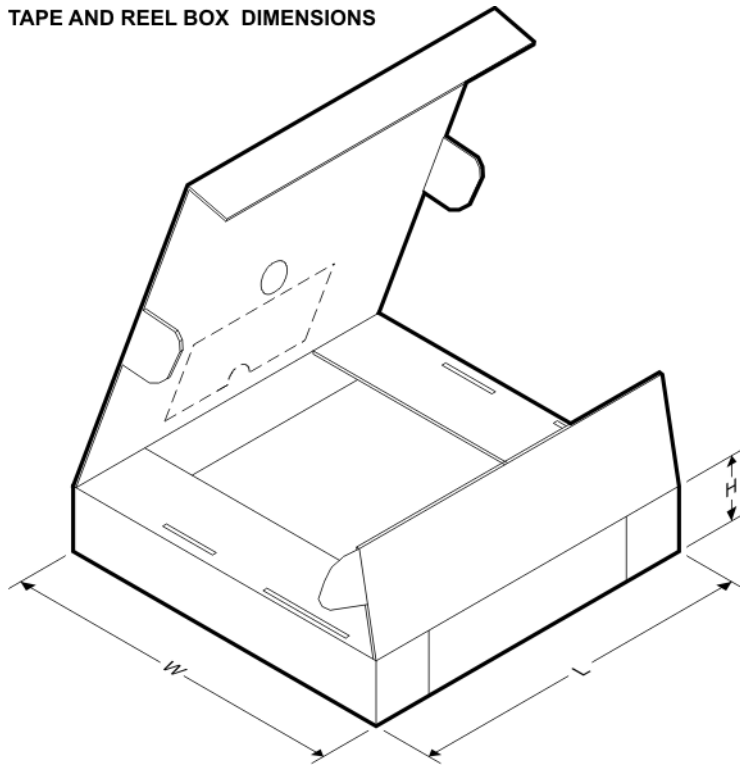
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT645DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74HCT645PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



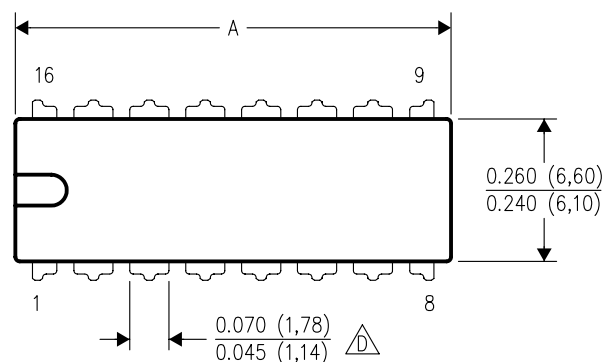
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT645DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HCT645PWT	TSSOP	PW	20	250	367.0	367.0	38.0

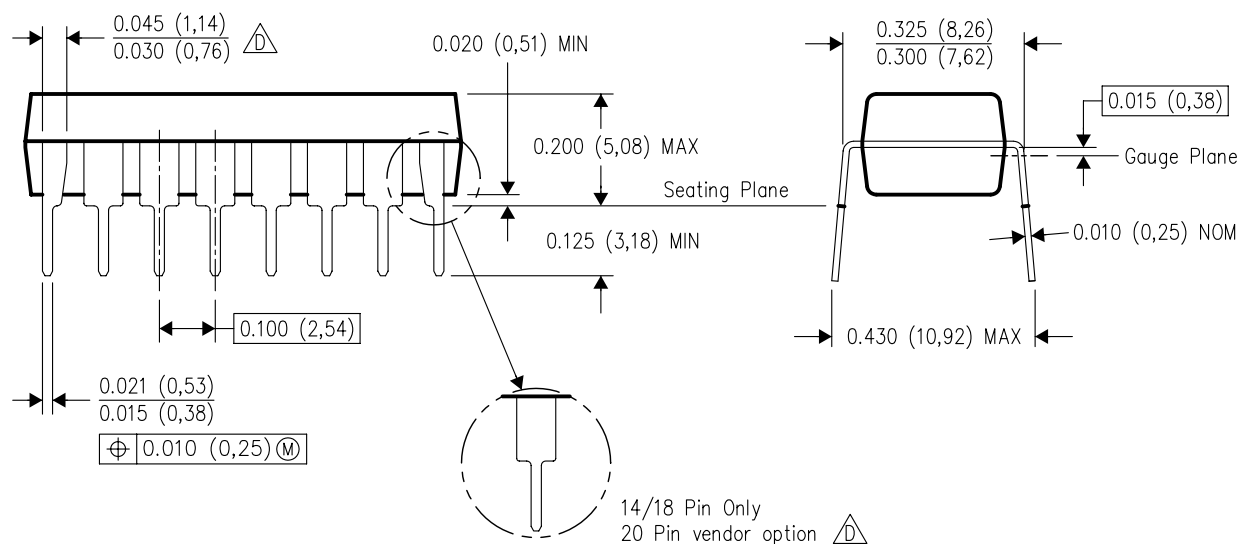
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

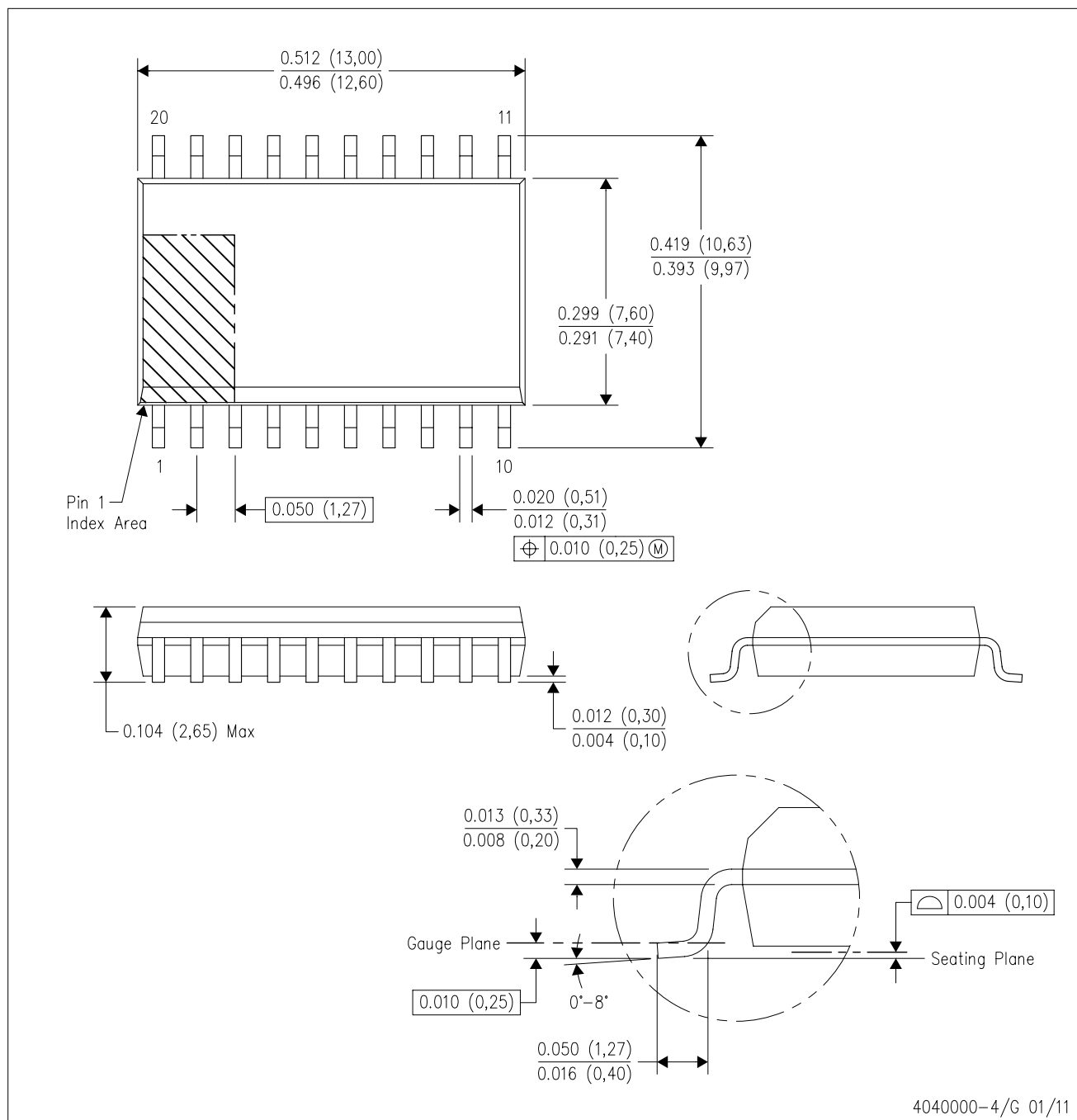


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

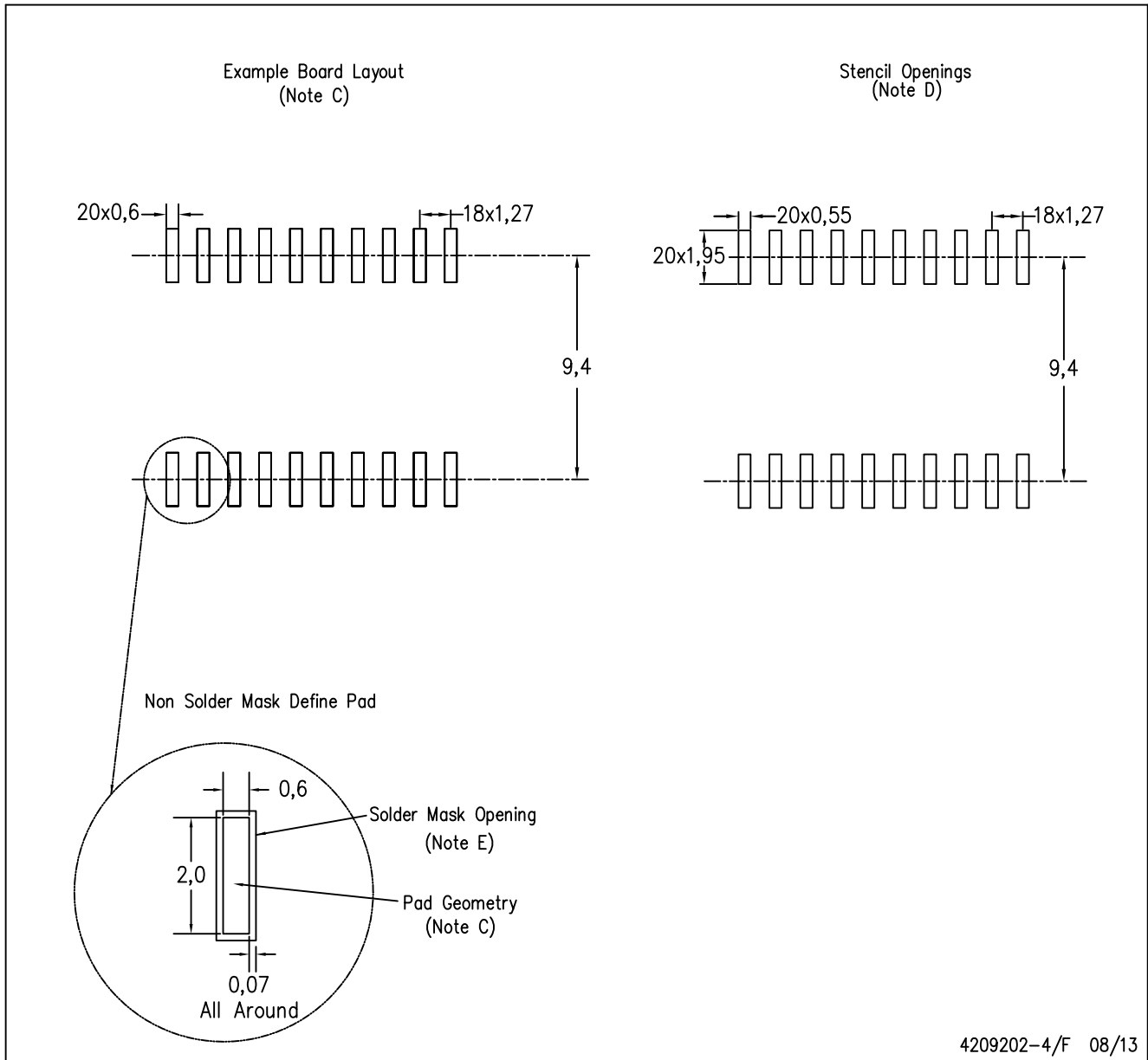
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

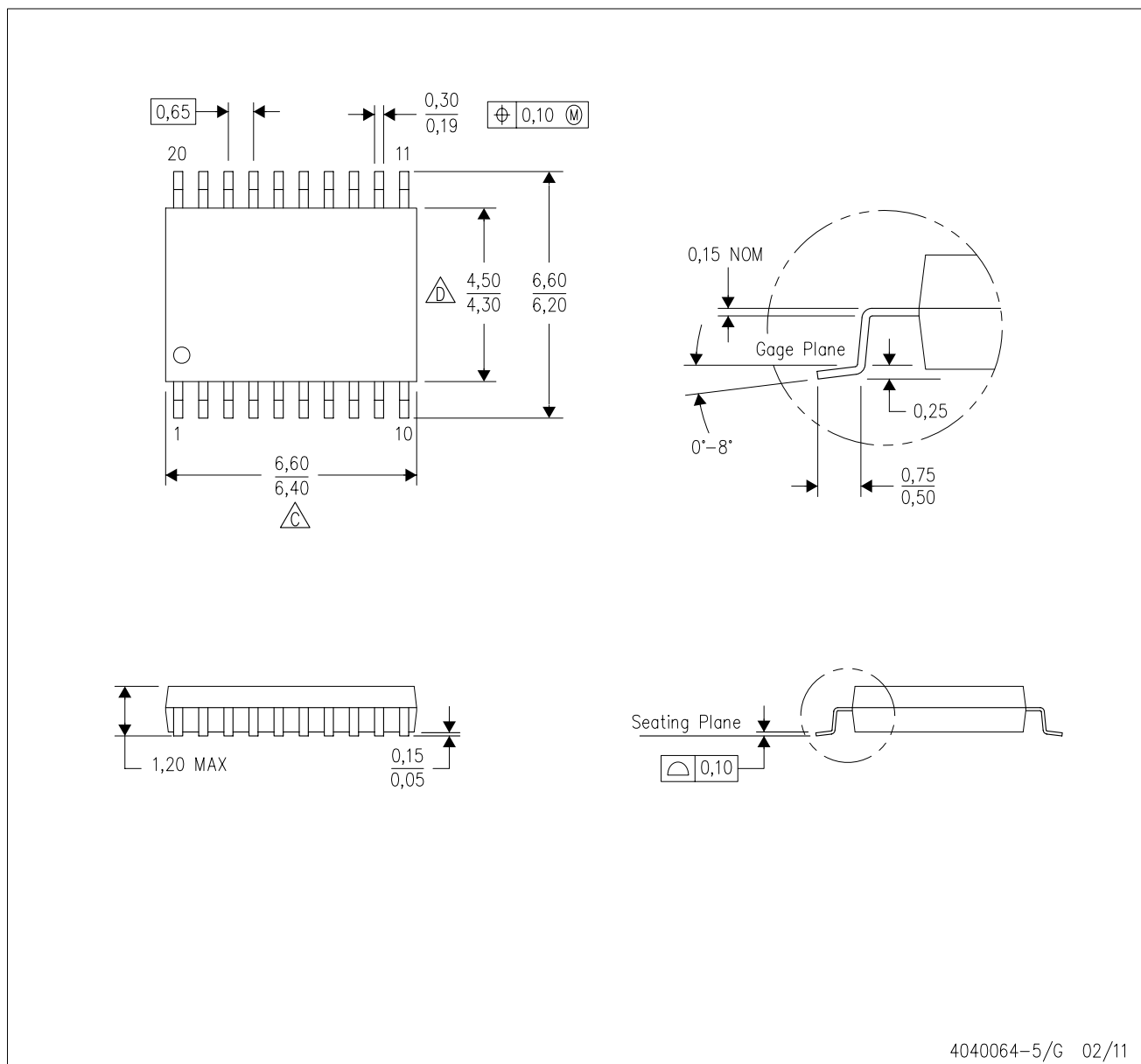
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



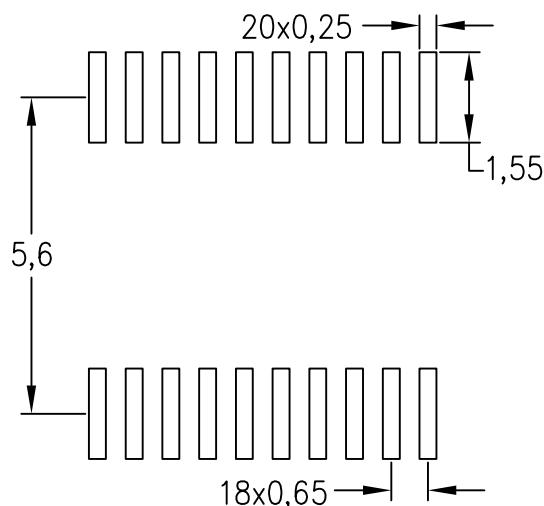
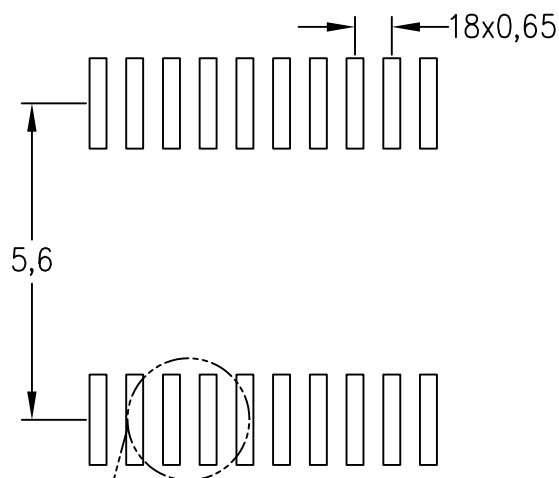
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

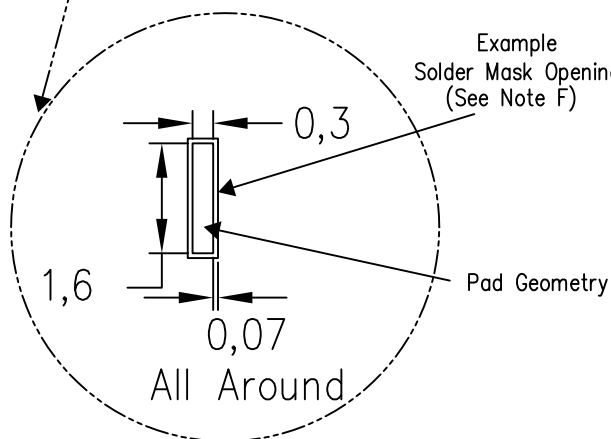
Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).



Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)



4211284-5/F 12/12

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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