CMOS Digital Integrated Circuits Silicon Monolithic

74VHC240FT,74VHC244FT

1. Functional Description

- Octal Bus Buffer

74VHC240FT: INVERTED, 3-STATE OUTPUTS
74VHC244FT: NON-INVERTED, 3-STATE OUTPUTS

2. General

The 74VHC240FT and 74VHC244FT are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The 74VHC240FT is an inverting 3-state buffer having two active-low output enables. The 74VHC244FT is a non-inverting 3-state buffer, and has two active-low output enables.

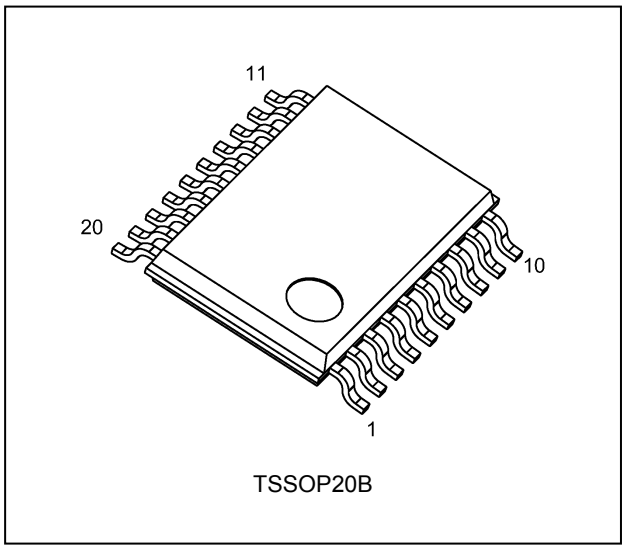
These devices are designed to be used with 3-state memory address drivers, etc.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

3. Features

(1) High speed: t_{pd} = 3.9 ns (typ.) at V_{CC} = 5 V
(2) Low power dissipation: I_{CC} = 4 μA (max) at T_a = 25 °C
(3) High noise immunity: $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (min)
(4) Power down protection is provided on all inputs.
(5) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
(6) Wide operating voltage range: $V_{CC(opr)}$ = 2 V to 5.5 V
(7) Low noise: V_{OLP} = 0.8 V (max)
(8) Pin and function compatible with the 74 serise (74AC/HC/AHC/LV etc.) 240 or 244 type.

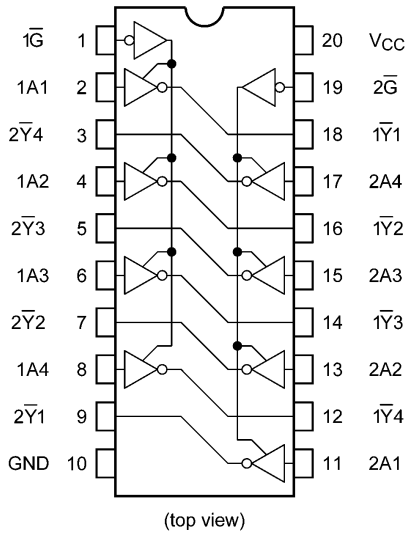
4. Packaging



TSSOP20B

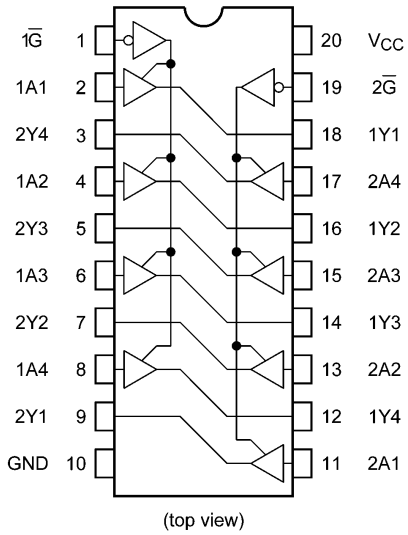
5. Pin Assignment

74VHC240FT



(top view)

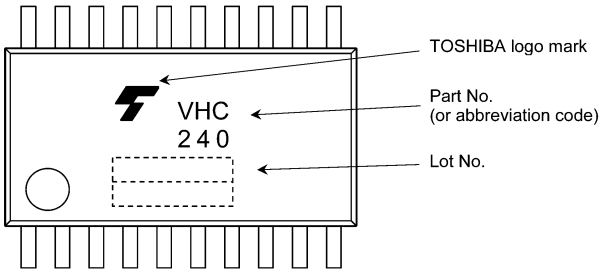
74VHC244FT



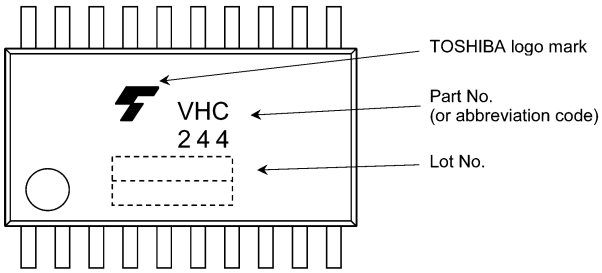
(top view)

6. Marking

74VHC240FT

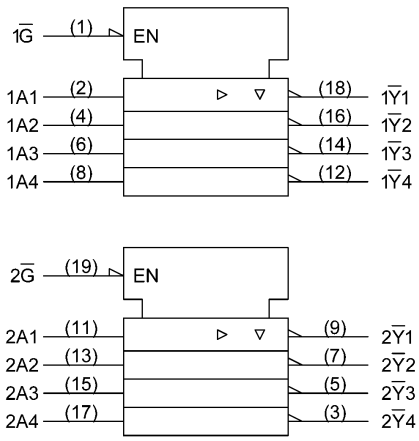


74VHC244FT

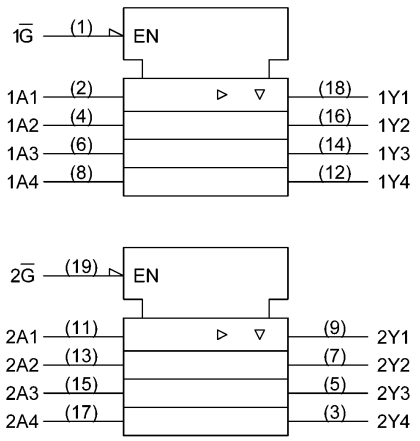


7. IEC Logic Symbol

74VHC240FT



74VHC244FT



8. Truth Table

Input $\overline{G}$	Input A_n	Output Y_n	Output $\overline{Y}_n$
L	L	L	H
L	H	H	L
H	X	Z	Z

X: Don't care
Z: High impedance
Y_n: 74VHC244FT
$\overline{Y}_n$: 74VHC240FT

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input voltage	V_{IN}	-0.5 to 7.0	
Output voltage	V_{OUT}	-0.5 to V_{CC} + 0.5	
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	±20	
Output current	I_{OUT}	±25	
V_{CC}/ground current	I_{CC}	±75	
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	
Output voltage	V_{OUT}		0 to V_{CC}	
Operating temperature	T_{opr}		-40 to 85	°C
Input rise and fall times	dt/dv	V_{CC} = 3.3 ± 0.3 V	0 to 100	ns/V
		V_{CC} = 5 ± 0.5 V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	
				3.0 to 5.5	—	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	2.0	—	
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I_{OH} = -4 mA	3.0	2.58	—	—	
			I_{OH} = -8 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	—	0.1	
				3.0	—	—	0.1	
				4.5	—	—	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA	4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{out} = V_{CC} or GND		5.5	—	—	±0.25	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	

11.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				3.0 to 5.5	V_{CC} x 0.7	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	
				3.0 to 5.5	—	V_{CC} x 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	—	
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -4 mA	3.0	2.48	—	
			I_{OH} = -8 mA	4.5	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 50 μA	2.0	—	0.1	
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 4 mA	3.0	—	0.44	
			I_{OL} = 8 mA	4.5	—	0.44	
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	±2.50	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±1.0	
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	40.0	

11.3. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time	74VHC240FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	—	5.3	7.5	ns
						50	—	7.8	11.0	
					5.0 ± 0.5	15	—	3.6	5.5	
						50	—	5.1	7.5	
	74VHC244FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	—	5.8	8.4	
						50	—	8.3	11.9	
					5.0 ± 0.5	15	—	3.9	5.5	
						50	—	5.4	7.5	
3-state output enable time		t_{PZL},t_{PZH}		R_L = 1 kΩ	3.3 ± 0.3	15	—	6.6	10.6	
						50	—	9.1	14.1	
					5.0 ± 0.5	15	—	4.7	7.3	
						50	—	6.2	9.3	
3-state output disable time		t_{PLZ},t_{PHZ}		R_L = 1 kΩ	3.3 ± 0.3	50	—	10.3	14.0	
					5.0 ± 0.5	50	—	6.7	9.2	
Output skew		t_{osLH},t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	—	1.5	
					5.0 ± 0.5	50	—	—	1.0	
Input capacitance		C_{IN}		—			4	—	10	pF
Output capacitance		C_{OUT}		—			6	—	—	
Power dissipation capacitance	74VHC240FT	C_{PD}	(Note 2)	—			17	—	—	
	74VHC244FT						19	—	—	

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per bit)

11.4. AC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

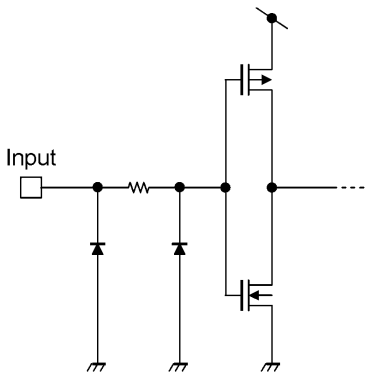
Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	74VHC240FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	1.0	9.0	ns
						50	1.0	12.5	
					5.0 ± 0.5	15	1.0	6.5	
						50	1.0	8.5	
	74VHC244FT	t_{PLH},t_{PHL}		—	3.3 ± 0.3	15	1.0	10.0	
						50	1.0	13.5	
					5.0 ± 0.5	15	1.0	6.5	
						50	1.0	8.5	
3-state output enable time		t_{PZL},t_{PZH}		R_L = 1 kΩ	3.3 ± 0.3	15	1.0	12.5	
						50	1.0	16.0	
					5.0 ± 0.5	15	1.0	8.5	
						50	1.0	10.5	
3-state output disable time		t_{PLZ},t_{PHZ}		R_L = 1 kΩ	3.3 ± 0.3	50	1.0	16.0	
					5.0 ± 0.5	50	1.0	10.5	
Output skew		t_{osLH},t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	1.5	
					5.0 ± 0.5	50	—	1.0	
Input capacitance		C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

11.5. Noise Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 3 ns)

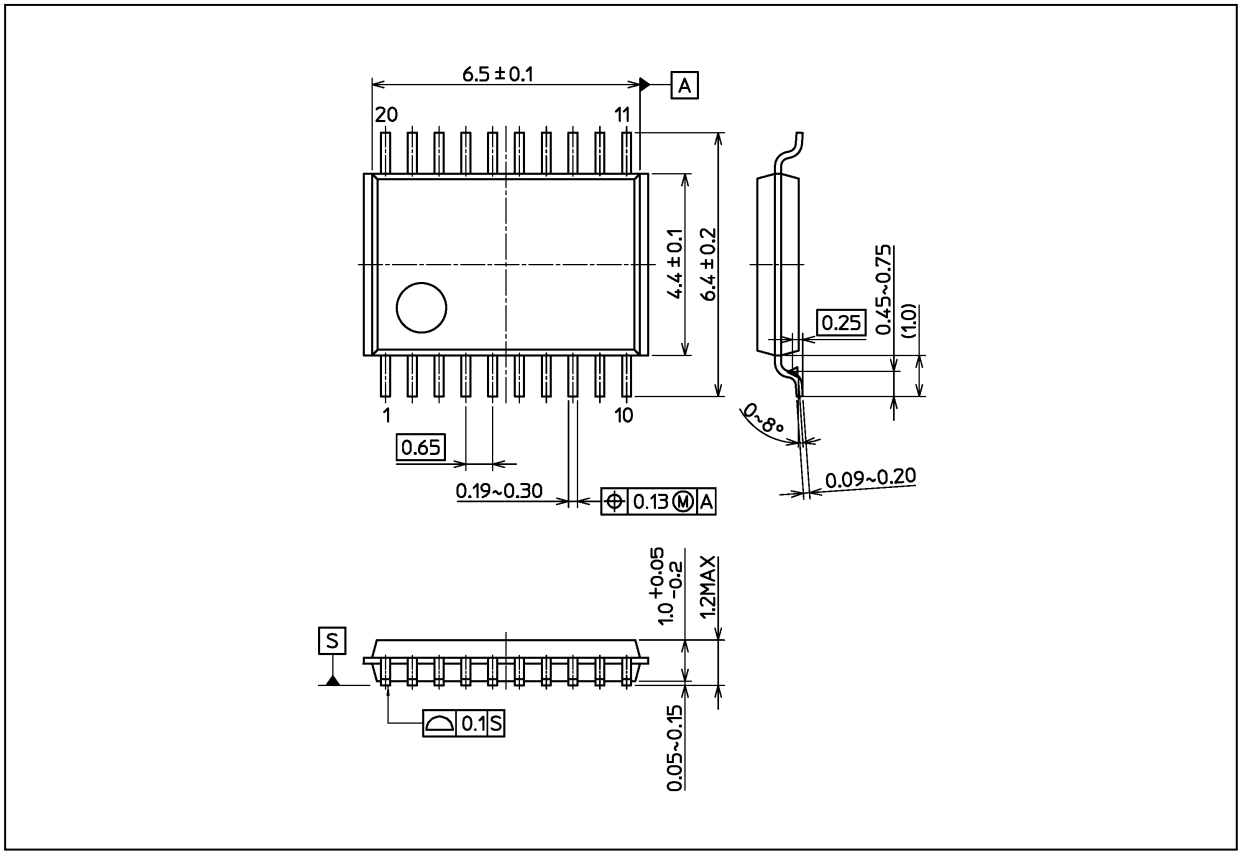
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.5	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	-0.5	-0.8	
Minimum high-level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	
Maximum low-level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	

11.6. Internal Equivalent Circuit



Package Dimensions

Unit: mm



Weight: 0.071 g (typ.)

Package Name(s)
Nickname: TSSOP20B

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