Dual Retriggerable Monostable Multivibrator

74VHC123A

General Description

The VHC123A is an advanced high speed CMOS Monostable Multivibrator fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Each multi-vibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one-shot. The VHC123A can be triggered on the positive transition of the clear while A is held low and B is held high. The output pulse width is determined by the equation: PW = $(R_X)(C_X)$; where PW is in seconds, R is in ohms, and C is in farads.

Limits for R_x and C_x are:

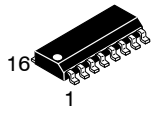
- External capacitor, C_X:
  - No limit
- External resistors, Rx:
  - V_{CC} = 2.0 V, 5 kΩ min
  - V_{CC} > 3.0 V, 1 kΩ min

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

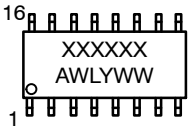
Features

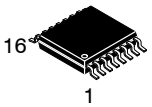
- High Speed: t_{PD} = 8.1 ns (Typ.) at T_A = 25 °C
- Low Power Dissipation: I_{CC} = 4 μA (Max.) at T_A = 25 °C
- Active State: I_{CC} = 600 μA (Max.) at T_A = 25 °C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Power down protection is provided on all inputs
- Pin and function compatible with 74HC123A
- These Devices are Pb-Free and are RoHS Compliant

MARKING DIAGRAMS

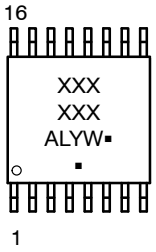


SOIC-16, 150 mils
CASE 751BG





TSSOP-16
CASE 948AH



XXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

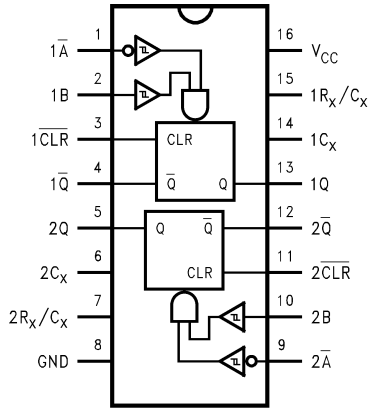


Figure 1. Connection Diagram

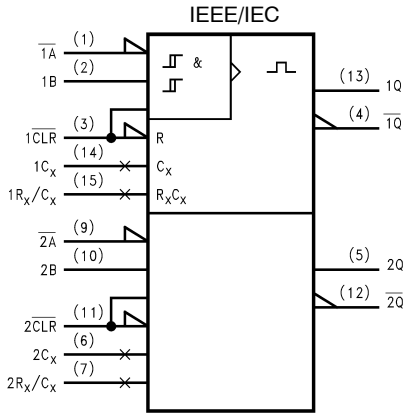


Figure 2. Logic Symbol

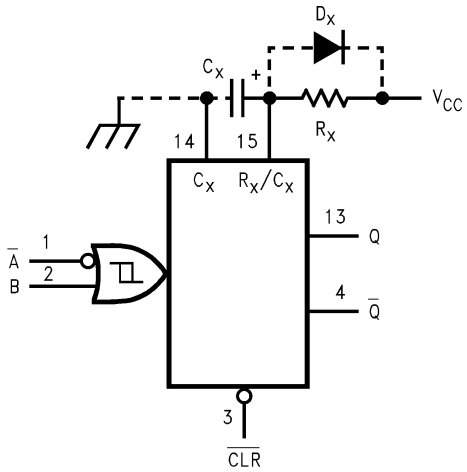
PIN DESRIPTION

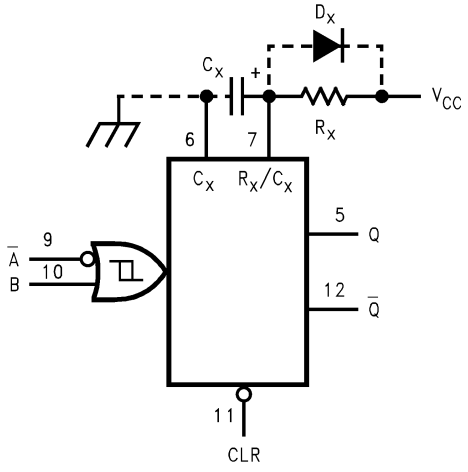
Pin Names	Description
A	Trigger Inputs (Negative Edge)
B	Trigger Inputs (Positive Edge)
CLR	Reset Inputs
Cx	External Capacitor
Rx	External Resistor
Q, $\overline{Q}$	Outputs

TRUTH TABLE

Inputs			Outputs		
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	Function
↓	H	H	⎍	⎍	Output Enable
X	L	H	L	H	Inhibit
H	X	H	L	H	Inhibit
L	↑	H	⎍	⎍	Output Enable
L	H	↑	⎍	⎍	Output Enable
X	X	L	L	H	Reset

H = HIGH Voltage Level
L = LOW Voltage Level
↓ = HIGH-to-LOW Transition
↑ = HIGH-to-HIGH Transition
X = Don't Care





Note A: C_x, R_x, D_x are external Capacitor, Resistor, and Diode, respectively.
Note B: External clamping diode, D_x;
External capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied.
If the supply voltage is turned off, C_x discharges mainly through the internal (parasitic) diode. If C_x is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the in rush current is automatically limited and damage to the IC is avoided.
The maximum value of forward current through the parasitic diode is ±20mA. In the case of a large C_x, the limit of fall time of the supply voltage is determined as follows:
$t_f \geq (V_{CC} - 0.7)\ C_x / 20\ mA$
(t_f is the time between the supply voltage turn off and the supply voltage reaching 0.4 V_{CC})
In the event a system does not satisfy the above condition, an external clamping diode (D_x) is needed to protect the IC from rush current.

Figure 3. Block Diagram

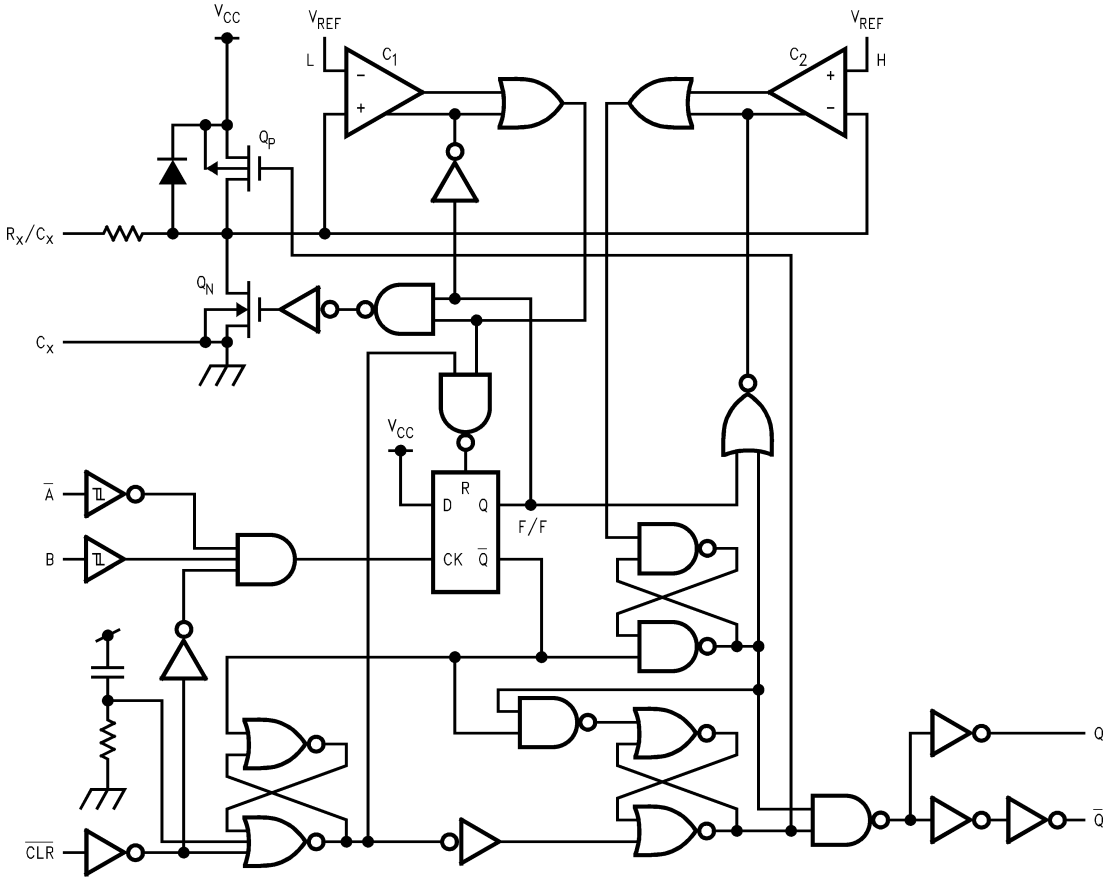


Figure 4. System Diagram

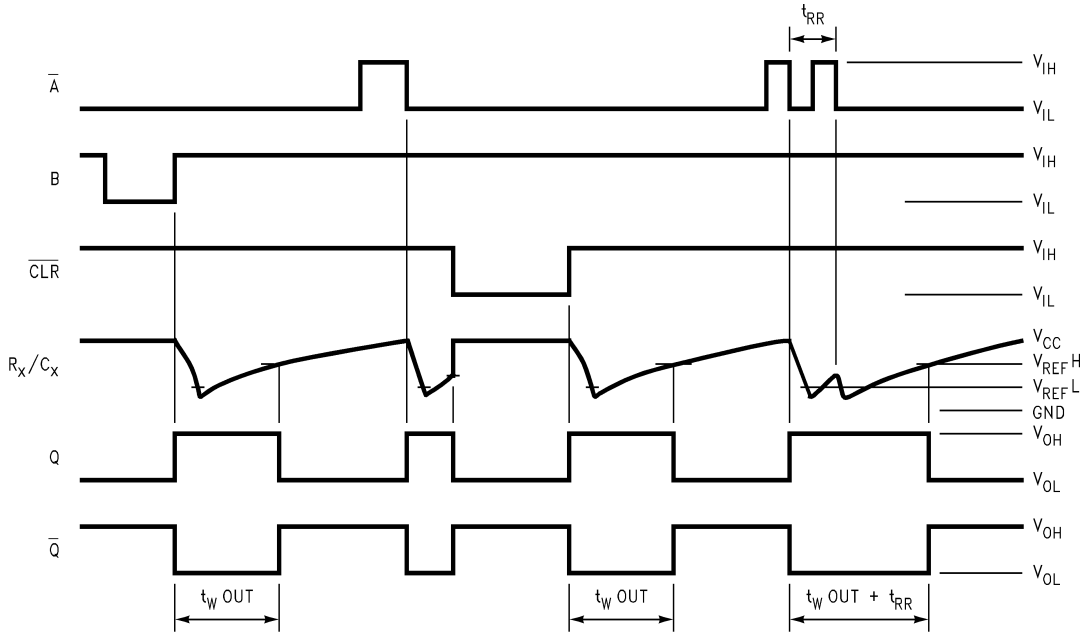


Figure 5. Timing Chart

FUNCTIONAL DESCRIPTION

Stand-by State

The external capacitor (C_x) is fully charged to V_{CC} in the Stand-by State. That means, before triggering, the Q_P and Q_N transistors which are connected to the R_x/C_x node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

Trigger Operation

Trigger operation is effective in any of the following three cases. First, the condition where the A input is LOW, and B input has a rising signal; second, where the B input is HIGH, and the A input has a falling signal; and third, where the $\overline{A}$ input is LOW and the B input is HIGH, and the $\overline{CLR}$ input has a rising signal.

After a trigger becomes effective, comparators C_1 and C_2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the R_x/C_x node drops. If the R_x/C_x voltage level falls to the internal reference voltage $V_{ref}L$, the output of C_1 becomes LOW. The flip-flop is then reset and Q_N turns off. At that moment C_1 stops but C_2 continues operating.

After Q_N turns off, the voltage at the R_x /C_x node starts rising at a rate determined by the time constant of external capacitor C_x and resistor R_x.

Upon triggering, output Q becomes HIGH, following some delay time of the internal F/F and gates. It stays HIGH even if the voltage of R_x/C_x changes from falling to rising. When R_x/C_x reaches the internal reference voltage $V_{ref}H$, the output of C_2 becomes LOW, the output Q goes LOW and C_2 stops its operation. That means, after triggering, when the voltage level of the R_x/C_x node reaches $V_{ref}H$, the IC returns to its MONOSTABLE state.

With large values of C_x and R_x, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, t_W (OUT), is as follows:

t_W (OUT) = 1.0 C_x R_x

Retrigger Operation (74VHC123A)

When a new trigger is applied to either input $\overline{A}$ or B while in the MONOSTABLE state, it is effective only if the IC is charging C_x. The voltage level of the R_x/C_x node then falls to $V_{ref}L$ level again. Therefore the Q output stays HIGH if the next trigger comes in before the time period set by C_x and R_x.

If the new trigger is very close to a previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2nd trigger, t_{RR} (Min), depends on V_{CC} and C_x.

Reset Operation

In normal operation, the $\overline{CLR}$ input is held HIGH. If $\overline{CLR}$ is LOW, a trigger has no affect because the Q output is held LOW and the trigger control F/F is reset. Also, Q_p turns on and C_x is charged rapidly to V_{CC}.

This means if $\overline{CLR}$ is set LOW, the IC goes into a wait state.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−16 TSSOP−16	126 159	°C/W
P_D	Power Dissipation in Still Air at 25 °C	SOIC−16 TSSOP−16	995 787	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.112 in	–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device's lifespan or reliability.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 2)		0	5.5	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0	100 20	ns/V
C_X	External Capacitor (Note 3)		–	–	F
R_X	External Resistor (Note 3)	V_{CC} = 2.0 V V_{CC} > 3.0 V	5 1	– –	kΩ

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). These may not float.
3. The maximum allowable values of C_x and R_x are a function of the leakage of capacitor C_x, the leakage of the device, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for R_x > 1 MΩ.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V_{CC} (V)	T_A = 25 °C			T_A = −40 °C to 85 °C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage			2.0 3.0–5.5	1.50 0.7x V_{CC}	– –	– –	1.50 0.7x V_{CC}	– –	V
V_{IL}	LOW Level Input Voltage			2.0 3.0–5.5	– –	– –	0.50 0.3x V_{CC}	– –	0.50 0.3x V_{CC}	V
V_{OH}	HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	– – –	1.9 2.9 4.4	– – –	V
			I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94	– –	– –	2.48 3.80	– –	V
V_{OL}	LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0 3.0 4.5	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5	– –	– –	0.36 0.36	– –	0.44 0.44	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND		0–5.5	–	–	±0.1	–	±1.0	μA
I_{IN}	R_x / C_x Terminal Off-State Current	V_{IN} = V_{CC} or GND		5.5	–	–	±0.25	–	±2.50	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND		5.5	–	–	4.0	–	40.0	μA
I_{CC}	Active-State (Note 4) Supply Current	V_{IN} = V_{CC} or GND, R_x / C_x = 0.5 V_{CC}		3.0	–	160	250	–	280	μA
				4.5	–	380	500	–	650	
				5.5	–	560	750	–	975	

4. Per circuit.

AC ELECTRICAL CHARACTERISTICS (Note 5)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25 °C			T_A = −40 °C to 85 °C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Time (A, B–Q, $\overline{Q}$)	C_L = 15 pF	3.3 ±0.3	–	13.4	20.6	1.0	24.0	ns
		C_L = 50 pF		–	15.9	24.1	1.0	27.5	
		C_L = 15 pF	5.0 ±0.5	–	8.1	12.0	1.0	14.0	ns
		C_L = 50 pF		–	9.6	14.0	1.0	16.0	
t_{PLH}, t_{PHL}	Propagation Delay Time ($\overline{CLR}$ Trigger – Q, $\overline{Q}$)	C_L = 15 pF	3.3 ±0.3	–	14.5	22.4	1.0	26.0	ns
		C_L = 50 pF		–	17.0	25.9	1.0	29.5	
		C_L = 15 pF	5.0 ±0.5	–	8.7	12.9	1.0	15.0	ns
		C_L = 50 pF		–	10.2	14.9	1.0	17.0	
t_{PLH}, t_{PHL}	Propagation Delay Time (CLR – Q, Q)	C_L = 15 pF	3.3 ±0.3	–	10.3	15.8	1.0	18.5	ns
		C_L = 50 pF		–	12.8	19.3	1.0	22.0	
		C_L = 15 pF	5.0 ±0.5	–	6.3	9.4	1.0	11.0	ns
		C_L = 50 pF		–	7.8	11.4	1.0	13.0	
t_{WOUT}	Output Pulse Width	C_L = 50 pF, C_x = 28 pF, R_x = 2 kΩ	3.3 ± 0.3	–	160	240	–	300	ns
			5.0 ± 0.5	–	133	200	–	240	
		C_L = 50 pF, C_x = 0.01 μF, R_x = 10 kΩ	3.3 ± 0.3	90	100	110	90	110	μs
			5.0 ± 0.5	90	100	110	90	110	
		C_L = 50 pF, C_x = 0.1 μF, R_x = 1 kΩ	3.3 ± 0.3	0.9	1.0	1.1	0.9	1.1	ms
			5.0 ± 0.5	0.9	1.0	1.1	0.9	1.1	
Δt_{WOUT}	Output Pulse Width Error Between Circuits (In same Package)			–	±1	–	–	–	%
C_{IN}	Input Capacitance	V_{CC} = Open		–	4	10	–	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 6)		–	73	–	–	–	pF

5. Refer to Timing Chart.
6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:
   I_{CC} (opr.) = C_{PD} x V_{CC} x f_{IN} + $I_{CC}{}^1$ x Duty / 100 + I_{CC} / 2 (per Circuit)
   $I_{CC}{}^1$: Active Supply Current
   Duty: %

AC OPERATING REQUIREMENTS (Note 7)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25 °C			T_A = −40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
t_W(L), t_W(H)	Minimum Trigger Pulse Width		3.3	5.0	–	–	5.0	–	ns
			5.0	5.0	–	–	5.0	–	
t_W(L)	Minimum Clear Pulse Width		3.3	5.0	–	–	5.0	–	ns
			5.0	5.0	–	–	5.0	–	
t_{RR}	Minimum Retrigger Time	R_x = 1 kΩ, C_x = 100 pF	3.3 ± 0.3	–	60	–	–	–	ns
			5.0 ± 0.5	–	39	–	–	–	
		R_x = 1 kΩ,, C_x = 0.01μF	3.3	–	1.5	–	–	–	μs
			5.0	–	1.2	–	–	–	

7. Refer to Timing Chart.

DEVICE CHARACTERISTICS

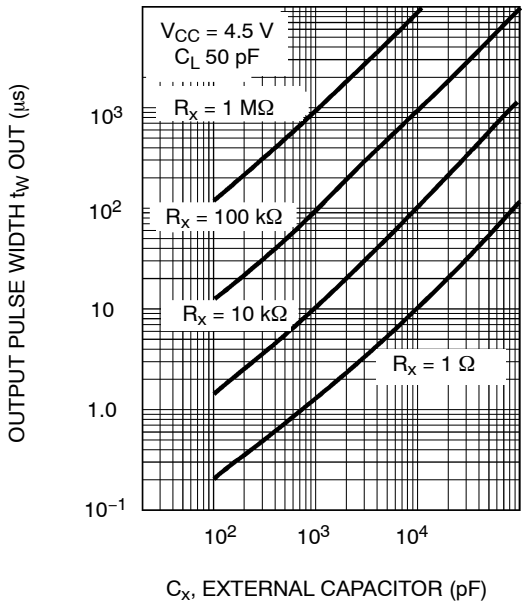


Figure 6. t_{wout} * C_x Characteristics (Typ.)

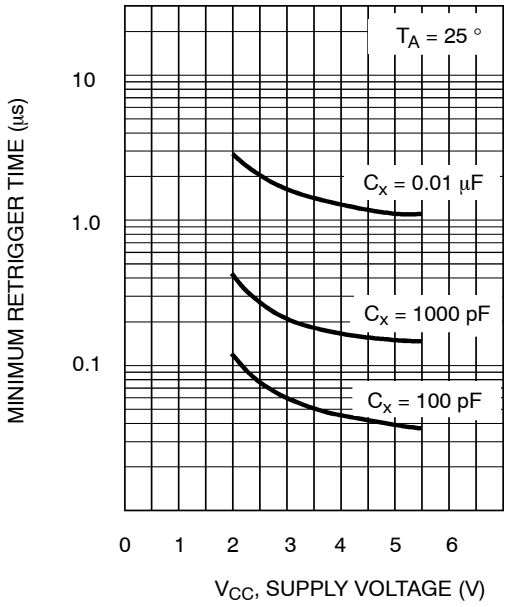


Figure 7. t_{RR} * V_{CC} Characteristics (Typ.)

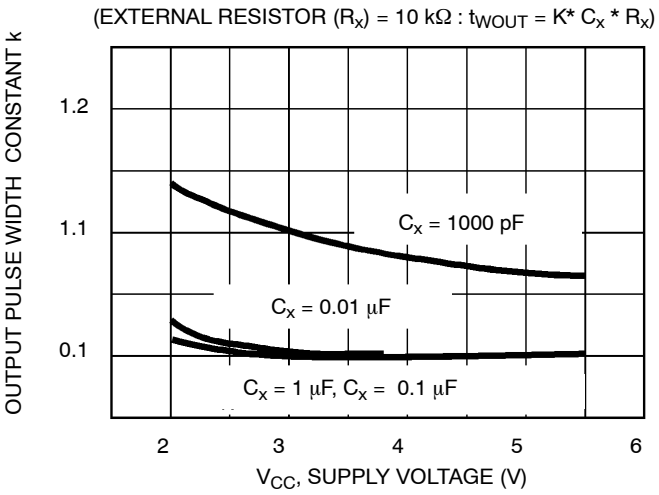


Figure 8. Output Pulse Width Constant K-Supply Voltage (Typ.)

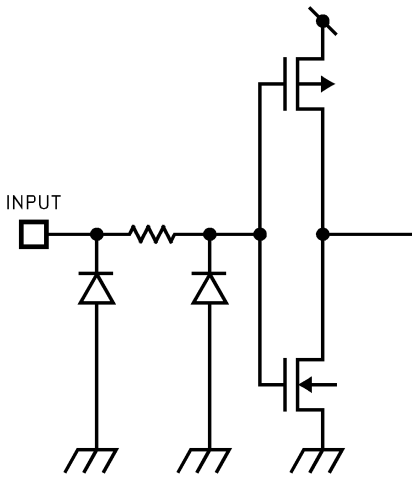


Figure 9. Input Equivalent Circuit

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74VHC123AMX	74VHC123A	SOIC-16	2500 Units / Tape & Reel
74VHC123AMTCX	V123A	TSSOP-16	2500 Units / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

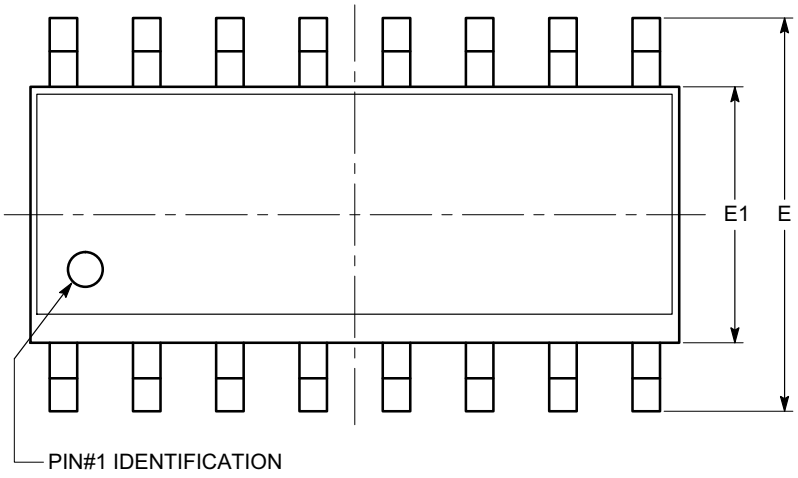
REVISION HISTORY

Revision	Description of Changes	Date
1	Converted the Data Sheet to **onsemi** format.	10/3/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

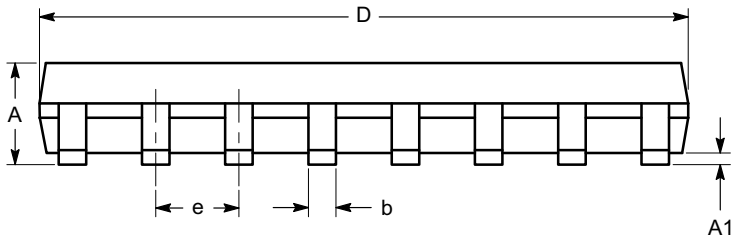
SOIC−16, 150 mils
CASE 751BG
ISSUE O

DATE 19 DEC 2008

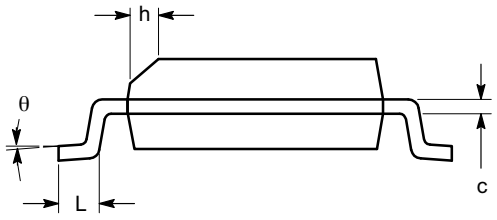


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



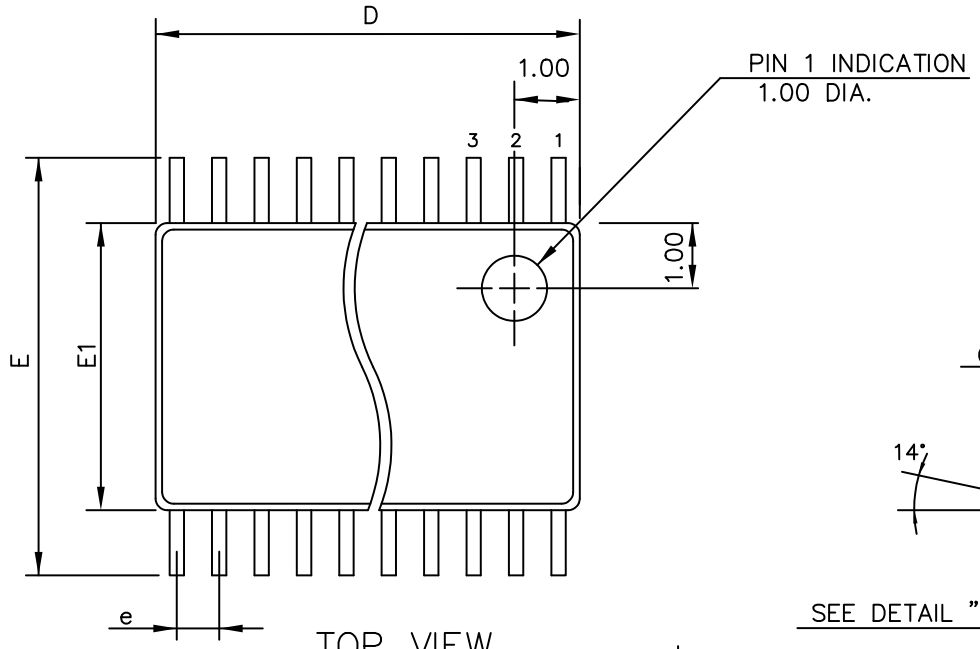
END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

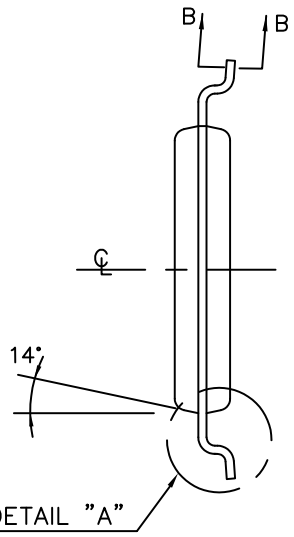
DOCUMENT NUMBER:	**98AON34275E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−16, 150 mils**		**PAGE 1 OF 1**

TSSOP 16
CASE 948AH
ISSUE O

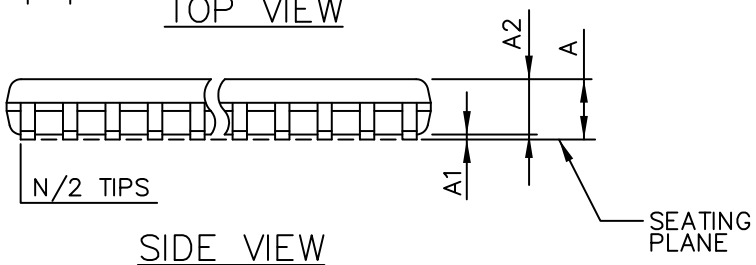
DATE 19 SEP 2008



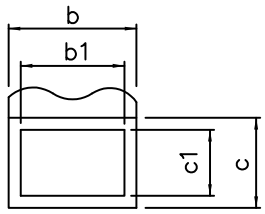
TOP VIEW



END VIEW



SIDE VIEW

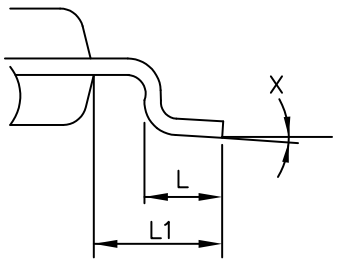


SECTION "B–B"

THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.10
A_1	0.05	——	0.15
A_2	0.85	0.90	0.95
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
c1	0.09	0.127	0.16
D	SEE VARIATIONS		
E1	4.30	4.40	4.50
e	0.65 BSC		
E	6.40 BSC		
L	0.50	0.60	0.70
L1	1.00 REF		
N	SEE VARIATIONS		
X	0°	——	8°

NOTE VARIATIONS	D	N
AA/AAT	3.00 BSC	8
AB–1/ABT	5.00 BSC	14
AB/ABT	5.00 BSC	16
AD/ADT	7.80 BSC	24



DETAIL 'A'

ALL DIMENSIONS IN MILLIMETERS

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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DESCRIPTION:	**TSSOP 16**	**PAGE 1 OF 1**

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