CMOS 4-BIT MICROCONTROLLER

TMP47C440AN
TMP47C440AF

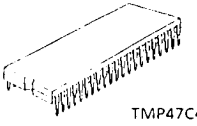
The 47C440A has 8-bit A/D converter and watchdog timer based on the TLCS-47 CMOS series.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C440AN	4096 x 8-bit	256 x 4-bit	SDIP42	TMP47C940AE
TMP47C440AF			QFP44	TMP47C940AG

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9μs (at 4.2MHz)
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available
- ◆I/O port (34 pins)
  - Input 2ports 5pins
  - Output 2ports 8pins
  - I/O 6ports 21pins
- ◆Interval timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Watchdog Timer
- ◆Serial Interface with 4-bit buffer
  External/internal clock, leading/trailing edge shift mode
- ◆8-bit successive approximate type A/D converter
  - With sample and hold
  - 8 analog inputs
  - Converting time : 48μs (4MHz)
- ◆High current outputs
  LED direct drive capability (typ. 20mA x 8bits)
- ◆Hold function
  Battery/Capacitor back-up
- ◆Real Time Emulator : BM47214A

SDIP42

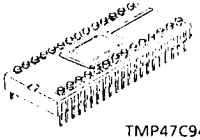


TMP47C440AN

QFP44

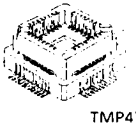
TMP47C440AF

SDIC42



TMP47C940AE

QFC44



TMP47C940AG

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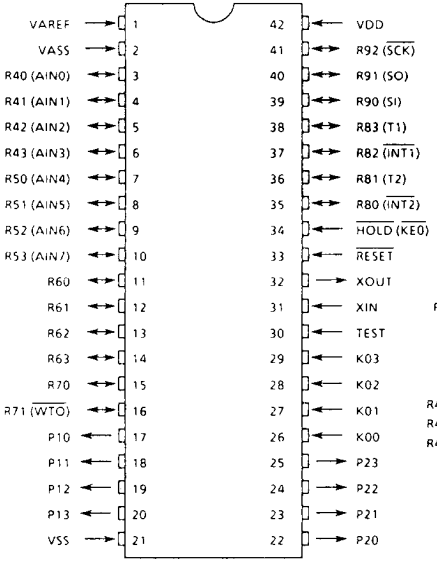
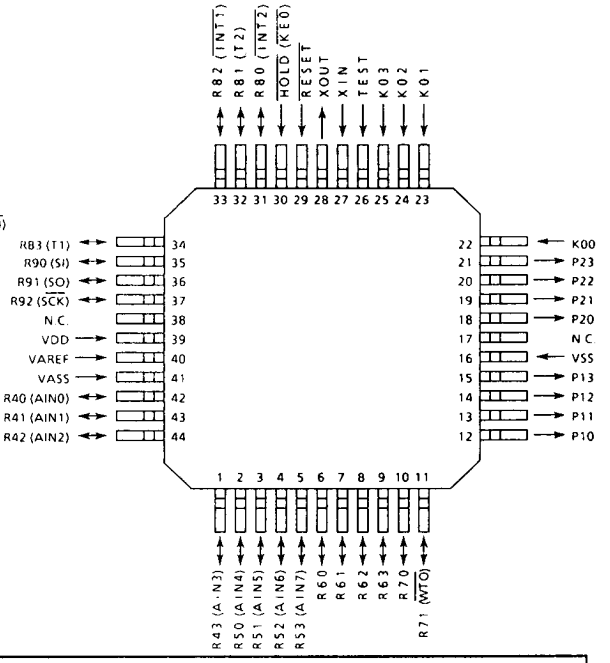
PIN ASSIGNMENTS (TOP VIEW)

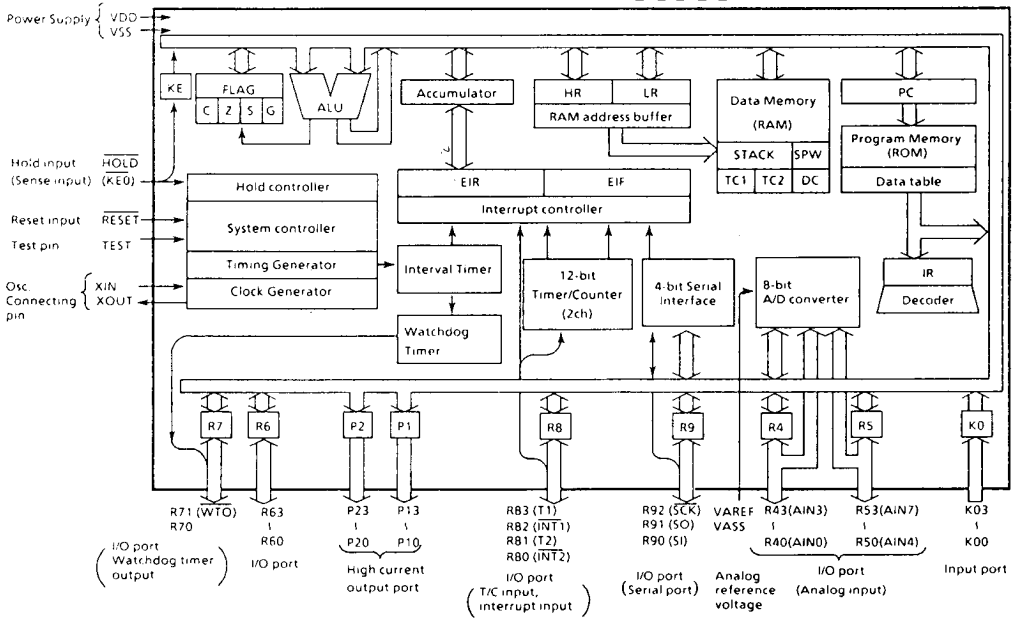
(1) SDIP42



(2) QFP44



BLOCK DIAGRAM



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PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
P13 - P10	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
P23 - P20			
R43 (AIN3) - R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When used as input port or analog input, the latch must be set to "1".	A / D converter analog input
R53 (AIN7) - R50 (AIN4)			
R63 - R60	I/O	4-bit I/O port with latch	
R71 ($\overline{WTO}$)	I/O (Output)	2-bit I/O port with latch. When used as input port or watchdog timer output, the latch must be set to "1".	Watchdog timer output
R70	I/O		
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O(I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	HOLD request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	
VAREF		A/D converter analog reference voltage (High)	
VASS		A/D converter analog reference voltage (Low)	

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OPERATIONAL DESCRIPTION

Conserning the 47C440A, the hardware configuration and operation of hardwares are described.
As the description is porvided with priority on those parts deffering from the 47C400A, the technical data sheets for the 47C400A shall also be referred to.

1. SYSTEM CONFIGURATION

(1) I/O Ports
(2) A / D Converter
(3) Watchdog Timer

2. PERIPHERAL HARDWARE FUNCTION

2.1 Ports

The 47C440A has 10 I/O ports (34 pins) each as follows :

① K0 ; 4-bit input
② P1, P2 ; 4-bit output
③ R4, R5 ; 4-bit input/output (shared with the A/D converter analog inputs)
④ R6 ; 4-bit input/output
⑤ R7 ; 2-bit input/output (shared with the watchdog timer output)
⑥ R8 ; 4-bit input/output(shared with external interrupt request input and timer/counter input)
⑦ R9 ; 3-bit input/output (shared with serial port)
⑧ KE ; 1-bit sense input (shared with hold request/release signal input)

This section describes ports of ③ and ⑤ which are changed from the 47C400A.
Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Ports R4 (R43-R40), R5 (R53-R50)
Ports R4 and R5 are 4-bit I/O ports with latch shared by the analog inputs for A/D converter. When used as an input ports or analog inputs, the latch should be set to "1". If other port is used as an output, be careful not to execute the output instruction for any port during A/D conversion in order to keep accuracy of conversion. The latch is initialized to "1" and analog input is selected R40 (AIN0) pin during reset.

Port R4 (Port address OP04 / IP04)

3	2	1	0
R43 (AIN3)	R42 (AIN2)	R41 (AIN1)	R40 (AIN0)

Port R5 (Port address OP05 / IP05)

3	2	1	0
R53 (AIN7)	R52 (AIN6)	R51 (AIN5)	R50 (AIN4)

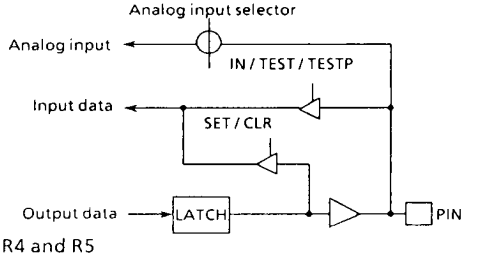

Figure 2-1. Port R4 and R5

(2) Port R7 (R71, R70)
Port R7 is 2-bits I/O port with latch. R71 pin is shared by the watchdog timer output. To use R71 pin for the watchdog timer output, the latch should be set to "1". The latch is initialized to "1" during reset. R70 pin is normal I/O pin. R72 and R73 pins do not exist actually but "1" is read when an input instruction is executed.

Port R7 (Port address OP07 / IP07)

3	2	1	0
		R71 ($\overline{WTO}$)	R70

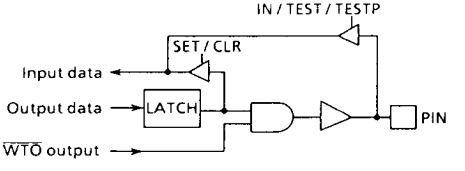

Figure 2-2. Port R7

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Port Address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A,%p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note 2)	○	○	–
02	P2 output latch	P2 output port	○	○	○	○	○	○	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port (Analog input)	R4 output port	○	○	○	–	–	○	○
05	R5 input port (Analog input)	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	A / D status input	——	○	–	–	–	–	○	–
0D	A / D converted value	——	○	–	–	–	–	–	–
0E	SIO, Hold status	——	○	–	–	–	–	○	–
0F	Serial recieve buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	A / D analog input selector	–	○	–	–	–	–	–
13	Undefined	A / D start register	–	○	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	Watchdog Timer control	–	○	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval Timer intrrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note 1. "——" means the reserved state. Unavailable for the user programs.

Note 2. The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Table 2-1. Port Address Assignments and Available I/O Instructions

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2.2 A/D Converter

The 47C440A has a 8-bit successive approximate type A/D converter and is capable of processing 8 analog inputs.

2.2.1 Circuit configuration

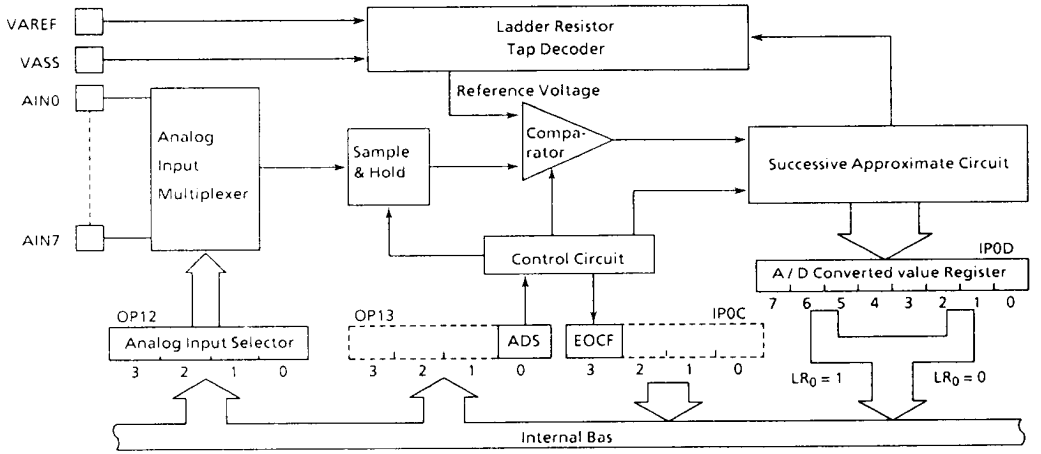

Figure 2-3. Block Diagram of A/D Converter

2.2.2 Control of A/D converter

The operation of A/D converter is controlled by a command. The command register is accessed as port adderesses OP12 and OP13. A/D converted value and end of conversion flag (EOCF) can be known by accessing port addresses IP0D and IP0C.

(1) Analog input selector

Analog inputs (AIN0 through AIN7) are selected by values of this register.

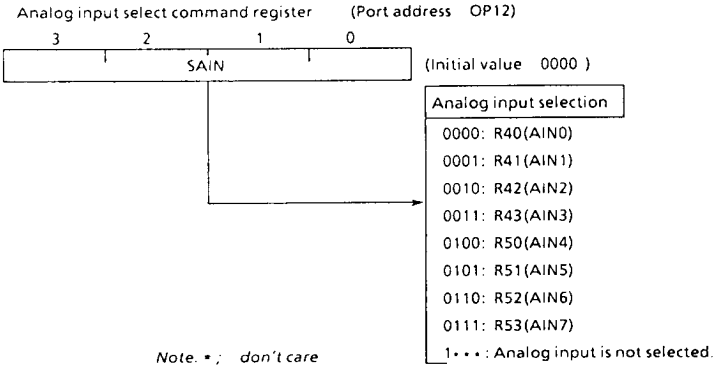

Figure 2-4. Analog input selector

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(2) Start of A/D conversion

A/D conversion is started when ADS is set to "1". After the conversion is started, ADS is cleared by hardware. If the restart is requested during the conversion, the conversion is started again at the time.

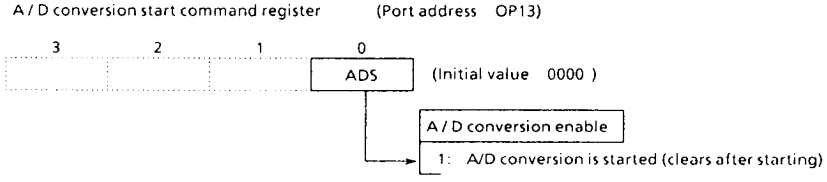

Figure 2-5. A/D conversion start register

(3) A/D converted value register

An A/D converted value is read by accessing port address IP0D. An A/D converted value is read by splitting into upper 4 bits and lower 4 bits by a value of LR_0 (LSB of the L registers).

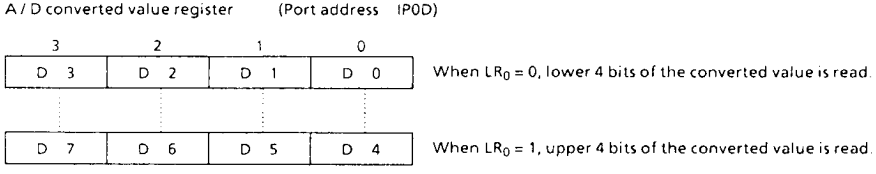

Figure 2-6. A/D converted value register

(4) A/D converter status register

End of Conversion Flag (EOCF) is a single bit flag showing the end of conversion and is set to "1" when conversion ended. When both upper 4 bits and lower 4 bits of a converted value are read or A/D conversion is started, EOCF is cleared to "0".

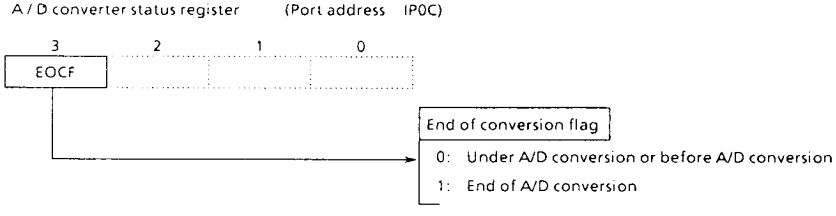

Figure 2-7. A/D converter status register

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2.2.3 How to use A/D converter

Apply positive of analog reference voltage to the VAREF pin and negative to the VASS pin. The A/D conversion is carried out by splitting reference voltage between VAREF and VASS to bit corresponding voltage by a ladder resistor and making a judgement by comparing it with analog input voltage.

(1) Start of A / D conversion

Prior to conversion, select one of the analog input AIN0 through AIN7 by the analog input selector. Place output of the analog input, which is to be A/D converted, in the high impedance state by setting "1". If other port is used as an output, be careful not to execute the output instruction for any port during conversion in order to keep accuracy of conversion.

A/D conversion is started by setting ADS (bit 1 of the A/D conversion start register). When conversion ends after 24 instruction cycles, EOCF showing the end of conversion is set to "1".

(2) Reading of an A/D converted value

After the end of conversion, read an A/D converted value is read by splitting into lower 4 bits and upper 4 bits by the A/D converted value register (IP0D).

Lower 4 bits of the A/D converted value can be read when LR_0 = 0 and upper 4 bits when LR_0 = 1. Usually an A/D converted value is stored in RAM by an instruction [IN %p, @HL]. Further, if an A/D converted value is read during the conversion, it becomes an indefinite value.

(3) A / D conversion with HOLD operation

When the HOLD operation is started during the conversion, the conversion is terminated and an A/D converted value becomes indefinite. Therefore, EOCF is kept clear to "0" after release from the HOLD operation. However, if the HOLD operation is started after the end of A/D conversion (after EOCF has been set), A/D converted value and status of EOCF are held.

Example: Selecting analog input (AIN4), starting A/D conversion, monitoring EOCF and storing lower 4 bits and upper 4 bits of a converted value to RAM [10_H] and RAM [11_H] respectively.

```
        LD      A, #4          ; Selects analog input (AIN4)
        OUT     A, %OP12
        LD      A, #1          ; Start of A/D conversion
        OUT     A, %OP13
SLOOP : TEST    %IP0C, 3       ; To wait until EOCF goes to "1"
        B       SLOOP
        LD      HL, #10H       ; HL ← 10H
        IN      %IP0D, @HL     ; RAM [10H] ← Lower 4 bits
        INC     L              ; Increment of L registers
        IN      %IP0D, @HL     ; RAM [11H] ← Upper 4 bits
```


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2.3 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (ranaway) of program due to external noise or other causes and return the operation to the normal condition.
The watchdog timer output is output to R71 must be set to "1". Further, during reset, the output latch of R71 is set to "1", and the watchdog timer becomes disable state.
The initialization at time of runaway will become possible when the $\overline{WTO}$ pin and $\overline{RESET}$ pin are connected each other.

2.3.1 Configuration of Watchdog Timer

The watchdog timer consists of 3-stage binary counter, flip-flop (F/F), and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

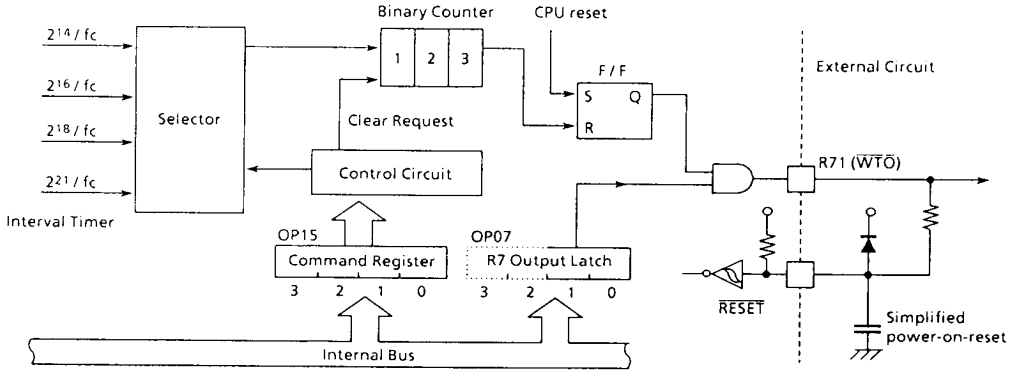

Figure 2-8. Watchdog Timer

2.3.2 Control of watchdog timer

The watchdog timer is controlled by the command register (OP15). This command register is initialized to "1000_B" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

① At first, detection time of the watchdog timer should be set and binary counter should be cleared.
② The watchdog timer should be become enable.
③ Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken place for some reason and binary counter is not cleared, the F/F is cleared to "0" at the rising edge of the binary counter and signal of runaway detection is become active ($\overline{WTO}$ output is "L").

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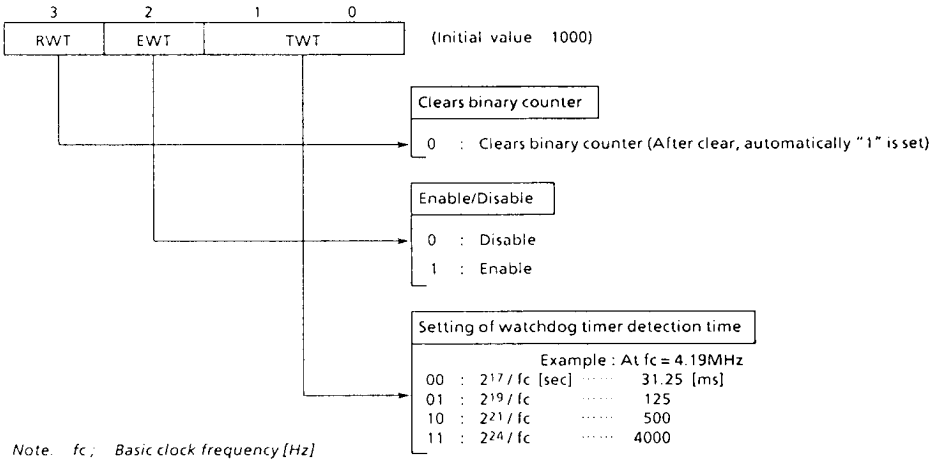
Watchdog Timer control command register (Port address OP15)



Note. fc ; Basic clock frequency [Hz]

Figure 2-9. Command Register

Example : To set the watchdog detection time (2^{21} / fc[sec]). And to enable the watchdog timer.

```
                LD      A, #0010B     ; OP15 ← 0010B
                                        (Sets WDT detection time. Clears binary counter)
                OUT     A, %OP15
                LD      A, #1110B     ; OP15 ← 1110B (Enables WDT)
               ┌OUT     A, %OP15
               │ :
Within WDT     │ :
               │ :
detection time │
               │LD      A, #0110B     ; OP15 ← 0110B (Clears binary counter)
               └OUT     A, %OP15
                :
                :
```

Note. It is not necessary to set RWT to "1". Note that both EWT (Enable Watchdog Timer) and RWT should not be set to "1" at the same time.

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
Input Voltage	V_{IN}		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Ports P1, P2, R6 - R9	− 0.5 to 10	
	V_{OUT3}	Analog inputs	− 0.5 to V_{DD} + 0.5	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	30	mA
	I_{OUT2}	Ports R6 - R9	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	120	mA
Power Dissipation [T_{opr} = 70℃]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc			0.4	4.2	MHz

Note. Input voltage V_{IH3}, V_{IL3} : in the HOLD mode

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D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Input Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	- 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output Low Voltage	V_{OL2}	Except XOUT, ports P	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Low output Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	—	20	—	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	—	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3V/0.2V
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

A / D CONVERSION CHARACTERISTICS

(T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} − 1.5	—	V_{DD}	V
	V_{ASS}		V_{SS}	—	1.5	
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} − V_{ASS}	2.5	—	—	V
Analog Input Voltage	V_{AIN}		V_{ASS}	—	V_{AREF}	V
Analog Supply Current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0V, V_{SS} = 0.0V V_{AREF} = 5.000V V_{ASS} = 0.000V	—	—	± 1	LSB
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	
Total Error			—	—	± 2	

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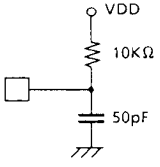
A. C. CHARACTERISTICS

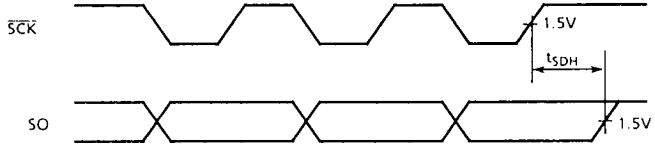
(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
A/D Sampling Time	t_{AIN}	fc = 4MHz	—	4	—	μs
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ − 300	—	—	ns

Note. Shift Data Hold Time
External circuit for $\overline{SCK}$ pin and SO pin



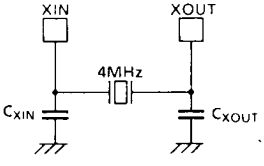
Serial port (completion of transmission)



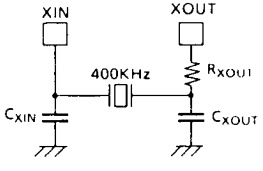
RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = − 30 to 70°C)

(1) 4MHz
Ceramic Resonator
CSA4. 00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-4. 00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF
Crystal Oscillator
204B-6F 4. 0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF



(2) 400KHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ



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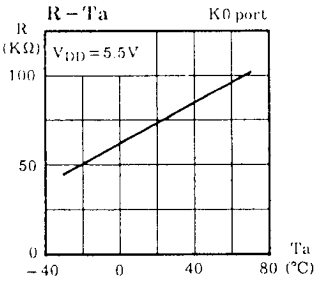
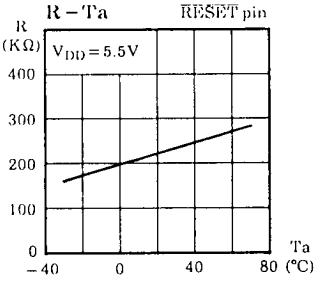
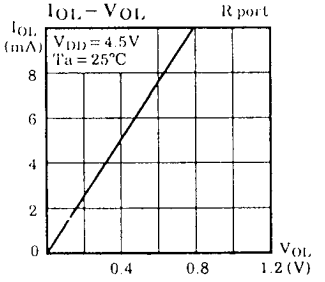
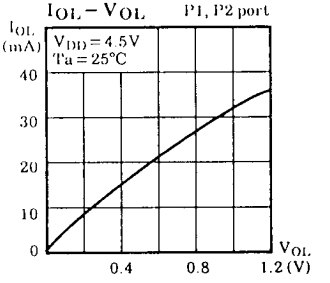
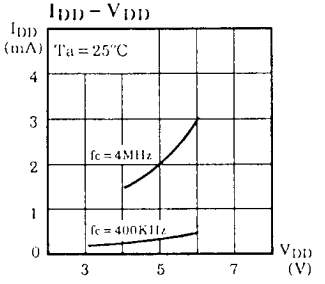
TYPICAL CHARACTERISTICS

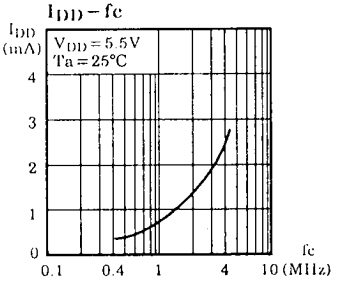












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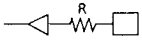
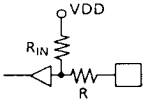
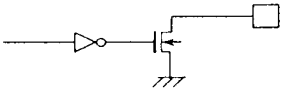
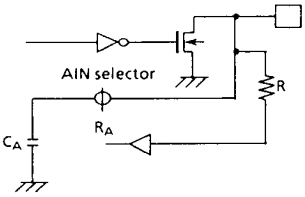
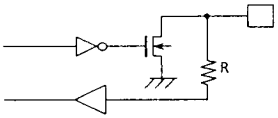
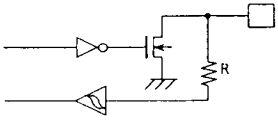
INPUT/OUTPUT CIRCUITRY

(1) Control pins

The input/output circuitries of the 47C440A control pins are similar to that of the 47C400A.

(2) I/O Ports

The input/output circuitries of the 47C440A I/O ports are shown below, any one of the circuitries can be chosen by a code (SA-SC) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE			REMARKS
		SA	SB	SC	
K0	Input				Pull-up / pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P1 P2	Output				Sink open drain output Initial "Hi-Z" High current I_{OL} = 20mA (typ.)
R4 R5	I/O				Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.) Analog input R_A = 5KΩ (typ.) C_A = 12pF (typ.)
R6 R7	I/O				Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	I/O				Sink open drain output Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)

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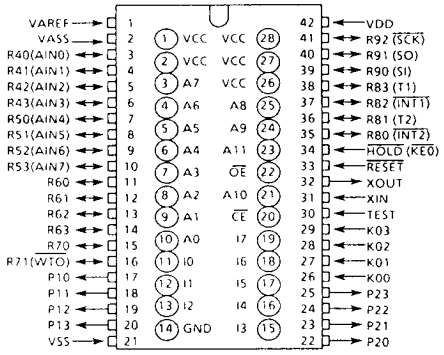
CMOS 4-BIT MICROCONTROLLER

TMP47C940AE
TMP47C940AG

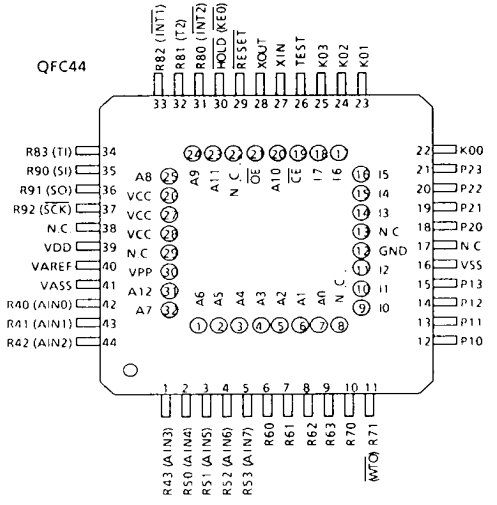
The 47C940A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C440A/242A application systems (programs).
The 47C940A is pin compatible with the 47C440A which are mask-programed ROM devices. Also, pin compatibility with the 47C242A is possible by using the 42-to-30 pin conversion adapter socket (BM1113).

PIN ASSIGNMENT (TOP VIEW)

SDIC42



QFC44



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 ~ A0	Output	Program memory address output
I7 ~ I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5 to 6.0V C_L = 100pF Topr = − 30 to 70°C	−	−	150	ns
Data Setup Time	t_{IS}		150	−	−	ns
Data Hold Time	t_{IH}		50	−	−	ns

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NOTES FOR USE

(1) Program memory

The program area are as shown in Figure 1. When this chip is used as evaluator of the 47C242, data conversion table for [OUTB @HL] instruction must be allocated at two areas and they must be the same contents as shown in Figure 1(b).

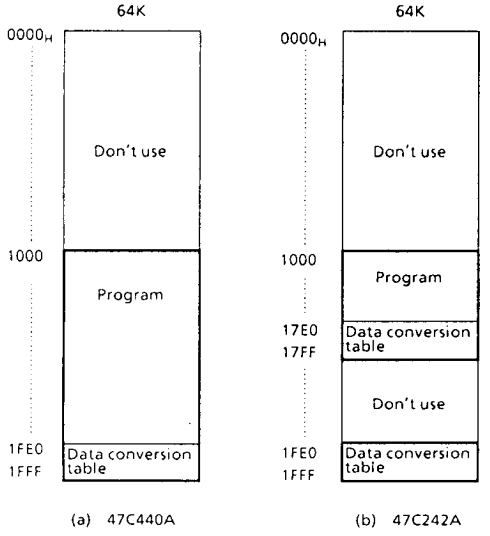

Figure 1. Program area

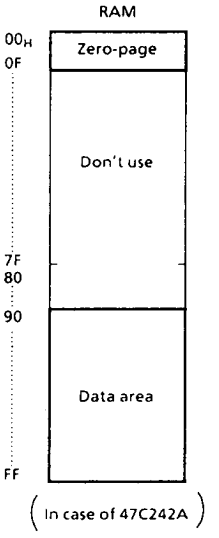

Figure 2. RAM addressing

(2) Data memory

The 47C940A contains 256 x 4-bit (equivalent to 47C440A) data memory. When the 47C940A is used as evaluator of the 47C242A, programming should be performed assuming that the RAM is assigned to addresses $00 \sim 0F_H$ and $90 \sim FF_H$ as show in Figure 2 by considering the application software evaluation.

(3) I/O ports

Input/Output circuitries of I/O ports in the 47C940A are similar to the code TA of the 47C440A.

When this chip is used as evaluator with other I/O code, it is nacessary to provide the external resistors. This is also the same when used as the 47C242A evaluator (the 47C242A does not have ports R5 and R6).

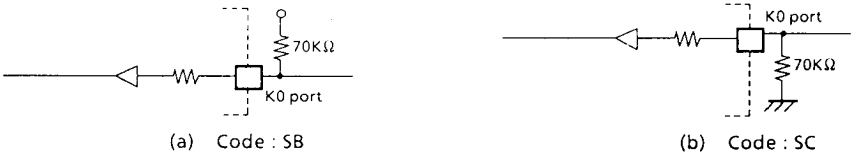

Figure 3. I/O code and external circuitry

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