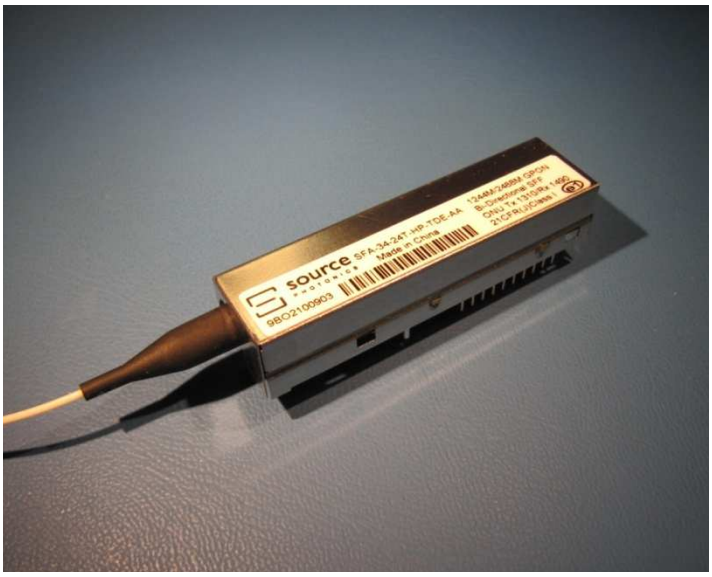
SFx-xx-24T-HP-CxE-xx

Integrated Diplexer Transceiver

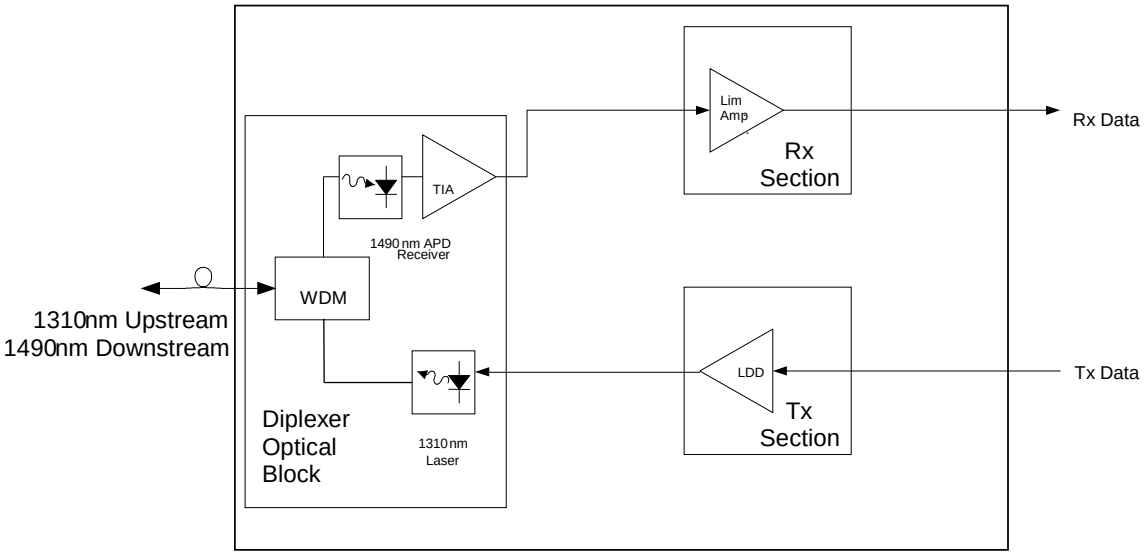


Features

- Single Fiber, CWDM Integrated Diplexer Transceiver
- 2x5 SFF pinout
- 2x10 SFF pinout supports I^2C digital diagnostics
- Voice/Data FTTx ONT/ONU Applications
- 1244 Mbps Tx, 2488 Mbps Rx Asymmetric Data Rate
- 5 Wavelength Pairs Available
- Burst Mode Transmission
- TX Burst Mode Detection, TX-SD
- Commercial temperature
- 28 dB link budget; 20 km reach
- Compliant to IEC-60825 Class 1 laser diode
- SC/APC or SC/UPC fiber connector
- RoHS compliant

- Digital Transmitter: A CWDM laser diode is employed for upstream transmission at OC-24 (1244Mbps). The optical transmitter includes a back facet photodetector to monitor laser power for APC control.

- Digital Receiver: An APD with TIA is employed for downstream data reception at OC-48 (2488Mbps). A post amplifier is also included for CML output compatibility.



Diplexer Block Diagram

Absolute Maximum Ratings

Usage of this transceiver shall adhere to the following absolute maximum ratings. Stresses beyond those in Table 1 may cause permanent damage to the unit. These are stress ratings only, and functional operation of the unit at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect unit reliability.

Table 1 - Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit/Conditions
Ambient Storage Temperature	-40	85	ºC
Operating Temperature*	0	70	ºC, C-Temp
Operating Humidity Range	10%	90%	non-condensing
ESD Sensitivity (Human Body Model)	-	1000	V
Lead Soldering Temperature	-	260ºC	10 sec
Vcc_Rx	-0.4	+4.2	V
Vcc_Tx	-0.4	Vcc_Rx + 1	V

*Operating temperature minimum is ambient, maximum is module case temperature.

Module Characteristics

Table 2 - Module Characteristics

Parameter	Minimum	Typical	Maximum	Unit/Conditions
Tx to Rx Crosstalk	-	-	-47	dB
Total TX and RX Supply Current	-	-	350	mA

Functional Characteristics

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Table 3 – Digital Transmitter Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operating Voltage	3.14	3.30	3.46	V	V_{CC} referenced to GND_Tx
Data Rate	-	1244.16	-	Mbps	
Average Optical Output Power, P_0 (BOL)	1.5	-	5	dBm	
Average Optical Output Power, P_0 (BOL)	0.5	-	5	dBm	
Output Power at Transmit Off	-	-	-40	dBm	
Extinction Ratio	10	-	-	dB	PRBS 2^{23}-1, NRZ, 50% duty cycle
Transmitter Output Eye	G.984.2 Figure 3				
Optical Rise and Fall Time	-	250	-	ps	20% to 80%
Center Wavelength		1271 1291 1311 1331 1351		nm	C-temp ±6.5nm
SMSR		30		dB	
Differential Input Voltage, V_{in}	200	-	1600	mVp-p	TXD+/-. DC-coupled
Common-Mode Input Voltage	GND_Tx + 1.4	-	Vcc - (V_{in}/2) - 0.1	V	DC coupled
Tx Burst Enable Time	-	-	12.86	ns	16 bits data @ 1244Mbps
Tx Burst Disable Time	-	-	12.86	ns	16 bits data @ 1244Mbps
Jitter Generation	-	-	0.2	UI	4 kHz to 10 MHz
TX_DIS Input Low	0		0.8	V	
TX_DIS Input High	2.0		Vcc_RX	V	
TX_SD timing “D”			1000	ns	See figure 3
TX_SD timing “X”			350	ns	See figure 3

Refer to Figure 1 which schematically describes the high speed data inputs/outputs of the optical transceiver module.

For CML
Tx/Rx Data

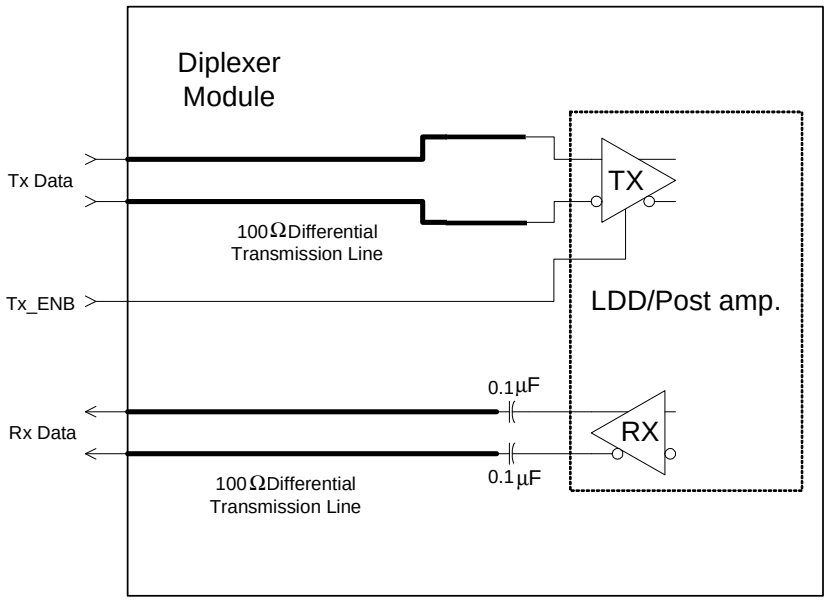


Figure 1 - Schematic representation of the module high speed inputs/outputs

Table 4 – Digital Receiver Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operating Voltage	3.14	3.30	3.46	V	V_{CC} referenced to GND_RX
Data Rate	-	2488.32	-	Mbps	
Operational Wavelength Range		1451 1471 1491 1511 1531		nm	
Received Optical Power, BOL	-28.0	-	-8	dBm	PRBS 2^{23}-1, 50% duty cycle
Received Optical Power, EOL	-27.0	-	-8	dBm	PRBS 2^{23}-1, 50% duty cycle
Data Output Rise and Fall Time	-	160	-	ps	20% to 80%
Signal Detect Assertion Level	-	-	-31	dBm	Transition during increasing light
Signal Detect De-Assertion Level	-45	-	-	dBm	Transition during decreasing light
Signal Detect Hysteresis	0.5	-	6	dB	
Differential Output Voltage	300	-	1200	mV	CML output, ac coupled (0.1µF)
Signal Detect Output HIGH Voltage	2.4	-	-	V	LVTTL with internal 4.7kΩ pull up resistor. Asserts HIGH when input data amplitude is above threshold.
Signal Detect Output LOW Voltage	-	-	0.6	V	LVTTL. De-asserts LOW when input data amplitude is below threshold .
RSSI Range	-28	-	-8	dBm	2x10 only
RSSI Accuracy	-3	-	+3	dB	2x10 only

Table 5 - Microcontroller Specifications

Parameter	Minimum	Typical	Maximum	Unit	Notes
Operating Voltage	3.14	3.30	3.46	V	
SDA[a]	-	-	-	-	LVTTL, open collector serial data line from the I²C bus to the on board Microcontroller. 100kbps max. data rate.
SCL[b]	-	-	-	-	LVTTL, open collector serial clock line from the I²C bus to the on board Microcontroller.
Reset hold[c]	30	-	-	ms	LVTTL input, internal 50kΩ pull-up. Active Low

[a] I²C SDA and SCL must be open collector or open drain connections.
[b] Clock stretching, as per paragraph 13.2 of the I²C Bus Standard, must be implemented to operate correctly.
[c] Please see Table 6 and the timing diagram in Figure 2 below for the recommended system start-up sequence.

Table 6 – Suggested Start-up Sequence

Step	Action
1	Power up the host system, with the RESET pin pulled to ground via a ≤4.7kΩ resistor.
2	Drive the RESET pin LOW.
3	Ensure power to the unit is on.
4	Drive the RESET pin HIGH to release the unit to become operational.
5	Read byte A2.6E several times. There will be a NACK until the processor is booted, followed by a 01 (DATA READY BAR) until the A2D data is ready, followed by 00 (assuming TXDIS and TXFAIL are inactive).
6	The unit is now ready for normal operation.

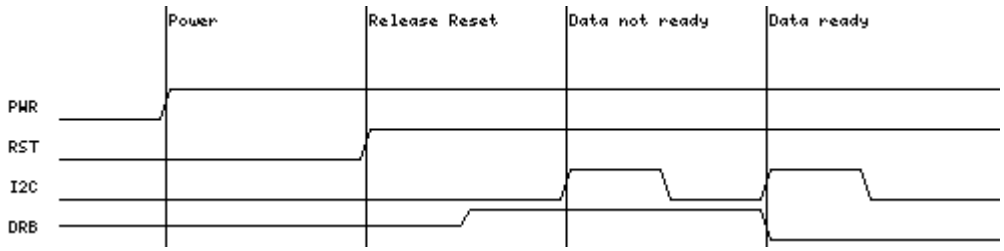
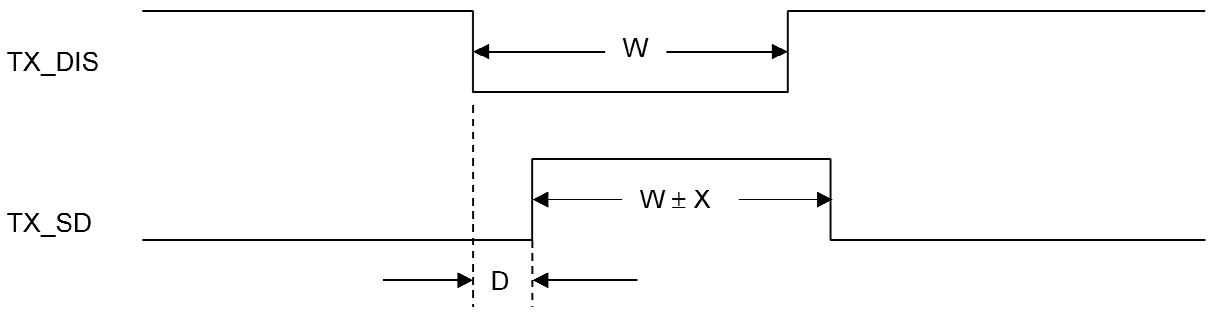


Figure 2 - Recommended transceiver module start-up sequence

Fig 3 TX_SD Timing Diagram



2x5 Pin Definitions

Refer to Table 7 for a description of the function of each I/O pin.

Pin Number	Label	Definition
1	GND_RX	Digital Rx Ground
2	Vcc_RX	Digital Rx Vcc
3	SD	Signal Detect output, pull up internally. Asserts high when input optical power level is above threshold
4	RxD-	RX data bar output, CML. 50Ω terminated to Vcc and AC coupled to module output (0.1μF)
5	RxD+	RX data output, CML. 50Ω terminated to Vcc and AC coupled to module output (0.1μF)
6	Vcc_TX	Digital Tx Vcc
7	GND_TX	Digital Tx Ground
8	TX_DIS	Tx Disable, LVTTL Input (1=TX OFF, 0=TX ON)
9	TxD+	Tx data input, CML. Internally DC coupled. 100Ω differential termination.
10	TxD-	Tx data bar input, CML. Internally DC coupled. 100Ω differential termination.

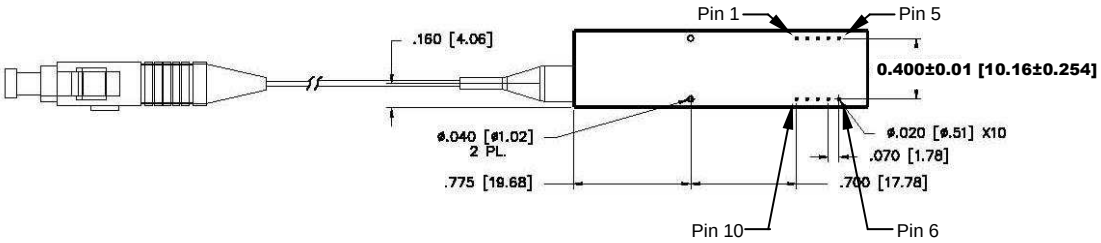
2x10 Pin Definitions

Refer to Table 8 for a description of the function of each I/O pin.

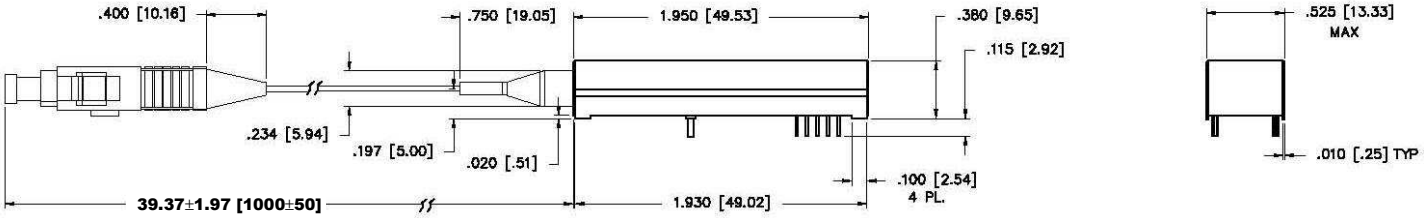
Table 8 - Module Pin Definitions

Pin Number	Label	Definition
1	NC	No User Connection
2	GND_RX	Digital Rx ground
3	GND_RX	Digital Rx ground
4	NC	Reserved, No User Connection
5	NC	Reserved, No User Connection
6	GND_RX	Digital Rx Ground
7	Vcc_RX	Digital Rx Vcc
8	SD	Signal Detect output, pull up internally (4.7kΩ). Asserts high when input optical power level is above threshold
9	RxD-	RX data bar output, CML. 50Ω terminated to Vcc and AC coupled to module output (0.1µF)
10	RxD+	RX data output, CML. 50Ω terminated to Vcc and AC coupled to module output (0.1µF)
11	Vcc_TX	Digital Tx Vcc
12	GND_TX	Digital Tx Ground
13	TX_DIS	Tx Disable, LVTTL Input (1=TX OFF, 0=TX ON), internal 47kΩ pull-up.
14	TxD+	Tx data input, CML. Internally DC coupled. 100Ω differential termination.
15	TxD-	Tx data bar input, CML. Internally DC coupled. 100Ω differential termination.
16	GND_TX	Digital Tx Ground
17	SCL	I2C Clock input
18	SDA	I2C Data input/output
19	TX_Fault	TX Fault Alarm, LVTTL, TX Fault state=High, TX Normal state=Low.
20	TX_SD	TX Signal Detect, TX Active state=High. See TX_SD diagram.

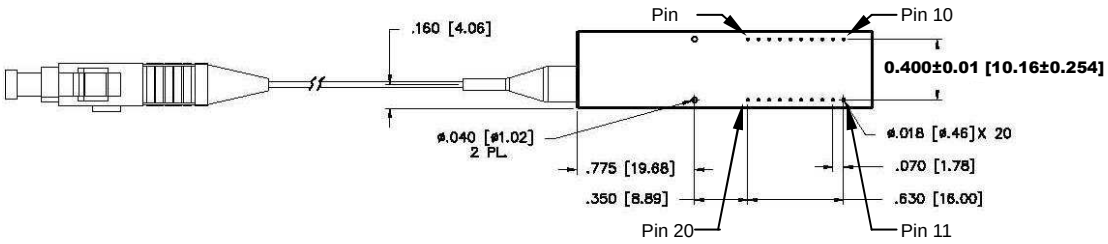
SFF 2x5 Package Diagram



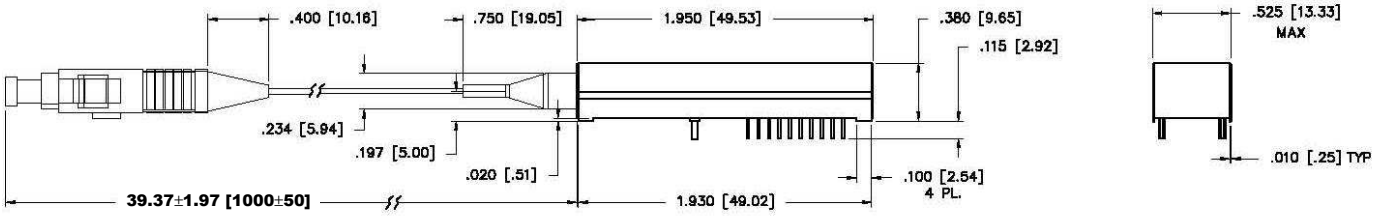
Bottom View



SFF 2x10 Package Diagram



Bottom View



Ordering Information

Table 9 - Ordering Information

	Connector		TX & RX Wavelength (nm)		Temperature Range	Digital Diagnostic	Design Revision	Customer Specific
SF	x	**-**	xx	**-24T-HP-**	**C**	x	**E**	-xx
	A = APC		**AJ** = 1271 & 1451		**C** = Commercial Temp (0 to 70℃)	**N** = Non-Diagnostic		
	U = UPC		**BK** = 1291 & 1471			**D** = Diagnostic		
			CL = 1311 & 1491					
			DM = 1331 & 1511					
			EN = 1351 & 1531					

Example: **SFA-CL-24T-HP-CDE** = Transceiver with APC connector, TX=1311nm, RX=1491nm, Commercial Temp, Diagnostic.

Table 10 - Device Handling/ESD Protection

The devices are static sensitive and may easily be damaged if care is not taken during handling. The following handling practices are recommended.	
1	Devices should be handled on benches with conductive and grounding surfaces.
2	All personnel, test equipment and tools shall be grounded.
3	Do not handle the devices by their leads.
4	Store devices in protective foam or carriers.
5	Avoid the use of non-conductive plastics, rubber, or silk in the area where the devices are handled
6	All modules shall be packaged in materials that are anti-static to protect against adverse electrical environments.
7	Avoid applications of any voltage higher than maximum rated voltages to this part. For proper operation, any VIN or VOUT should be constrained to the range GND ≤ (VIN or VOUT) ≤ VCC. Unused inputs must always be tied to an appropriate logic voltage (e.g. either GND or VCC). Unused outputs must be left open.

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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Contact

SOURCE PHOTONICS

20550 NORDHOFF ST.

CHATSWORTH, CA 91311

sales@sourcephotonics.com

Tel: 818-773-9044 Fax: 818-576-9486

Or visit our website: http://www.sourcephotonics.com